SRS and TDP testing in Clause 95

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Background

- Table 95-7 defines 100GBASE-SR4 receive characteristics
  - Comment c (pertaining to stressed receiver sensitivity - SRS) points to “conformance test signal at TP3 (see **95.8.8**) for the BER specified in 95.1.1” (5e-5).
- Subclause 95.8.8 specifies “measured using the method defined by **52.9.9**” with a list of exceptions:

a) The reference test procedure for a single lane is defined in 52.9.9. See 95.8.1.1 for multilane considerations.

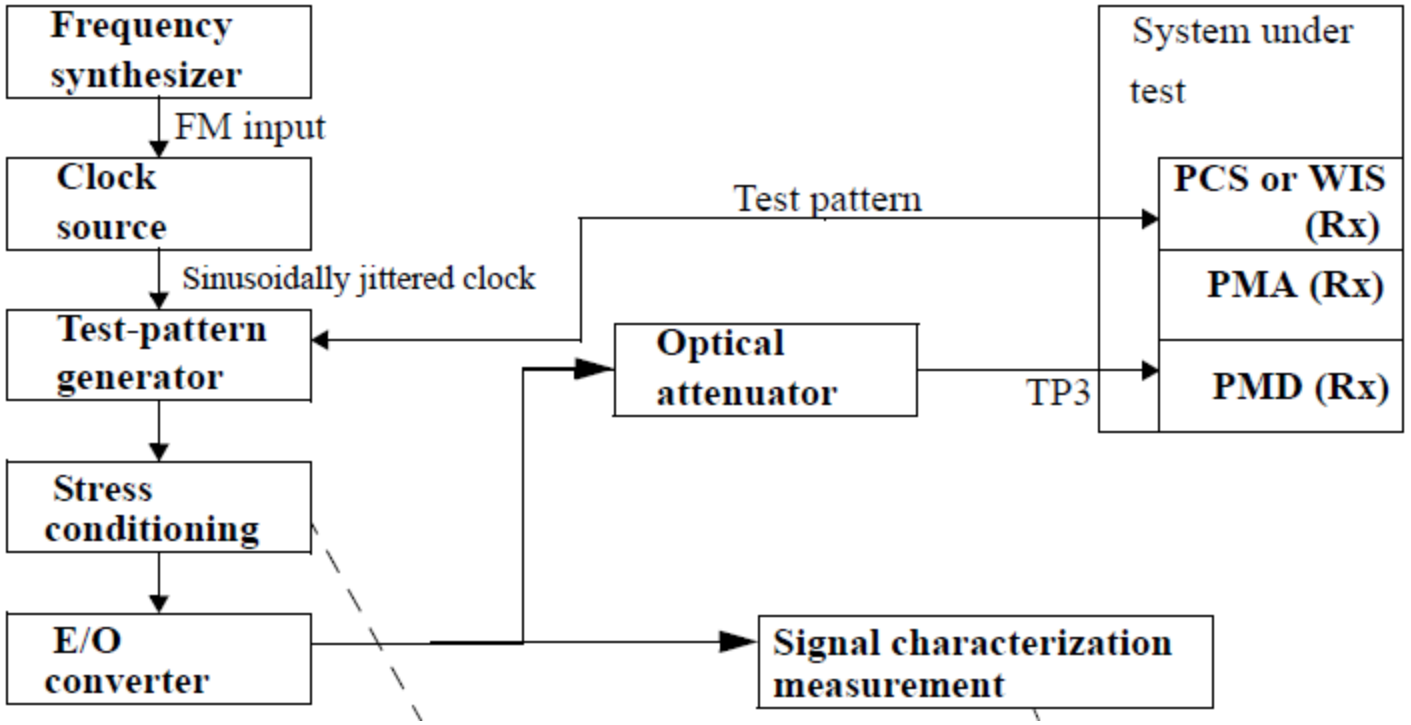
…

f) Pattern specified in Table 95–10 ➔ either 3 (PRBS31) or 5 (RS-FEC encoded scrambled idle).

Details of clause 52 test method

- 52.9.9 and its subclauses define the test using the PCS attached to the PMD under test.
  - This is obvious from figure 52-10 where “system under test” includes PMA and PCS/WIS blocks in addition to the PMD, and is fed with the test pattern to enable comparison.
  - 52.9.9.1 specifies error counting at the PCS/WIS:

    The receiver of the system under test is tested for conformance **by enabling the error counter on the receiving side**. As defined in section 49.2.12 and 50.3.8, the PCS or WIS is capable of detecting the data pattern and reporting any errors received.
  - The 10GBASE-R PCS can count errors in either “Pseudo-random pattern” (using PCS scrambling) or optionally PRBS31 (see 49.2.12). The test transmitter generates one of these patterns.
- No option for using an external error counter is suggested.



Relevant part of figure 52–10

Problem statement

- 100GBASE-SR4 uses Clause 82 100GBASE-R PCS, which can count errors only in the **scrambled-idle test pattern** – see 82.2.17
  - To provide the PCS with this pattern, the transmitter should use Test pattern 5 (RS-FEC encoded)
  - The scrambled idle test pattern is recovered by the RS-FEC decoder, **but in this process, most PMD errors are corrected**.

    ➔ PCS error counting and Test pattern 5 can't be used to measure the PMD BER, as defined in the current test.
- The optional PRBS31 error counting functionality has moved to the PMA (83.5.10)
  - PMA error counting can be used in 100GBASE-SR4, but needs an additional exception if clause 52 method is the reference procedure.

How did previous projects define SRS?

- Draft 2.0 defines SRS quite like 86.8.4.7 (which also refers to 52.9.9) – but for the PHYs defined in clause 86, no error correction is performed; thus, the scrambled idle pattern can be used with the PCS error counters.
  - For clause 86, if Pattern 3 is used, error counting should still be done in the PMA as an additional exception to clause 52, but this is a minor issue.
- In contrast, 87.8.11 does not refer to clause 52 at all, and defines SRS explicitly as a PMD test (at TP4; see figure 87-3). It doesn't specify how errors are counted (thus allowing using either PMA counters or an external device). Clause 88 refers to clause 87 method.
  - For clause 87, if Pattern 5 is used, error counting should be done by the PCS after reconstructing 66-bit blocks across the lanes; this is suitable for an attached PCS, but using an external device is complex and unlikely.

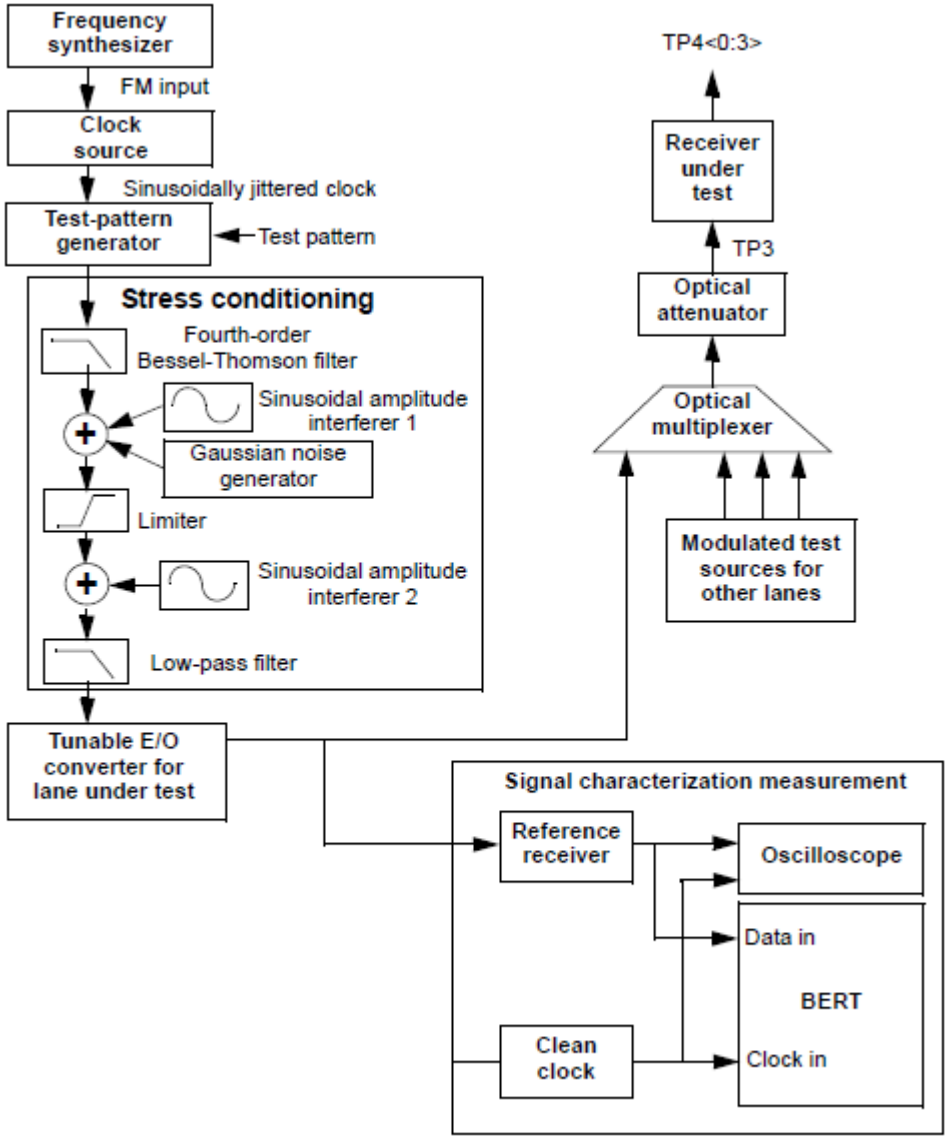


Figure 87–3—Stressed receiver conformance test block diagram

TDP measurement

- TDP measurement is also specified to use either Pattern 3 or Pattern 5.
- Subclause 95.8.1.1 addresses TDP as follows:

  To allow TDP measurement with Pattern 5, unstressed lanes for the error detector may be created by setting the power at the reference receivers well above their sensitivities, or by copying the contents of the transmit lanes not under BER test to the error detector by other means.
- Error detection and counting (required for TDP) with Pattern 5 requires a **four-lane BERT with RS-FEC and PCS decoding capability**. This is not standard equipment and isn't likely to be widely available.
- TDP with Pattern 5 does not provide any additional accuracy compared to pattern 3.

Comment #87 against D2.0

- The comment noted the problems listed above and suggested a remedy (see backup) for using Pattern 5 in SRS, and a clarification for using Pattern 5 in TDP.
- The response stated that "**A stand-alone pattern generator and error counter could be used**". However…
  - While a stand-alone error counter could be a fine way for SRS testing, it is not allowed by the text in 52.9.9.
  - Availability of stand-alone error counters capable of handling Pattern 5 is questionable.
- Specifying multiple test methods which are quite different, for measuring the same parameter, may cause ambiguity. Why not specify only the simplest one?

Possible remedies for SRS

We can go in one of two different paths:

1. Treat SRS as a full receiver test (including PMD, PMA and RS-FEC).
   - This is similar to the approach taken in 802.3bj for clauses 92, 93, 94.
   - Error counting can be done by the RS-FEC. This requires transmitting Pattern 5 or valid 100GBASE-SR4 data (but not Pattern 3).
   - This was the suggested remedy for comment #87.
2. Change to treat SRS as a PMD test excluding the RS-FEC.
   - Specify BER at the PMD service interface, as done in clause 87.
   - In practice, a module can be tested separately from the host (e.g. with an MCB and a BERT) or with the host (using PMA counters)
   - Pattern 3 must be used for PMA counting. Using pattern 5 requires RS-FEC and PCS decoding, and makes the test more complex.

Each path has only one suitable pattern!

Proposal

- In Table 95-10, specify using Pattern 3 for SRS and for TDP.
- In 95.8.8, remove the reference to clause 52. Instead, refer to the method defined in 87.8.11 (or its relevant subclauses), with exceptions if necessary.
  - This enables using either PMA or external error counting.
- Delete the beginning of the second paragraph of 95.8.1.1 (Multi-lane testing considerations), as shown in the next slide.

~~Measurements with Pattern 3 (PRBS31) allow lane-by-lane BER measurements. Measurements with Pattern 5 (RS-FEC encoded scrambled idle) give the interface BER if all lanes are stressed at the same time. If each lane is stressed in turn, the BER is diluted by the three unstressed lanes, and the BER for that stressed lane alone must be found, e.g., by multiplying by four if the unstressed lanes have low BER. To allow TDP measurement with Pattern 5, unstressed lanes for the error detector may be created by setting the power at the reference receivers well above their sensitivities, or by copying the contents of the transmit lanes not under BER test to the error detector by other means.~~ In stressed receiver sensitivity and receiver jitter tolerance measurements, unstressed lanes may be created by setting the power at the receiver under test well above its sensitivity and/or not stressing those lanes with ISI and jitter, or by other means. Each receive lane is stressed in turn while all are operated. All aggressor lanes are operated as specified. To find the interface BER, the BERs of all the lanes when stressed are averaged.

Most of this paragraph deals with implications of using Pattern 5 and is not required if only Pattern 3 is specified. The fact that Pattern 3 allows lane-by-lane BER measurements is obvious and doesn't need to be mentioned.

Backup

Cl 95	*SC* 95.8.1.1	*P* 105	*L* 29	# 87

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Comment Type TR *Comment Status* R

For the receiver tests, according to 52.9.9.1: The receiver of the system under test is tested for conformance by enabling the error counter on the receiving side.

For pattern 5 (RS-FEC encoded scrambled idle), the adequate error counters are in the RS-FEC sublayer, since errors are corrected before being delivered to the PCS. RS-FEC error counters are per lane so this allows lane-by-lane measurement just as in pattern 3. It can also work with any valid RS-FEC encoded 100GBASE-R signal.

It should be noted that the RS-FEC error counters count 10-bit symbol errors, while the specification in 95.1.1 is for bit errors. Since the counts are expected to be the same (assuming bit errors are independent), the per-lane symbol error counters should be used to measure the lane-by-lane BER.

It should also be noted that pattern 3 testing uses error counters at the PMA (85.3.10) - I couldn't find any reference to this in the text (receiver test methods refer to clause 52).

For the TDP test, using pattern 5 requires an error detector capable of decoding this pattern, which requires all lanes to be received in parallel. Assuming this is intended, it should be noted.

SuggestedRemedy

Change this paragraph to read:

Receiver BER measurements are performed on a lane-by-lane basis. Lanes can be stressed at the same time or separately. To find the interface BER, the BERs of all the lanes when stressed are averaged. All aggressor lanes are operated as specified.

If Pattern 3 is used, each lane can be tested separately, and BER is read from error counters at the PMA (85.3.10) when stress is applied. If Pattern 5 (RS-FEC encoded scrambled idle) or valid RS-FEC encoded 100GBASE-R signal is used, transmission is done on all lanes in parallel, and BER is read from the per-lane RS-FEC symbol error counters (91.6.10) when stress is applied. Bit error count is considered equal to RS-FEC symbol error count for the purpose of this measurement.

Add the following paragraph:

TDP measurement with Pattern 5 requires an error detector capable of receiving all lanes in parallel and decoding this pattern. To allow unstressed lanes for the error detector may be created by setting the power at the reference receivers well above their sensitivities, or by conveying the contents of the transmit lanes not under BER test to the error detector by other means.