CAUI-4 Chip to Chip and Chip to Module Applications

IEEE 802.3bm Task Force

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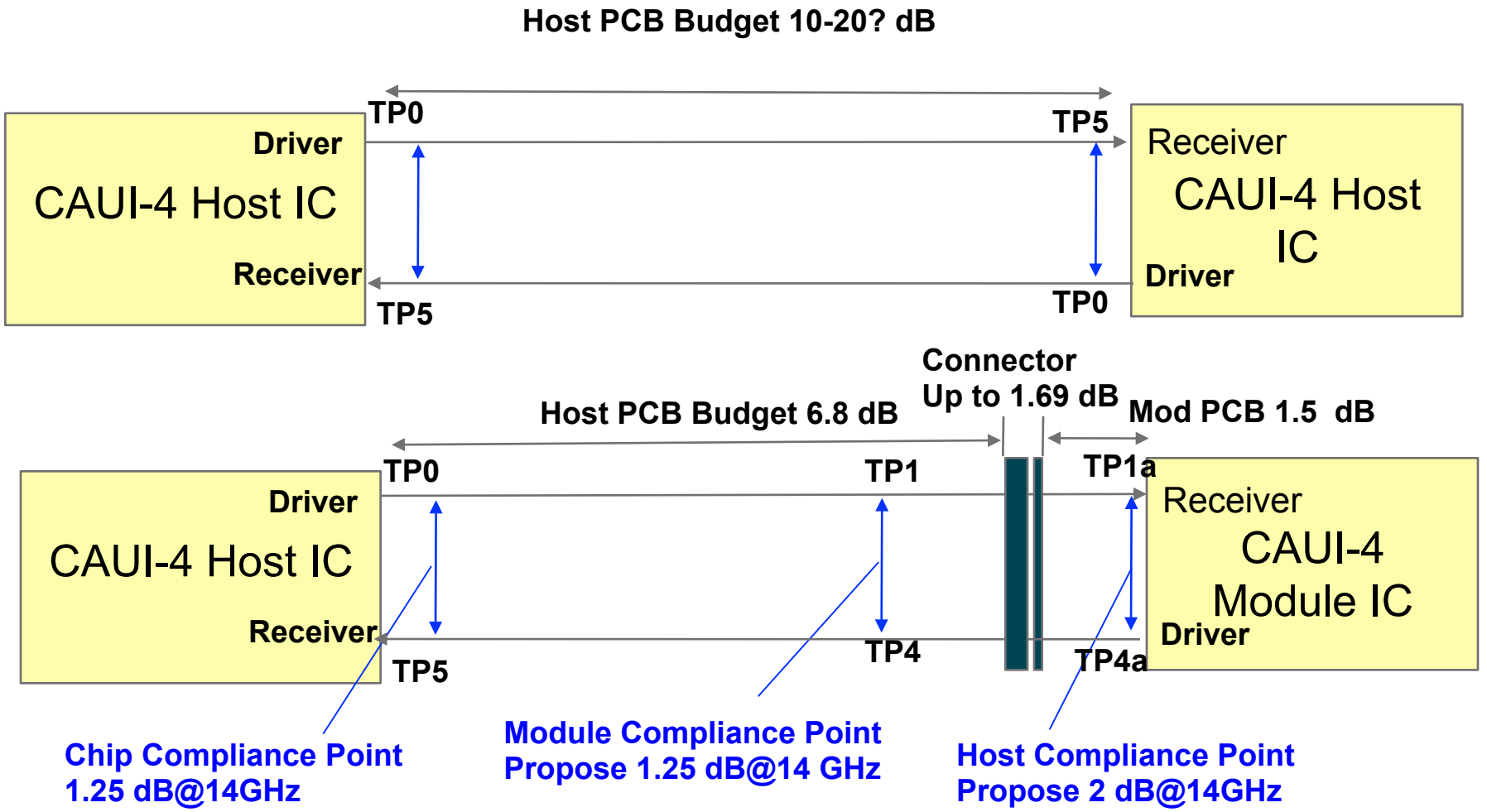
Overview

- CAUI-4 applications
- Implication and feasibility of higher loss budget CAUI-4
- As result of MTTFPA some of CAUI-4 options previously considered could result in undetected frame error http://www.ieee802.org/3/bj/public/may12/cideciyan_01_0512.pdf
  - Non-symmetrical link based on host with greater capability to deliver the required signal at TP1a and relying on host DFE receiver may not be an option
  - A simple interface based 4x25.78 Gbd with CTLE+1-3 tap DFE may not an option for 100Gbase-R
- If bj KR4 FEC capability is required to avoid MTTFPA, wouldn't be easier to just turn down bj KR4 capability over defining another CAUI-4 chip to chip

CAUI-4 Architecture and Reference Points

- The bm group need to further study CAUI-4 chip to chip application
  - Considering all the constrains, the 10 dB is the best choice for the chip to module

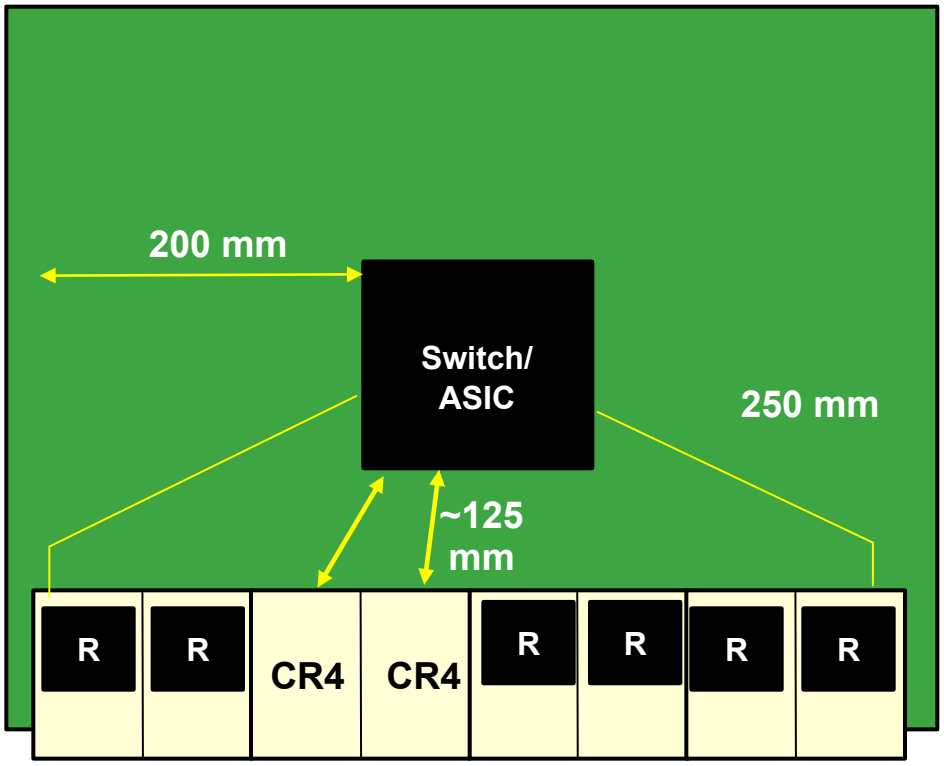


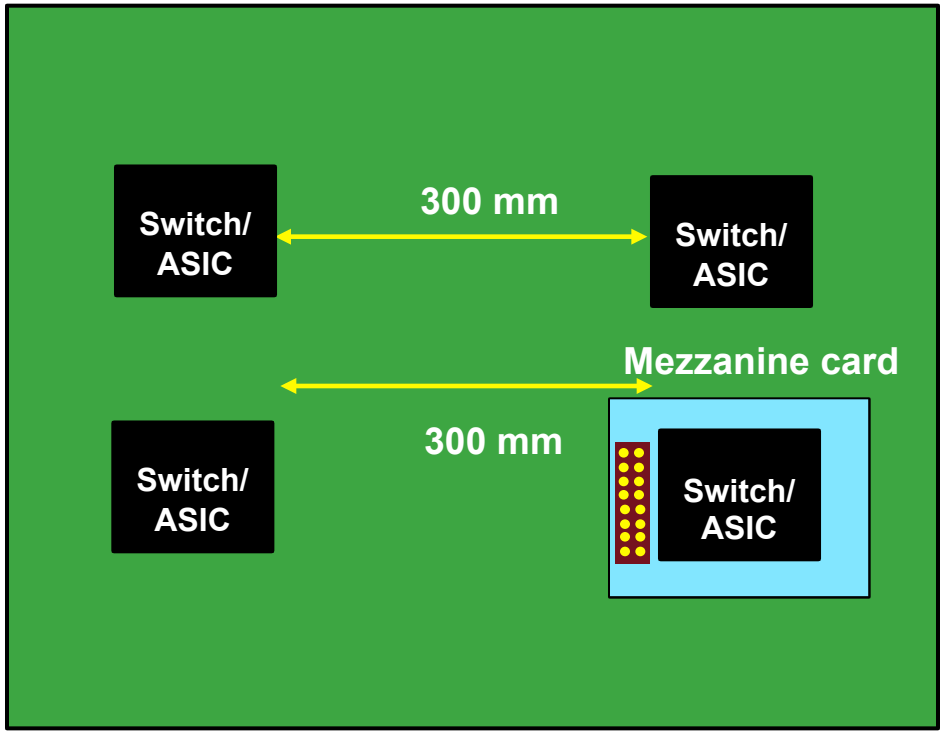
CAUI-4 Reality Check 4 Month Later

- Mr. Latchman hosted several conference calls to study CAUI-4 solution for chip to module and chip to chip plus the commonality with CR4
  - The group consensus is in support of port commonality with CR4 with maximum chip to module channel loss of 10 dB
  - One may push the CAUI-4 loss budget by 2-3 dB assuming CTLE in the module but does not solve large ASIC driving 12-15” of PCB
  - ICN and return loss for some of the next generation connectors are not as good as early VSR connectors, the extra margin may quickly evaporate
  - There was also interest to define informative annex how to engineer the CAUI-4 chip to module for greater than 10 dB at expense of CR4 compatibility
- Previously it was identified the need to define chip to chip interface with 18-20 dB loss budget similar to OIF-28G-MR
  - The assumption was simple CTLE+1-3 tap DFE would be sufficient
  - However as result of 100GBase-R PCS carried over 4 lanes with a DFE receiver can result 4 or more errors, where CRC can not protect and resulting in MTTFPA

CAUI-4 Applications and Background

- http://www.ieee802.org/3/bj/public/jul12/ghiasi_02a_0712.pdf identified CAUI-4 applications as well as limitations
  - As result of MTTFPA, non-symmetrical interface is not an option unless module retiemr has FEC capability
  - Supporting 300 mm link require SerDes with bj KR4 capability
  - Is it really worth defining bj-KR4 link with 20 dB loss budget?





PCB Reach for Various Interfaces

- PCB loss estimate assumptions and tools for calculation
  - IEEE 803.bj spreadsheet http://www.ieee802.org/3/bj/public/tools/DkDf_AlgebraicModel_v2.02a.xlsm for N4000-13SI and Megtron-6 calculation
  - Rogers Corp impedance calculator (free download but require registration) https://www.rogerscorp.com/acm/technology/index.aspx for FR4-6 and N4000-13
  - Stripline ~ 50 Ω, trace width is 5 mils, and with ½ oz Cu
  - Surface roughness med per IEEE spreadsheet or 2.8 um RMS
  - FR4-6 DK=4.2 and DF=0.02, N4000-13 DK=3.6 and DF=0.014, N4000-13SI and Meg-6 per IEEE spreadsheet

Host Trace Length (in)	Total Loss (dB)	Host Loss(dB)	FR4-6	N4000-13	N4000-13SI	Megtron 6
Nominal PCB Loss/in at 5.15 GHz	N/A	N/A	1.00	0.79	0.56	0.43
Nominal PCB Loss/in at 12.89 GHz	N/A	N/A	2.00	1.60	1.25	0.92
CAUI Classic	10.5	6.81	6.8	8.6	12.2	15.8
PPI CL85A/86A with one connector & HCB#	6.5	4.37	4.4	5.5	7.8	10.2
CAUI-4 with one connector & HCB*	10.5	6.81	3.4	4.3	5.4	7.4
802.3bj CL92A with one connector & HCB *	10.5	6.81	3.4	4.3	5.4	7.4
CAUI-4 Chip to Chip	10	10	5.0	6.3	8.0	10.9
CAUI-4 Chip to Chip Engineered	15	15	7.5	9.4	12.0	16.3
cPPI-4 #	7	3.8	1.9	2.4	3.0	4.1
OIF 28G-MR	20	20	10.0	12.5	16.0	21.7

Assumes connector loss is 0.87 dB and HCB loss is 1.26 dB at 5.5 GHz.

* Assumes connector loss is 1.69 dB and HCB loss is 2.0 dB at 12.89 GHz.

Option for Chip to Chip Interface

- CAUI-4 chip to module should be redefined at chip ball for chip to chip applications
  - With CAUI-4 chip to chip interface under control of single OEM, the interface could be engineered for possibly as much as 15 dB
  - A transmitter with faster rise time and lower jitter could be used to increase the loss budget
  - A receiver with higher sensitivity and CTLE peaking can extend PCB reach
  - A channel with lower ILD, ICN, and return loss could increase the loss budget
  - Engineering CTLE link to operate over 15 dB is not too difficult if one has control over TX, RX, and channel but rather difficult for the standard to define it
- Defining a 2nd CAUI chip to chip with 20 dB requiring all the provision of 802.3bj KR4 to avoid MTTFPA may defeat the original presumption of a simple low power interface
  - If the interface has all the provisions of KR4 interface but with loss budget of 20 dB then it would be simpler to turn off some of the KR4 SerDes capability instead of defining another interface!

Summary

- After detail study over course of several conference call the take away is that 10 dB is the best choice for chip to module among number of other choice less attractive and loss of compatibility with CR4
- One could argue CAUI-4 with CTLE could support 12-15 dB loss budget
  - With some of the next generation 28G connectors having ICN in excess of 5 mV RMS, it is risky to push the CTLE to 15 dB
  - Higher loss budget chip to chip/module should be left as engineered solution and perhaps some guideline could be provided in an informative annex
- After the group arrived at consensous that 10 dB is the right choice, there was still support for defining a 2nd chip to chip with loss of 20 dB
  - Now that is clear we need bj KR4 port capability to avoid MTTFPA it is not clear if it worth defining bj-KR4 port with 20 dB loss over just turning off some of the bj-KR4 port capability
  - There may still be need for higher than 10 dB loss budget without the use of bj-KR4 these could be supported via engineered link
  - An OEM having control on both end of the link potentially could engineer these link where the standard can't define the same link.

Thank You