Implementation tradeoffs for WDM4 PMD in relation to cost

Contributors

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Introduction

- One of P802.3bm adopted objectives :
  “Define a 100 Gb/s PHY for operation up to at least 500 m of SMF”

- WDM PMD has been proposed as cost-effective solution
  vlasov_01_0312_NG100GOPTX.pdf
  vlasov_01_1112_optx.pdf

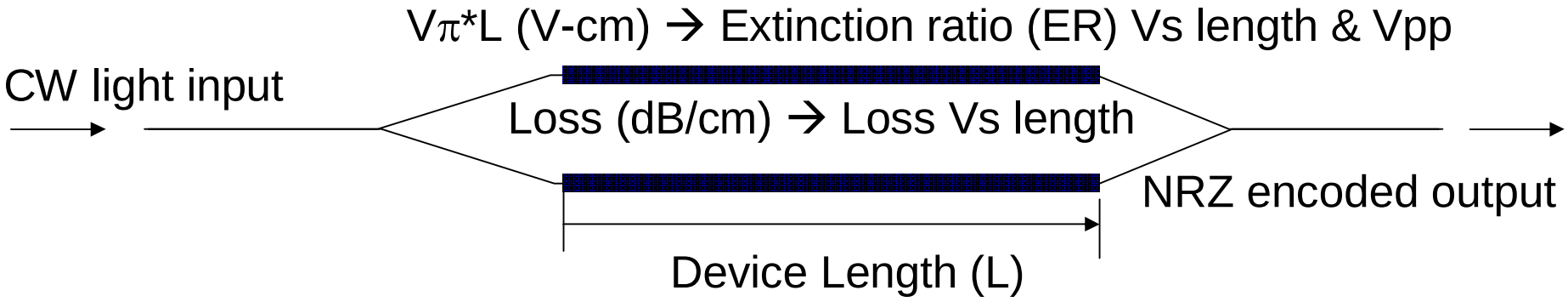
- Impact of extinction ratio and drive voltage on silicon MZI modulator insertion loss is presented

- Impact of WDM grid on laser cost is considered

Silicon photonics MZI modulator fundamental tradeoffs

Impact on link budget/cost

CMOS Mach-Zender Interferometric (MZI) Transmitter



- Two Modulator Figures of Merit (FOM) used today
  - FOM_1 = Vπ*L (V-cm) → Extinction ratio (ER) Vs length → Modulation Penalty
  - FOM_2 = Loss (dB/cm) → Gives loss Vs length → Loss Link Penalty

Using two figures of merits makes it difficult to understand transmitter impact on link penalty*

* D.M. Gill, *et. al*, A Figure of Merit Based Transmitter Link Penalty Calculation for CMOS-Compatible Plasma-Dispersion Electro-Optic Mach-Zehnder Modulators, http://arxiv.org/ftp/arxiv/papers/1211/1211.2419.pdf

CMOS MZI Modulator Loss Vs ER & Drive Voltage (Vpp)

Fundamental trade-offs for silicon MZI modulator

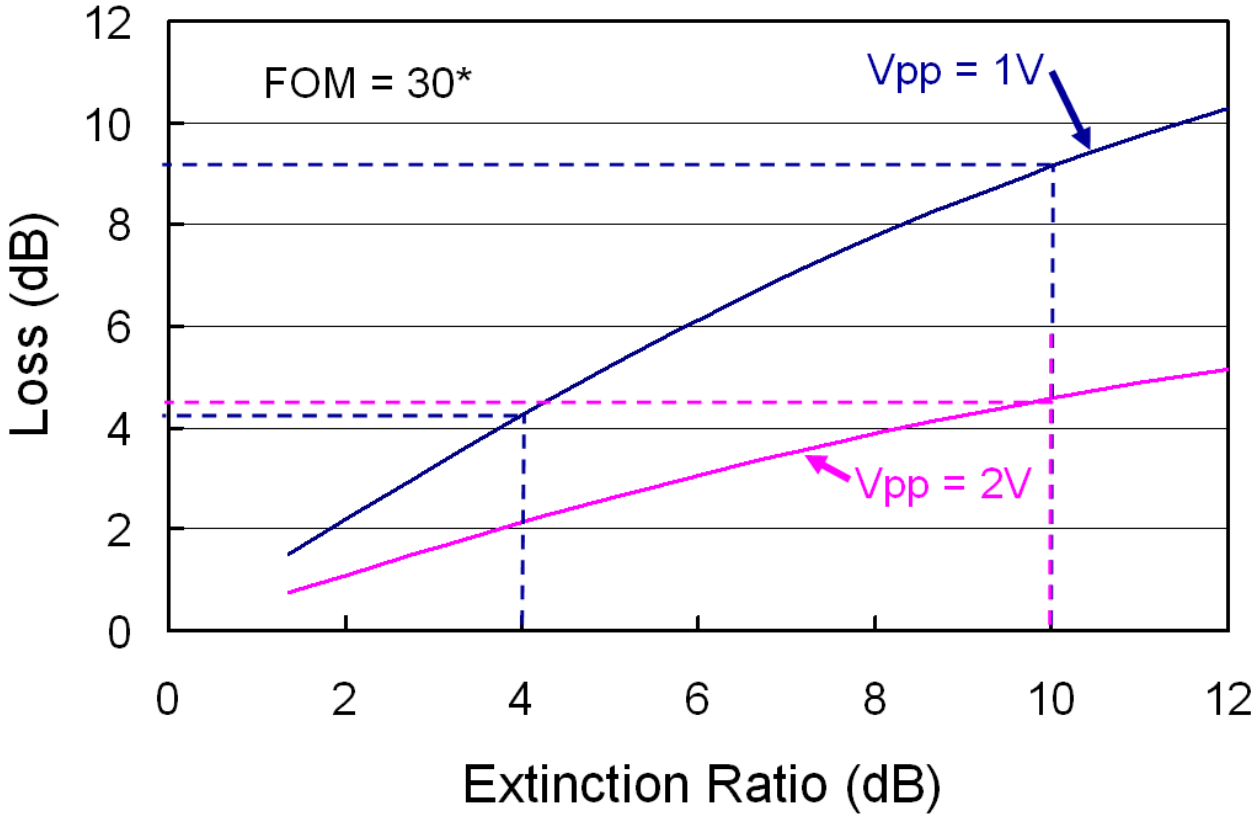
Loss ⟷ ER ⟷ Vpp drive

FOM=$V\pi L \cdot \alpha$

$V\pi L$ = 1V•cm

α= 30dB/cm

FOM = 30 V•dB



Example for silicon MZI with FOM=30 V•dB and ER=10dB:

1Vpp driving voltage directly from CMOS → 9dB insertion loss

* See also backup slides. Reference: D.M. Gill, *et. al*, A Figure of Merit Based Transmitter Link Penalty Calculation for CMOS-Compatible Plasma-Dispersion Electro-Optic Mach-Zehnder Modulators, http://arxiv.org/ftp/arxiv/papers/1211/1211.2419.pdf

Impact on link budget and/or cost

Fundamental trade-offs

Loss ⟷ ER ⟷ Vpp drive

Extinction Ratio	Peak-to-Peak Drive Voltage	Optical Loss
4 dB	1 Vpp	4.3 dB
10 dB	1 Vpp	9.2 dB
10 dB	2 Vpp	4.5 dB

ER=4dB → modest 4.3dB insertion loss at 1Vpp

- silicon MZI that can be driven directly from CMOS driver

ER=10dB → high 9.2dB insertion loss at 1Vpp

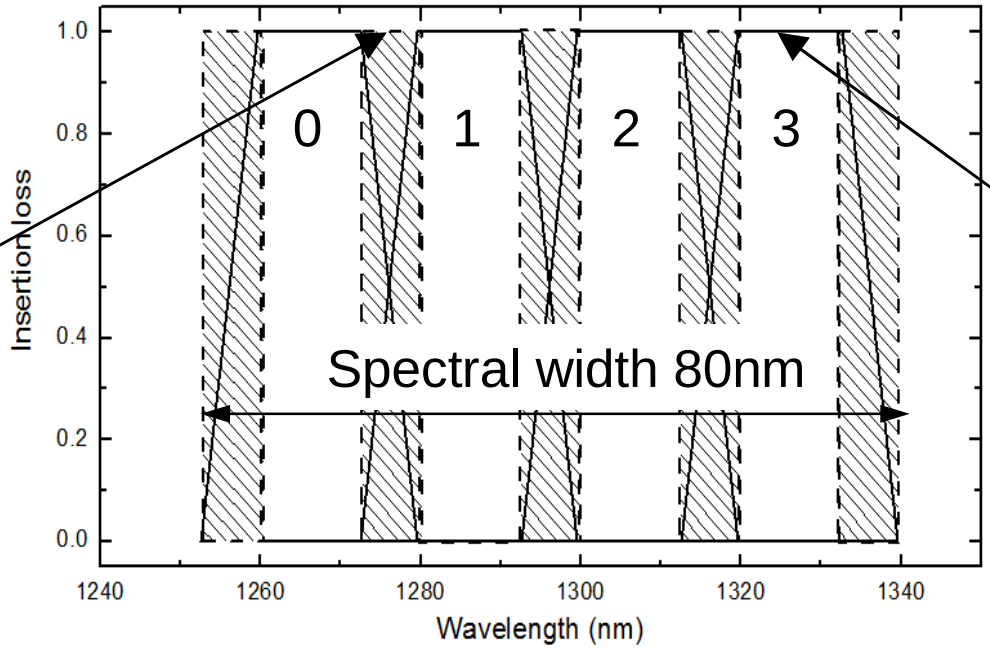
- high power laser to compensate for high loss → high laser cost
- SiGe driver to increase the driving voltage → high packaging cost

Conclusion:

For WDM4 PMD the ER=4dB is chosen to reduce the cost

Choice of grid for 100GbE 2km WDM4 PMD

ITU G694.2 CWDM grid for 100GbE 2km PMD



Guard band 7nm

Channel width 13nm

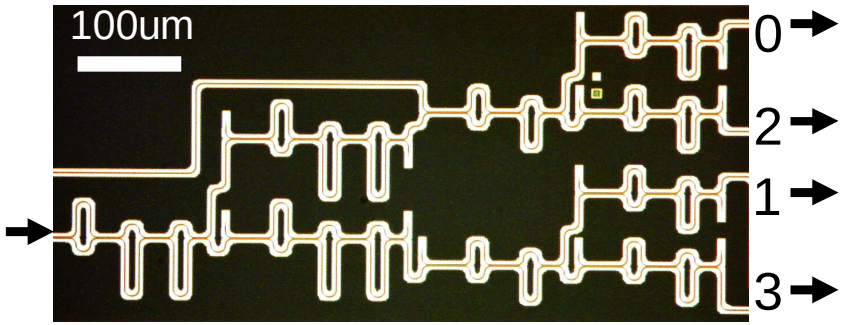
- LAN WDM requires active wavelength locking and tracking
- CWDM is OK
  - → 100% laser yield, no wavelength testing
  - → Up to 130ºC can be accommodated
- However 80nm spectral width of ITU G694.2CWDM is not optimal:
  - → Laser gain spectral width is not easy to achieve
  - → Larger variations of slope efficiency and output power

Resemble 4-year old discussions: traverso_01_0108.pdf, traverso_01_0308.pdf, cole_01_0308.pdf

Feasibility: CMOS WDM - no add-on cost solution

- No additional mask levels
- No additional processing
- Designed for high yield
- No post-processing trimming required
- Footprint 0.6x0.3mm^2

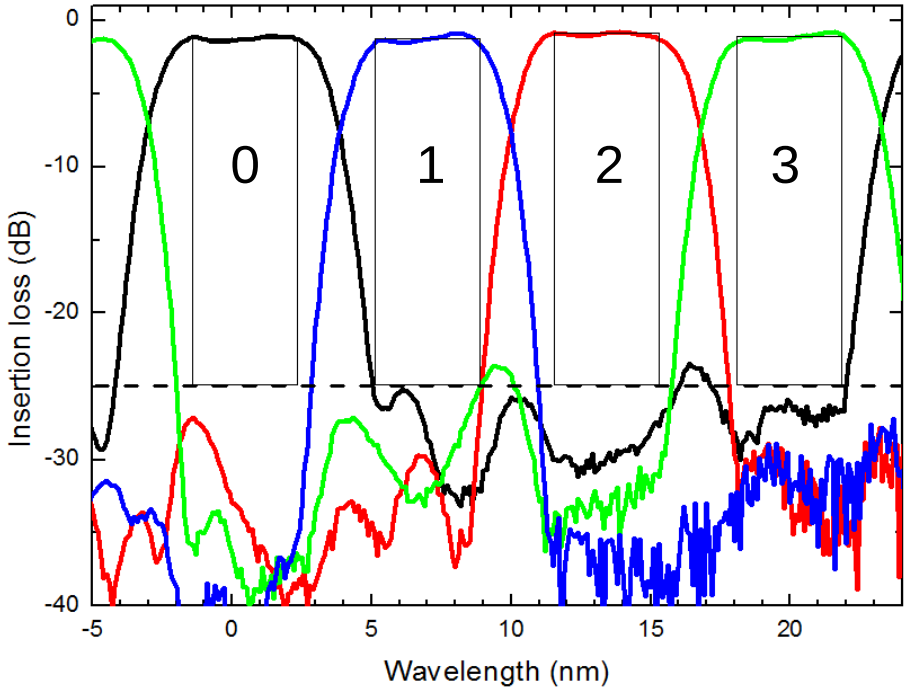
Die photo of cascaded 4-stage MZI filter



Design and test by Folkert Horst, IBM Zurich

Verified design:

Grid (nm)	6.5
Width (nm)	3.8
Guard band (nm)	2.7
Crosstalk	<-25dB
Insertion loss	<1dB
In-band ripple	<1dB

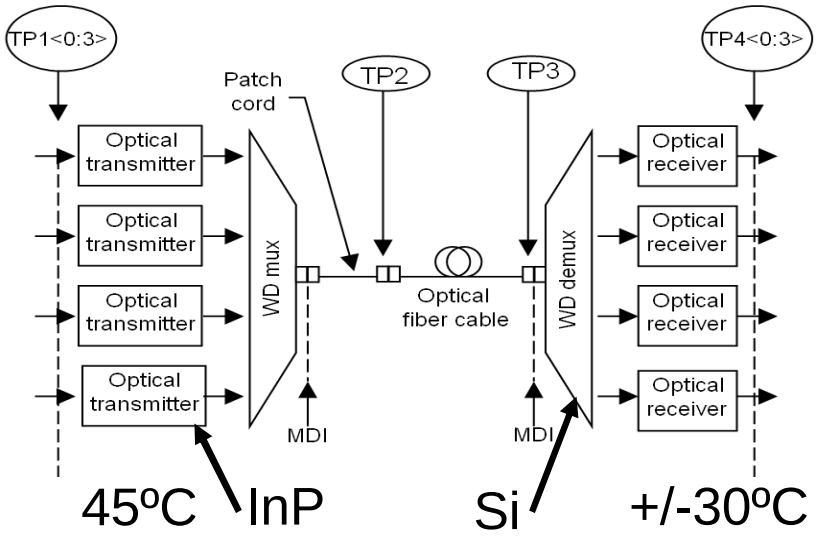


Technical feasibility:

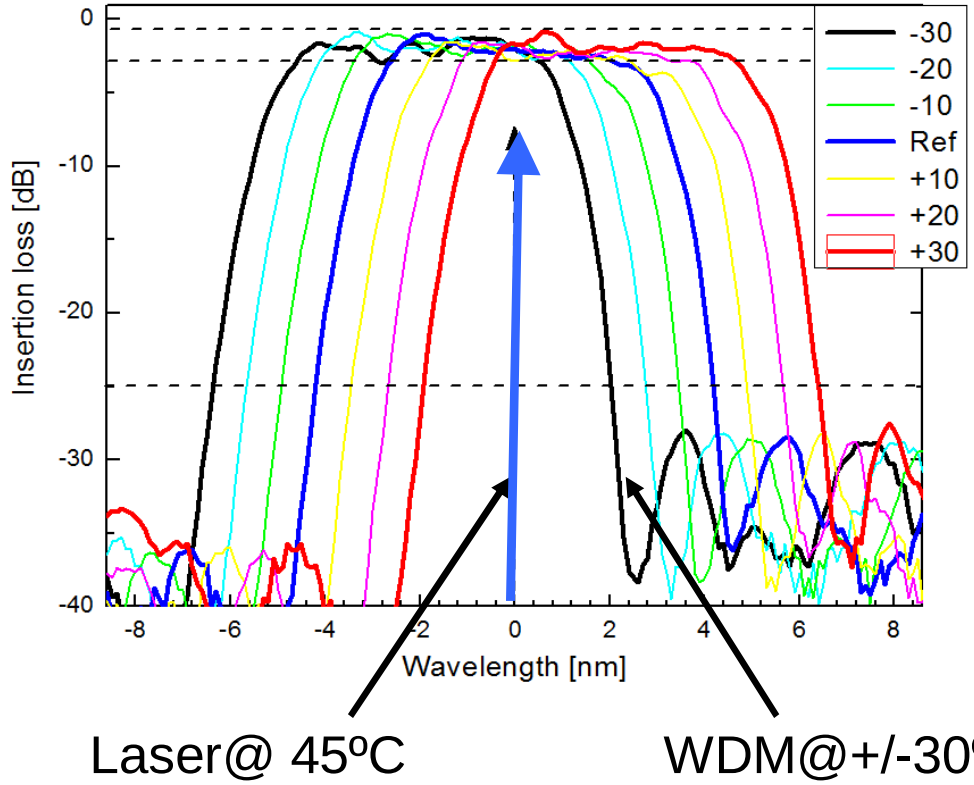
Occupies only 40% of total CWDM spectral width

S.Assefa et al, IEDM 2012

Feasibility: CMOS WDM - temperature tolerance



Design and test by Folkert Horst, IBM Zurich



Technical feasibility:

Less than -25dB xtalk is maintained over 60ºC swing

Less than 2dB channel insertion loss penalty over 60ºC swing

If both TP1 and TP2 are not temperature stabilized

Current WDM design can provide operation 30ºC to 60ºC

Considerations for optimized WDM grid

WDM grid ←→Total spectral width ←→ Laser cost ←→ Temperature control

For operation within 0ºC to 70ºC range maximal temperature spectral shift of 12nm is expected – consistent with ITU G694.2 CWDM grid

Possible approaches for smaller total spectral width:

- ✓ WDM filters with steeper roll-offs – reduction of guard band width
- ✓ Local WDM heating – much more cost efficient solution than TEC
  - Active feedback electronic loops in the microcontroller
  - Microcontroller does not require high-end silicon (1000s gates)
- ✓ Temperature tolerant designs of silicon WDM filters

Conclusion: further consideration of balance between laser cost vs WDM design is justified

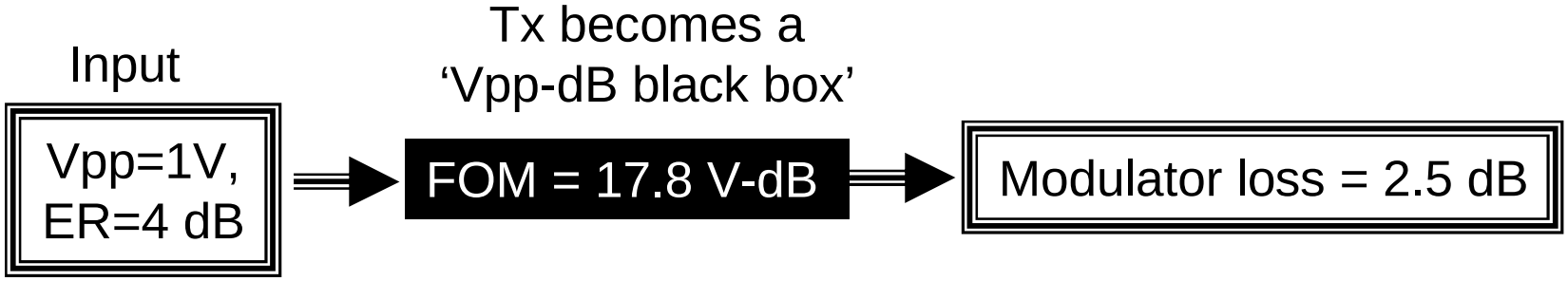
Summary

- Analysis of insertion loss of silicon MZI impact on link budget, driving voltage and cost is presented
  - Fundamental tradeoff between ER, loss and drive voltage is characteristic for silicon MZI modulators
  - It has direct impact on modulator insertion loss and link budget
  - ER=4dB is compatible with silicon MZI driven with 1Vpp CMOS driver
  - ER=10dB creates much higher loss that can be mitigated with 2Vpp driver or higher power laser to compensate for large insertion loss
- Consideration of impact of the wavelength grid on optimization of laser cost is presented
  - ITU G694.2 CWDM grid is acceptable for WDM4 PMD
  - Better laser yield could be achieved by optimizing the WDM grid
- Technical feasibility of a temperature-tolerant silicon WDM filter is verified

Backup

CMOS MZI Transmitter FOM

- Define new CMOS Modulator FOM
  - $FOM_{IBM} = FOM_1 * FOM_2 = (V\pi * L) * (Loss) = (Vpp\text{-}dB)$
  - Easily gives loss Vs. ER and drive Vpp, Loss = (FOM/Vpp)*(phase shift/π)
  - Removes device length from consideration and provides loss as a function of Vpp and required ER.
    - Note that changes in Tx bandwidth versus device length and not considered
  - Loss and ER then easily translated into Tx link penalty



CMOS MZI creates optical loss that needs to be included in link budget

* D.M. Gill, *et. al*, A Figure of Merit Based Transmitter Link Penalty Calculation for CMOS-Compatible Plasma-Dispersion Electro-Optic Mach-Zehnder Modulators, http://arxiv.org/ftp/arxiv/papers/1211/1211.2419.pdf

FOM allows Comparison of published modulator designs

Comparison of published modulator designs with our FOM

Loss (dB/cm)	Vπ*L (V-cm)	FOM (V-dB)	Ref
10.7	1.6	17.1	1
16.7	1.2	20.7	2
31.8	0.8	25.4	3
15.0	1.9	27.9	4
31.0	1.0	31.0	5
70.0	0.5	35.0	6

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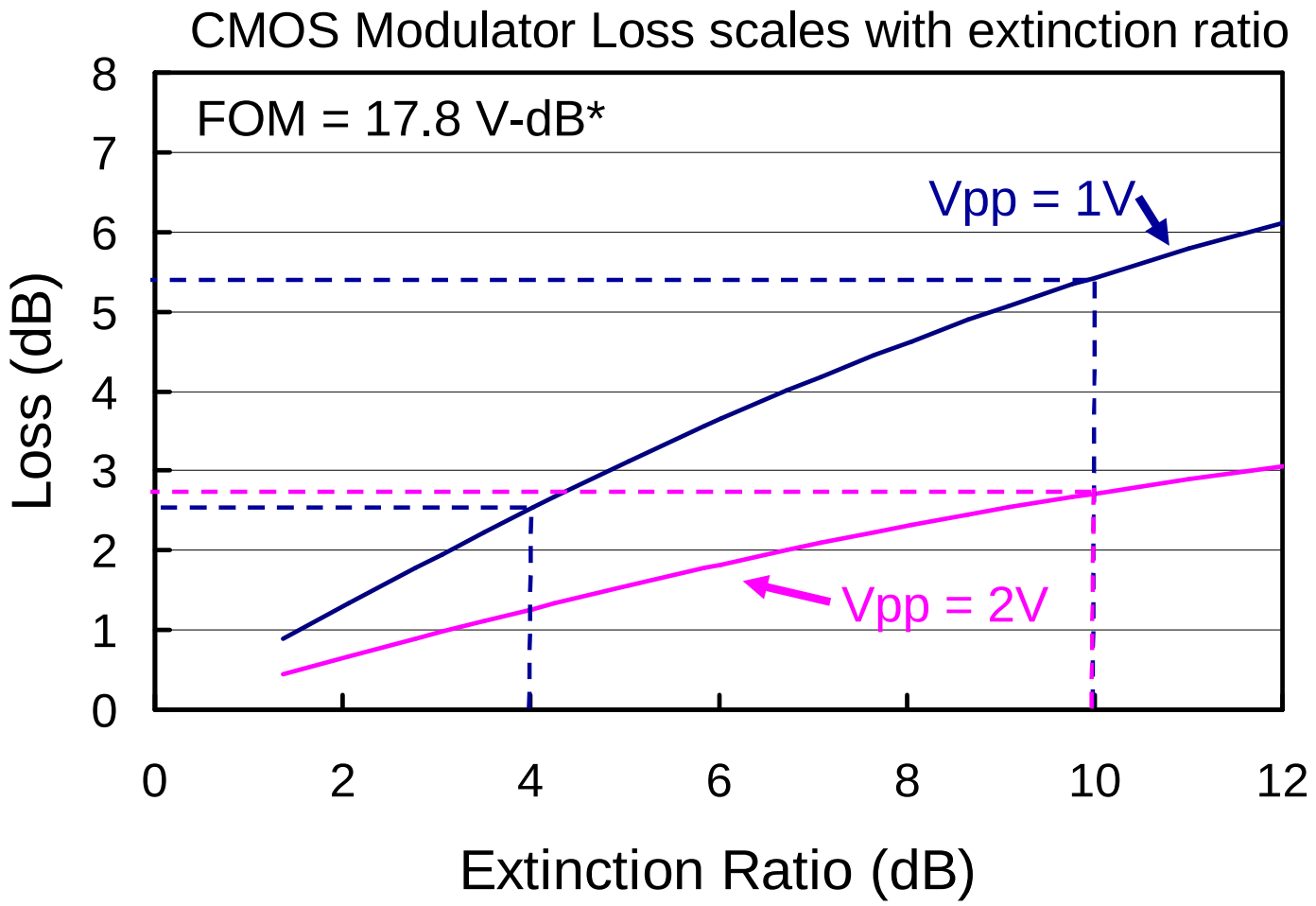
Lower FOM gives lower link penalty

References

(1) D.M. Gill, *et. al*, http://arxiv.org/ftp/arxiv/papers/1211/1211.2419.pdf
(2) X. Xiao, *et. al*, Opt. Express **20**, 2507-2515 (2012).
(3) J. Rosenberg, *et. al*, Opt. Express **20**, 2507-2515 (2012).
(4) P. Dong, *et. al*., Opt. Express **20**, 6163-6169 (2012).
(5) M. R. Watts *et al.*, JST Quantum Electron. **16**, 159 (2010).
(6) Junichi, *et al.*, paper OMI3, OFC (2010).

CMOS Modulator Loss Vs Extinction Ratio



4 dB ER, 1 Vpp → 2.5 dB loss
10 dB ER, 1 Vpp → 5.5 dB loss
10 dB ER, 2 Vpp → 2.75 dB loss

Proposed FOM allows impact of different modulator and driver technologies to be easily compared

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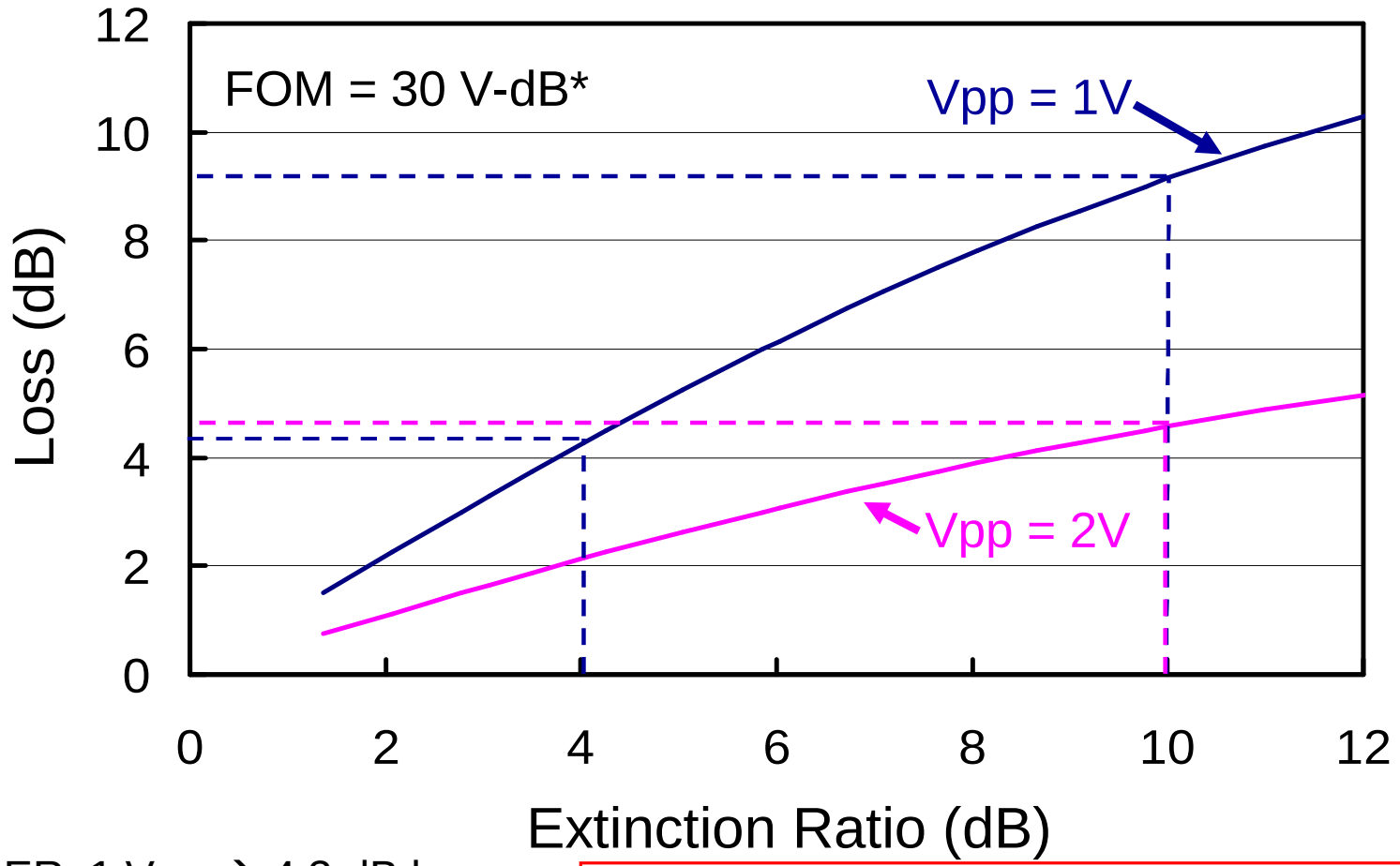
CMOS Modulator Loss Vs Extinction Ratio



4 dB ER, 1 Vpp → 4.3 dB loss
10 dB ER, 1 Vpp → 9.2 dB loss
10 dB ER, 2 Vpp → 4.6 dB loss

Proposed FOM allows impact of different modulator and driver technologies to be easily compared

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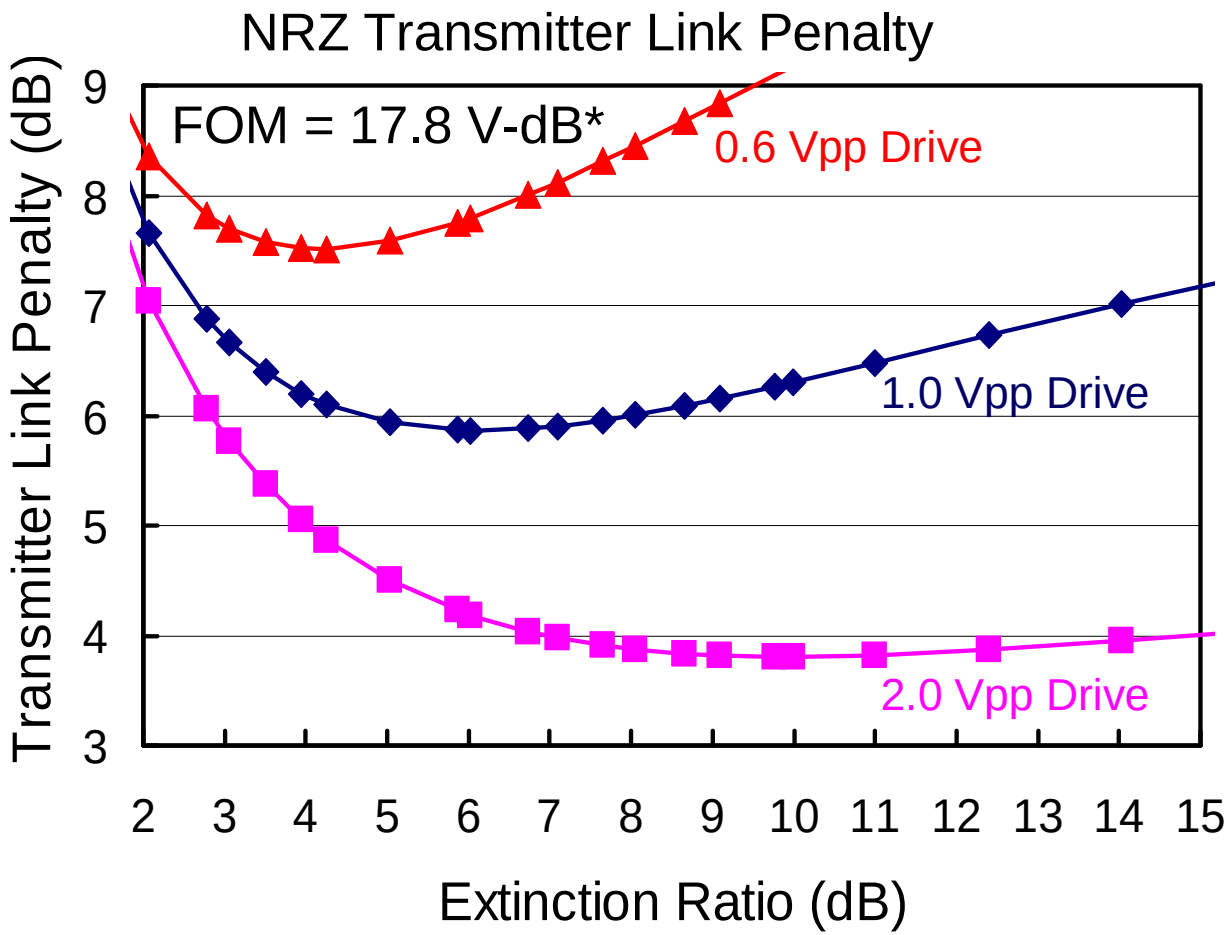
CMOS MZI Link Penalty Vs Drive Voltage



NRZ Modulation Penalty

$$= 10Log_{10}[(10^{\frac{ER}{10}} - 1)/(10^{\frac{ER}{10}} + 1)]$$

MZI loss

(FOM/Vpp)*(phase shift/π)

Transmitter Link Penalty = {NRZ Modulation Penalty} + {MZI loss}

MZI OMA does not change much between 4 dB and 10 dB ER.

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