CAUI-4 Chip – Chip Spec Discussion

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Chip-Chip Considerations

- Target: low power, simple chip-chip specification to allow communication over TBD loss with one connector
  - Similar to Annex 83A in 802.3ba
    - 25cm or ~10 inches over PCB
    - If we apply 1.7dB loss / inch at 14GHz we get 17dB + Connector (~1dB)
      - Meg6_HighSR-Narrow (kochuparambil_01_0112)
  - Compare to OIF SR / MR
    - SR: 15.4dB
    - MR: ~20dB
  - ghiasi_02_0912_optx mentions 30cm
    - 18-20dB loss budget
- Potential differences with KR4:
  - Lower loss budget supports lower power, smaller receiver design
  - Reduced latency & complexity
    - No FEC
    - No in-band transmitter training
      - Adaptive Rx (SFP+)
      - Assume “system management”
      - Spec similar to 802.3ba CAUI

Interface Discussion & Implications

- Chip-Chip
  - If loss is kept to <20dB, there are potential implementations which avoid MTTFPA issue
    - CTLE designs are able to support greater than 10dB
      - Previous discussions had ~15dB loss
      - VSR 28G has 100mVpp eye opening at 1E-15
    - 802.3bj KR4 test 1 and 2 targeting 10^{-12} with 16dB channel and high level of RMS broadband noise, 30dB with lower level of RMS broadband noise (without FEC)
      - High noise and high loss will be significantly relaxed for chip to chip

Table 93–7—Receiver interference tolerance parameters

Parameter	Test 1 values	Test 2 values	Test 3 values	Test 4 values	Units
Maximum BER without FEC	10^{-12}	10^{-12}	2×10^{-5}	2×10^{-5}	
Channel insertion loss at 12.89 GHz Real part of a_0, min.[a] Real part of a_1, min. Real part of a_2, min. Real part of a_4, min.	16 −0.1 -1.2×10^{-5} — -2.5×10^{-21}	30 −0.1 -1.2×10^{-5} — -3.5×10^{-21}	30 −0.1 -1.2×10^{-5} — -3.5×10^{-21}	35 −0.1 -1.2×10^{-5} — -5×10^{-21}	dB $Hz^{-1/2}$ Hz^{-1} Hz^{-2}
Applied peak-to-peak sinusoidal jitter[b]	0.115	0.115	0.115	0.115	UI
Applied peak-to-peak random jitter[c]	0.15	0.15	0.15	0.15	UI
Applied even-odd jitter	0.035	0.035	0.035	0.035	UI
Applied RMS broadband noise	10	2.8	6.3	3.2	mV

[a]For each test channel, a_0 is limited to a maximum value of 0.1 and a_1, a_2, and a_4 are limited to a maximum value of 0. There is no minimum value specified for a_2.
[b]The frequency of the sinusoid must be greater than 100 MHz.
[c]Random Jitter is specified at a BER of 10^{-12}.

CAUI-4 Chip-Chip transmitter considerations

	KR4 (D1.2, TP2)	MR	CAUI-4 Chip-Chip Potential
Signaling rate, per lane	25.78125+/-100ppm	19.6 – 28.05	25.78125+/-100ppm
Unit Interval	38.787879ps	35.65ps - 51ps	38.787879ps
Differential peak-to-peak output voltage (max) with Tx disabled	30mV		30mVppd
Common Mode Voltage (max)	1.9V	1.7V	1.9V
Common Mode Voltage (min)	0V	-0.1V	0V
Differential output return loss (min)	RL(f) >= - 10log10((449.7+f^2)/(3671+f^2))	A0 = -12 fo = 50MHz f1 = 4.4189 f2 = 25.78125 Slope = 12dB/dec	RL(f) >= - 10log10((449.7+f^2)/(3671+f^2)), 0.05<=f<=13GHz
Common mode output returnloss (min)	RL(f)>= 6dB, 0.05<=f<=13GHz	-6dB , f<10GHz -4dB, 10G<f<25.78125GHz	RL(f)>= 6dB, 0.05<=f<=13GHz
Common-mode AC output voltage (max,rms)	12mV	12mV	12mV
Amplitude peak-to-peak (max)	1200mV	1200mV	1200mV
Amplitude peak-to-peak (min)		800mV	800mV

CAUI-4 Chip-Chip transmitter considerations

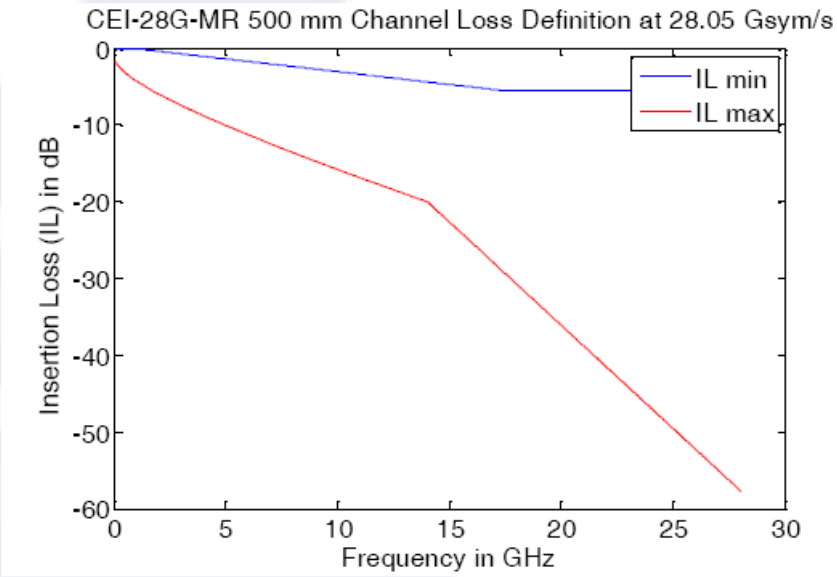
	KR4 (D1.2, TP2)	MR	CAUI-4 Chip-Chip Potential
Transmitter steady state voltage	0.4 (min) - 0.6V (max)		TBD
Linear fit pulse (min)	0.8 x Transmitter steady state voltage		TBD
Transmitted wave form Max RMS normalized error (linear fit), "e" abs coefficient step size (min.) abs coefficient step size (max.) Pre-cursor full-scale range (min.) Post-cursor full-scale range (min.)	 0.037 0.0083 0.05 1.54 4	C-1: -20 to 0 C1: -25 to 0 C0: 40 to 100 Step size: 1.25 to 5	TBD
Far end transmit output noise (max)	2mV (low loss channel) 1mV (high loss channel)		TBD
Output jitter (max)	Effective RJ: 0.15UI Even-odd jitter: 0.035UI TJ excluding DDJ: 0.28UI	TUUGJ = 0.15UIpp T_UBHPJ = 0.15UIpp T_DCD = 0.035UIpp TJ = 0.28UIpp	Effective RJ = 0.15UIpp Even-odd jitter = 0.035UIpp TJ = 0.28UIpp
Differential Resistance		80 ohms min, 100ohms typ, 120 ohms max	TBD
Transition time (min, 20/80%)	8ps	8ps	8ps

CAUI-4 Chip-Chip Receiver considerations

	KR4 (D1.2, TP2)	MR	CAUI-4 Chip-Chip Potential
Differential Input Return loss (min)	RL(f) >= - 10log10((449.7+f^2)/(3671+f^2))	A0 = -12 fo = 50MHz f1 = 4.4189 f2 = 25.78125 Slope = 12dB/dec	RL(f) >= - 10log10((449.7+f^2)/(3671+f^2)), 0.05<=f<=13GHz
Common mode input return loss (min)	RL(f) >=6dB, 0.05<=f<=13GHz	6dB , f<10GHz -4dB, 10G<f<25.78125GHz	RL(f) >=6dB, 0.05<=f<=13GHz
Differential to common-mode return loss (min)	TBD		TBD
Input Differential Voltage (max)		1200	1200mV
Differential Impedance		80ohms min, 100ohms typical, 120ohms max	TBD
Input Impedance Mismatch (max)		10%	TBD
Input common mode voltage		-200mV (min), 1800mV (max)	TBD

OIF MR ILmin/max

Channel ILmin and ILmax Graph



$$IL_{\max} = \begin{cases} 1.083 + 2.436\sqrt{\dfrac{f \times 28.05}{f_b}} + 0.698\dfrac{f \times 28.05}{f_b}, & f_{\min} \le f < \dfrac{f_b}{2} \\ -17.783 + 2.694\dfrac{f \times 28.05}{f_b}, & \dfrac{f_b}{2} \le f \le f_b \end{cases}$$

- IL_{max} (14.025 GHz) = -20 dB
- f_{min} = 50 MHz
- 19.90 <=f_b<=28.05 GHz

OIF MR fitted IL parameters

Parameter	Units	Value	
		Min	Max
Minimum Frequency	GHz	0.05	
Maximum Frequency	GHz		25.78
Fitted Insertion Loss At Nyquist	dB		20
Fitted Insertion loss a0	dB		2
Fitted insertion loss a1	dB		14.914
Fitted Insertion loss a2	dB		41.288
Fitted insertion loss a4	dB		19.728

OIF MR ICN

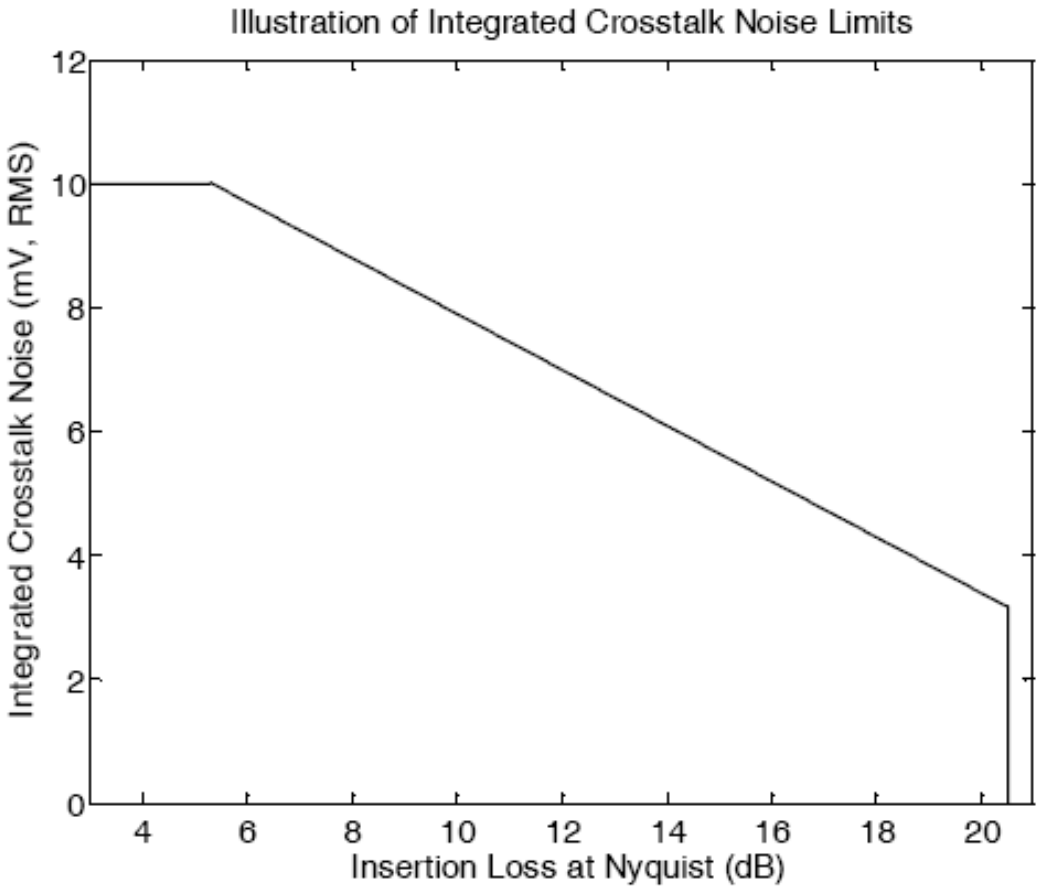


Illustration of Integrated Crosstalk Noise Limits
Integrated Crosstalk Noise (mV, RMS)
Insertion Loss at Nyquist (dB)
0
2
4
6
8
10
12
4
6
8
10
12
14
16
18
20

Receiver Interference Tolerance

Parameter	Test 1 values	Test 2 values
Maximum BER*	10^{-12}	10^{-12}
Channel Insertion Loss at 12.89GHz	TBD	TBD
Applied peak-to-peak sinusoidal jitter	TBD	TBD
Applied peak-to-peak random jitter	TBD	TBD
Applied even-odd jitter	TBD	TBD
Applied RMS broadband noise	TBD	TBD

* Maximum BER assumes errors are not correlated to ensure a sufficiently high mean time to false packet acceptance assuming 64b/66b coding. Actual implementation of the receiver is beyond the scope of the standard.

Compliance points

- **See 93.8.2.1 Receiver test fixture from 802.3bj**
- **See 93.8.1.1 Transmitter test fixture from 802.3bj**

Summary

- 802.3bm chip-to-chip has a significant amount of material that can be leveraged (802.3bj, OIF, etc)
  - Preliminary feedback from system vendors has been to leverage as much as possible
- CAUI-4 ad hoc group is collecting input to ensure appropriate application targets are met while achieving expected economies relative to 100GBASE-KR4
- Baseline focus areas include:
  - channel requirements
  - receiver interference tolerance
  - transmitter waveform specification
  - MTTFPA robustness