CAUI4 chip to chip applications

Tom Palkert, Xilinx
Mike Li, Altera
Ryan Latchman, Mindspeed
Nov. 6 2012

Agenda

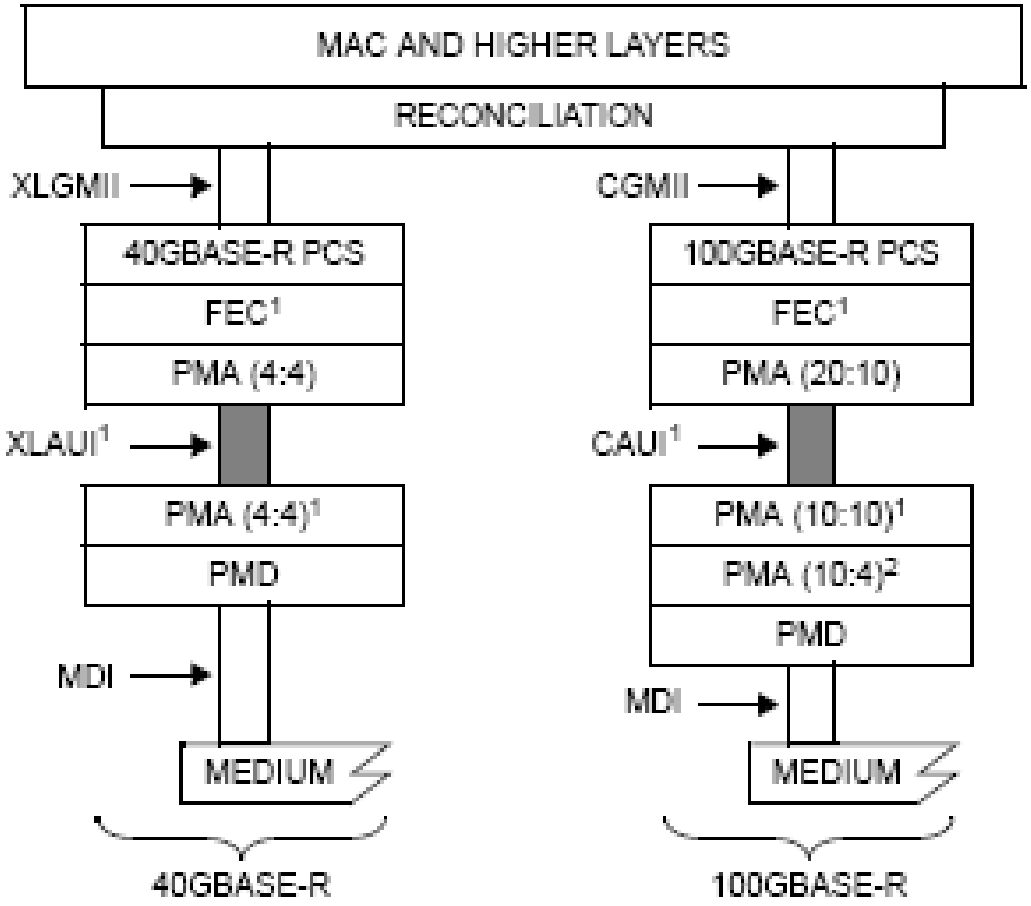
- Why do we need CAUI4 chip to chip?
- Applications
- Related standards work

Why do we need CAUI4 chip to chip?

- Precedence
  - We defined AUI interfaces for 10G Ethernet (4x3.125G XAUI), 40G Ethernet (4x10.3125G XLAUI), 100G Ethernet (10x10.3125G CAUI)
  - We need a chip to chip interface with longer distance/attenuation compared to CAUI4 chip to module.
    - System vendors have requested 20dB link budget

What were previous applications?

- XLAUI, CAUI

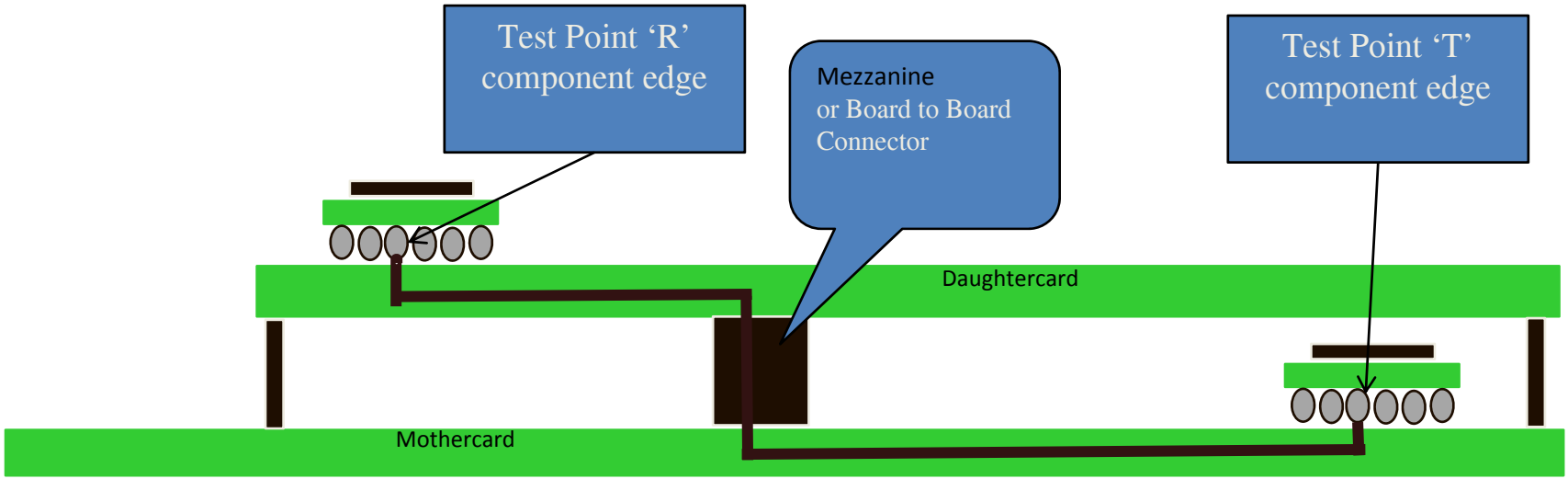


Target applications from 802.3ba

- XLAUI/CAUI chip to chip is needed to provide:
- a physical connection between a PMA and a PMA mapping element
- Lane extension for interfacing MAC and PHY components in an Ethernet system distributed across a circuit board

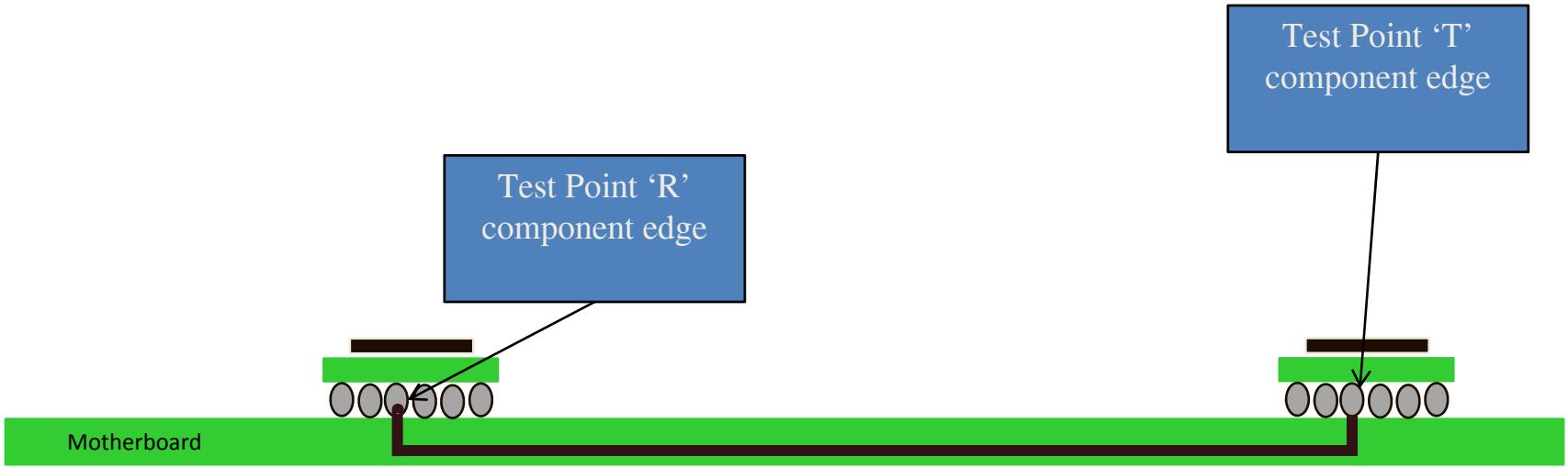
CAUI4 chip to chip applications

- Mezzanine card connections



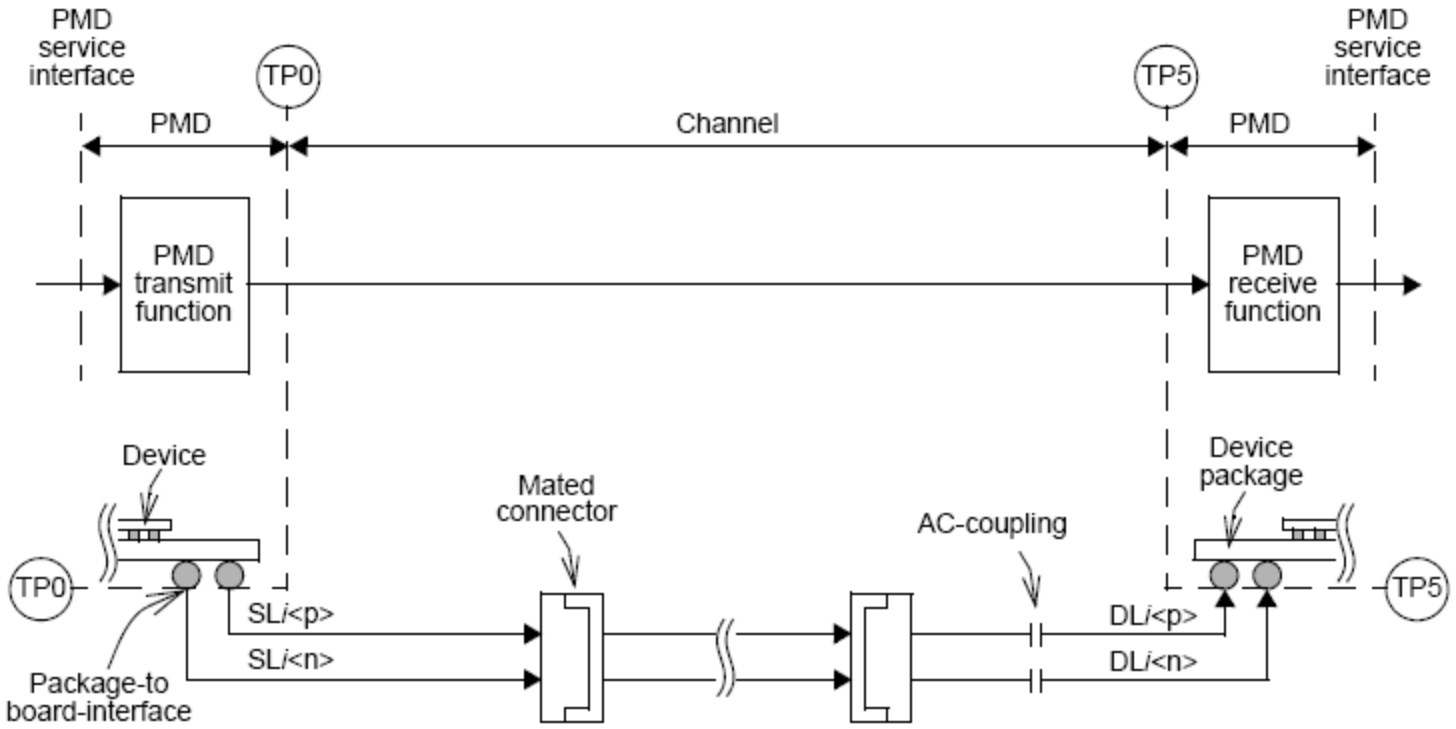
CAUI4 chip to chip applications

- Chip to chip connections on a motherboard



Proposed CAUI4 chip to chip compliance points

- We recommend we use the same compliance points as KR4



Proposed CAUI4 chip to chip interface characteristics (from appendix 83A)

- Independent transmit and receive data paths
- Differential AC coupled signaling with low voltage swing
- Self timed interface
- Shared technology with other 100Gb/s interfaces
- Utilization of 64B/66B coding

Channel insertion loss options

- CAUI was intended to support a point to point interface of up to approximately 25cm between integrated circuits using controlled impedance traces on low-cost circuit boards (PCBs). Longer reaches may be achieved by the use of better PCB materials, as the performance of an actual XLAUI/CAUI interconnect is highly dependent on the implementation

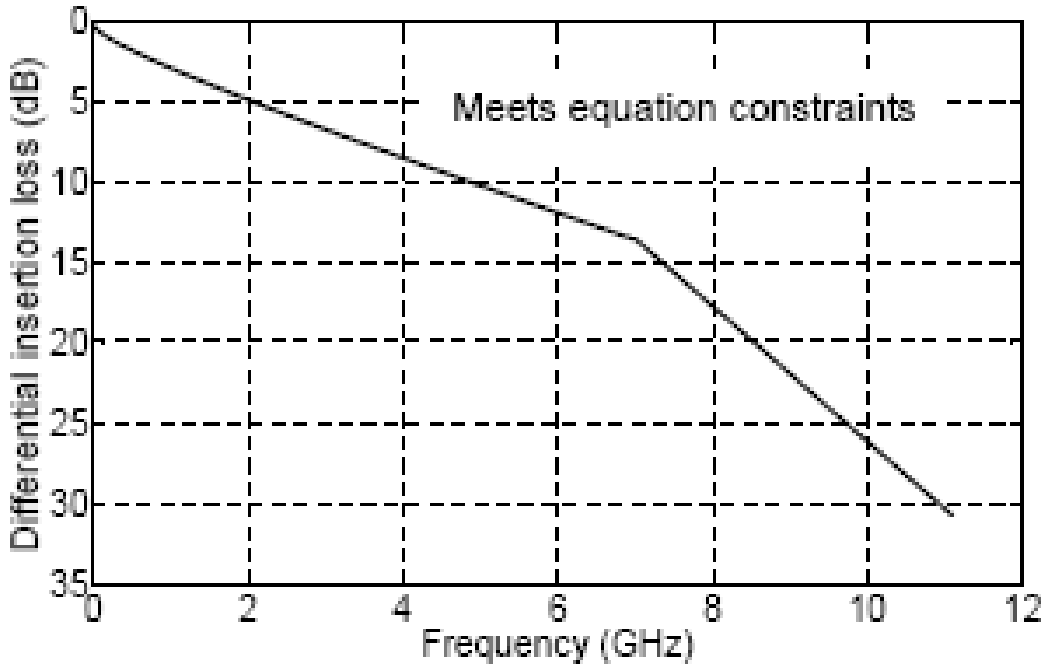


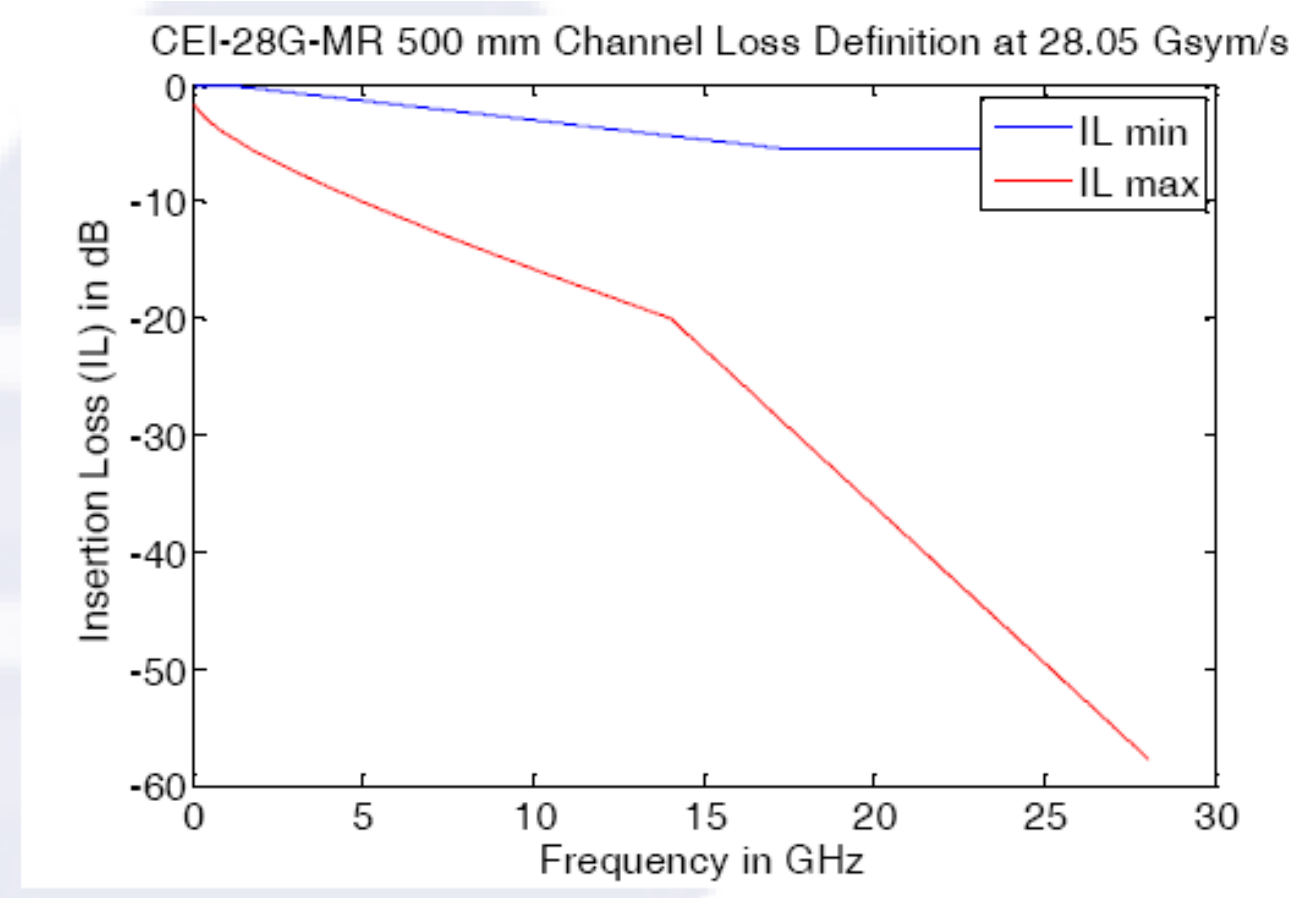
Figure 83A–13—Differential insertion loss

OIF CEI-28G-MR channel loss

Parameter	CEI-28G VSR	CEI-28G SR	CEI-28G MR	CEI-25G LR	IEEE 100GKR4
Speed range	19.9-28.05	19.9-28.05	19.9-28.05	19.9-25.08	25.8
BER Target	10^{-15}	10^{-15}	10^{-15}	10^{-15}	10^{-12}
Distance	150mm	300mm	500mm	686mm	1000mm
# Connectors	1	1	1	2	2
Insertion Loss	10dB	15dB	20dB	25dB	35dB
Signaling	NRZ	NRZ	NRZ	NRZ	NRZ

Channel insertion loss options

- CEI-28G-MR insertion loss curves



Recommendations

- We need a CAUI4 chip to chip interface
  - Necessary interface for IEEE stack
  - Not the same as:
    - CAUI4 chip to module (chip to chip needs to have higher loss)
    - KR4 (chip to chip should have lower loss, no FEC, no AN)
- Related work to consider:
  - OIF CEI-28G-MR (similar application, loss etc)
  - Infiniband EDR (similar loss but chip to module)
  - Fibre Channel T11.2 32GFC (lower loss chip to module)