FEC TRADEOFFFS AND ANALYSES FOR 100G OPTICAL NETWORKING

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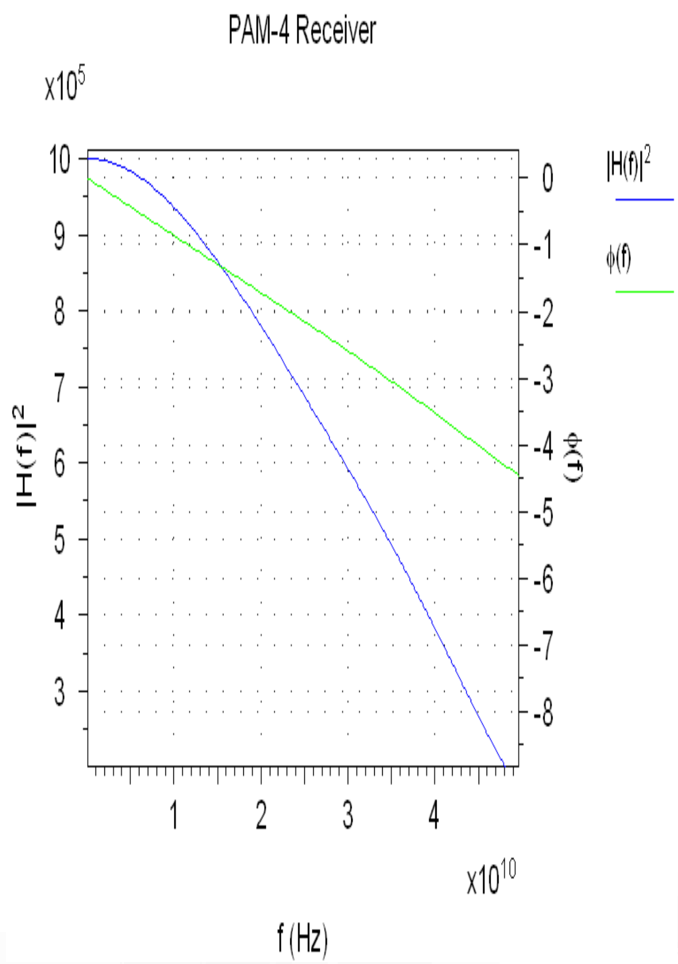
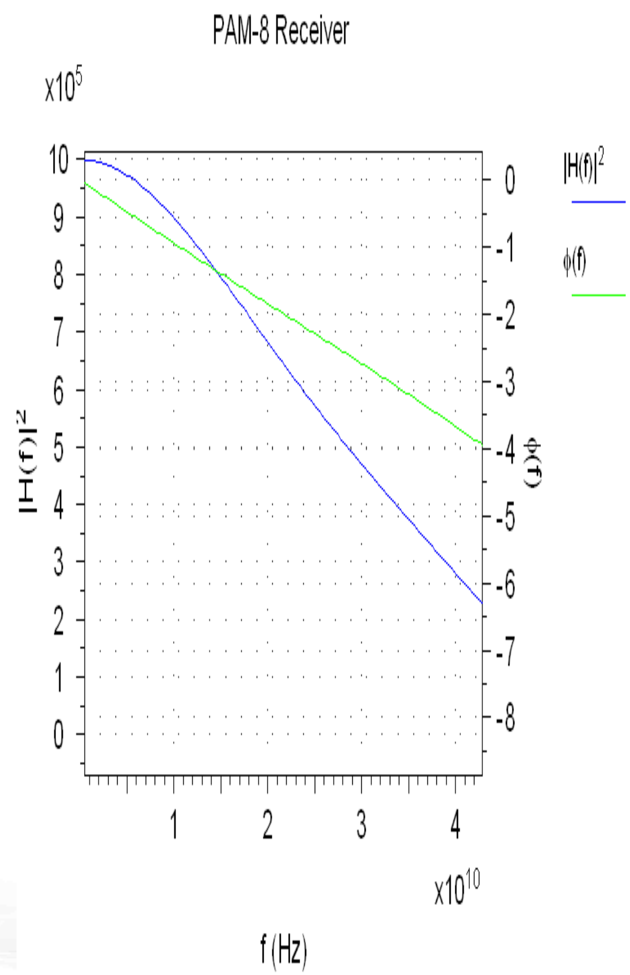
Motivation

- Defining a FEC code for 802.3bm should have following considrations in mind:
  - Overall FEC associated latency should be small, e.g., upper bounded by 250ns.
  - Overall power consumption should be reasonally small, e.g., ~ 200mW in 28nm CMOS
  - The efffective coding gain should be sufficiently large for the given modulation scheme.
  - If the selected code has much commonality with 802.3bj FEC codes, then it brings advantages in real implementation.
  - If RX can have options in achieving different tradeoffs between power, latency and coding gain for the specified code, it is good for various applications..
- Shannon limit vs real coding gain
  - A real FEC code can approach Shannon limit when the block size is very large, e.g., 1,000,000 bits.
  - Limited latency requirement generally leads to limited block length, which limits the final coding gain for a FEC code.
  - It is generally true that the higher the redundancy ratio, the harder for a real FEC code to get close to the Shannon limit.

Overclocking Loss (OCL)

- With PAM-4
  - 25% overclocking:
    OCL~= 6.0dB
  - 3% overclocking:
    OCL~= 0.72dB
- With PAM-8
  - 25% overclocking :
    OCL~= 3.8dB
  - 3% overclocking:
    OCL~= 0.46dB
- With DSQ128
  - 40% overclocking :
    OCL< 3 dB





FEC Options

- The burst error loss (BEL) is small for RS code with large t.
- 0% Overhead (OH), RS(1056, 1028, t=14, m=11)
  - similar to 100G-KR4 FEC (2.2X long, ~2X complexity, double t)
  - coding gain (CG) ~ 6.55dB, effective gain (EG) = CG – OCL – BEL= CG-BEL ~= 6dB.
  - latency ~ 190ns,
  - peak power (28nm) ~ 90 mw, average power < 60% peak power (depends on channel)
- 3% OH,RS(1088, 1028, t=30, m=11),
  - similar to 100G-KP4 FEC (2.2X long, ~2X complexity, double t)
  - coding gain ~ 7.66dB, EG=CG - (3% OCL) – BEL > 6.5dB
  - latency ~ 240 ns, peak power ~ 200mw.
- 6% OH RS(1120, 1028, t=46, m=11)
  - CG ~ 8.1 dB, Latency ~260ns, power ~= 310mw. EG > 6.5dB
- 100G-KR4 FEC (0% OH):
  - CG~=5.73dB, latency ~= 95ns, power ~=45mw
- 100G-KP4 FEC (3% OH)
  - CG~=7.04dB, latency ~= 102ns, power~=105mw

FEC Options (Cont'd)

- 20~50% OH single RS code
  - E.g., 20% OH, RS(312, 260, m=10, t=26), CG ~=8.5dB, peak power ~180mW, latency <150ns.
  - E.g., 50% OH, RS(312, 208, m=10, t=52), CG ~=10.0 dB, peak power ~ 350mW, Latency < 230ns
- 20~25% OH pseudo-product codes, only one Tx mode
  - RX mode-I: CG=6.54 ~ 7.12dB, peak power ~= 50mw, low latency < 25ns
  - RX mode-II: CG=11.0 ~ 11.7dB, long latency ~=1.5~ 2 us, avg. power: 250~300mw
- 20~25% OH, soft decoding FEC (LDPC code)
  - ~2000 bits per LDPC block
  - latency ~= 220ns
  - avg. power ~= 1.2W (28nm)
  - coding gain ~=11.8 ~ 12.4 dB
- 40% OH true-product code
  - E.g., use 64/65B transcoding, BCH(154, 130, t=3) x BCH(152, 128, t=3).
  - CG ~= 12.8dB (vague), latency ~ = 260 ns, average power ~ 300mw (vague).

Analyses

- For a target of 6 ~ 7 dB effective coding gain, 0~3% overclocking with simple RS FEC codes should be preferred.
- 20%+ OH hard-decision codes, neither single RS codes nor product codes are attractive due to increased power dissipation (PD) compared to 0~3% OH cases.
- 20%+ OH soft-decision FEC codes suffers from large power consumption.
- For 40%+ OH FEC codes, product codes should be considered for better tradeoff between coding gain and power consumption.
- For high OH cases, PD due to increased clock frequency can be very significant.

Summary

- Given the constraints on overall latency, FEC codes have to be well optimized to achieve good coding gain with reasonable PD.
- Promising FEC code options with different OH, PD, latency and coding gain are discussed and analyzed.
- Tradeoffs between soft-decision FEC and hard-decision FEC codes have been shown.