802.3bj FEC Overview and Status

IEEE P802.3bm

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Agenda

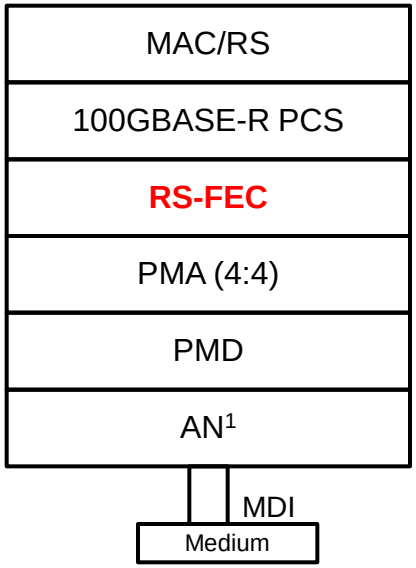
- Status of P802.3bj FEC
- Review of the RS-FEC architecture
- How the FEC could be applied to 802.3bm PMDs
- Issues to think about

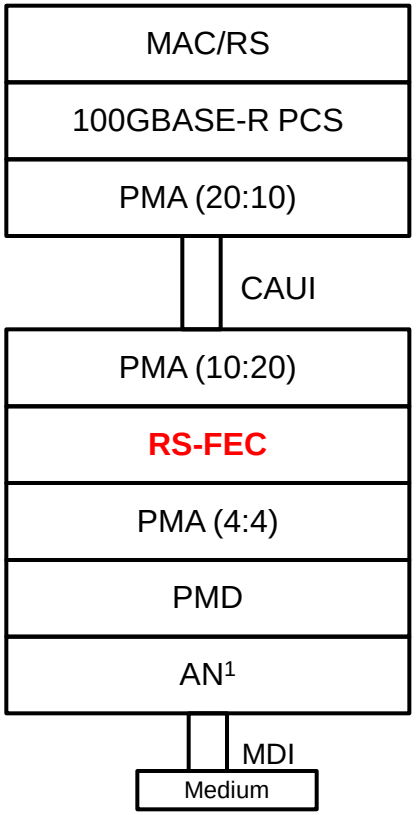
Status of 802.3bj FEC

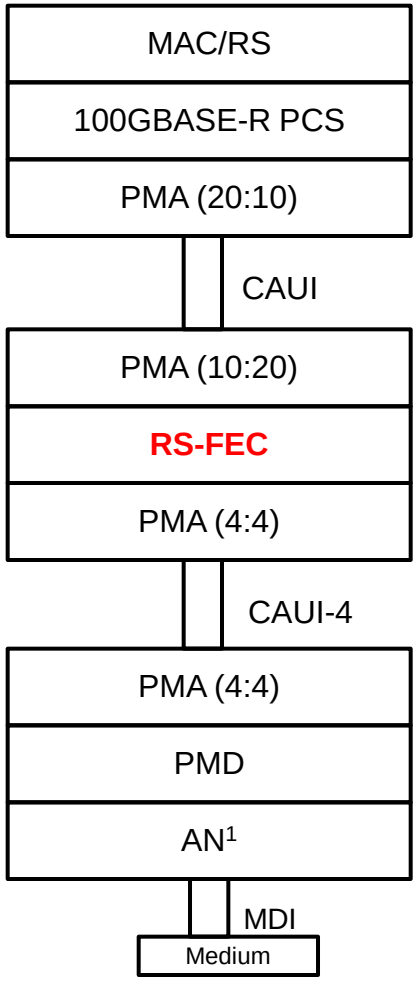
- **Comment resolution on draft 1.1 at this meeting**
- **Major open issues for Clause 91 “RS-FEC” sublayer:**
  - Signal_OK behavior
  - FEC behavior with EEE
  - FEC Codeword examples to be added
  - Management needs to be added
  - Delay constraints are TBD
- **In general the clause is pretty complete, but of course is subject to change since we are in task force review with the complete document in scope**

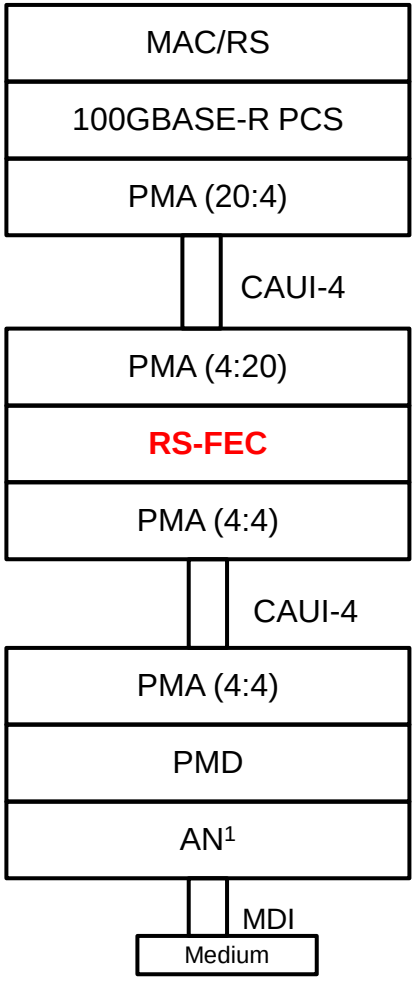
RS-FEC Architecture

- The figures below show possible implementations of the FEC architecture









Note 1: Conditional on PHY type

CAUI-4 – assumed new 25G+ interface

Draft 1.1 FEC Operation

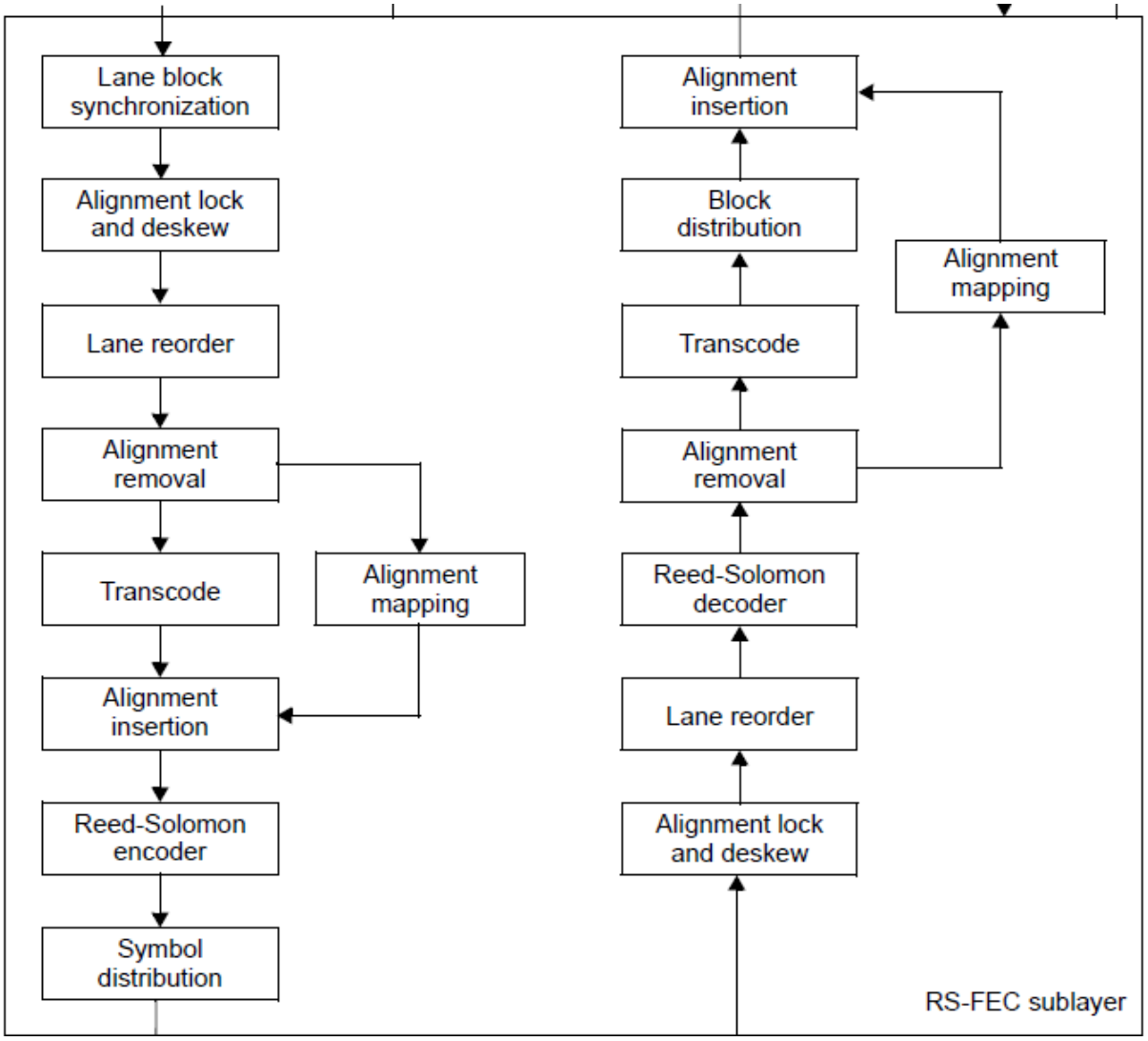
- **Backplane/Copper cable NRZ PHY (Clause 92 and 93):**
  - 256B/257B transcoding, so no increase in line rate for FEC operation
  - FEC is required to always be sent
    - Solves MTTFPA concerns when sending un-encoded 64B/66B data with 5 lane bit interleaving on a 25G lane
    - No Auto Negotiation needed
  - Adopted FEC code is RS(528, 514, T=7, M=10)
    - ~4.9 dB of gain at 10^{-15} output BER assuming burst errors due to DFE
    - ~5.3 dB of gain at 10^{-12} output BER assuming random errors
- **Backplane PAM4:**
  - Same 256B/257B transcoding as NRZ
  - FEC is required to always be sent and operates at 13.6 GBd
  - Adopted FEC code is RS(544, 514,T=15, M=10)
    - ~5.4 dB of gain at 10^{-15} output BER assuming burst errors due to DFE
    - ~6.5 dB of gain at 10^{-12} output BER assuming random errors
    - Gain figures assume that the only penalty for increase in rate is increased noise B/W
    - Includes pre-coding to reduce the effect of burst errors

Draft 1.1 FEC Operation Cont

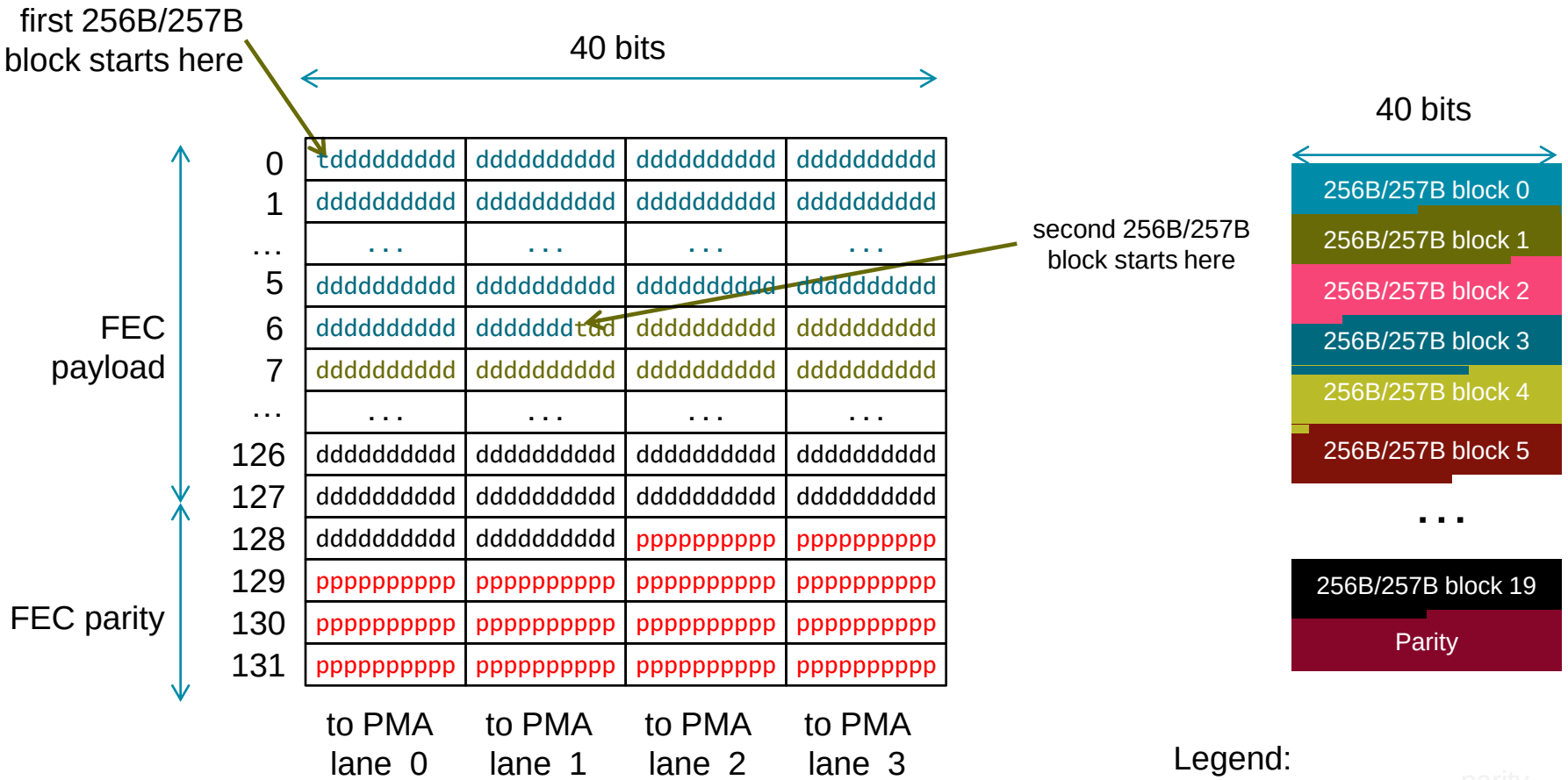
- **Draft 1.0 allowed you to send 64B/66B encoded data if FEC is not needed (loss < 30dB) for the NRZ PHY (backplane and copper cable)**
  - This reduces the latency for those channels/applications that don't need FEC
- **In cideciyan_01_0512 it was shown that sending 64B/66B data at a 10^{-12} BER has an MTTFPA of ~10^{4} years, falling to less than a year at a 10^{-7} BER**
  - Mainly due to the high probability of an error burst that extends to 4 bits due to the DFE, and how that error burst is spread in the packet due to the PCS lane bit multiplexing
- **Given the MTTFPA issues with sending bit multiplexed 64B/66B encoded data even on a low loss backplane or copper cable channel, the task force decide to require that FEC encoded data is always sent by the transmitter**
  - Other options explored were: block multiplexing, a new 4 lane PCS, pre-coding
- **The receiver has the option to:**
  - always correct (~100ns of added latency)
  - only detect errors for low loss channels (~ 50ns of added latency)
  - or do some proprietary trailing error detection if absolute lowest latency is needed (as low as 5ns of added latency depending how this is done)

Reed Solomon FEC Architecture

Processing flow is the same for NRZ and PAM4 PMDs in the FEC sublayer



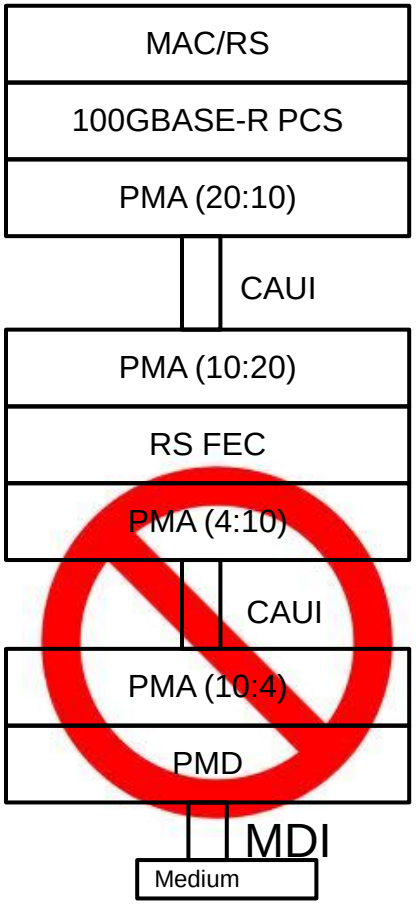
NRZ FEC frame structure



Legend:
“t” = 256B/257B header bit
“d” = 256B/257B data bit
“p” = FEC parity bit

Low Latency FEC Architecture

- The figure below shows an incorrect architecture, once the Low Latency FEC is inserted, the number of lanes cannot change!
  - At least not with the standard 802.3ba PMAs
  - Architectural restrictions being evaluated, exploring the possibility of supporting 4, 2 and 1 lane options. But we need to look at burst error behavior.



How applicable is the RS-FEC to Optics?

- Some presentations have shown significant increase in distance assuming the RS-FEC for SR4 optics
- The RS-FEC sublayer could be leveraged as is for optics
- Issues to solve:
  - When to enable FEC, for instance is it always on for a 100m SR4 PMD?
    - It is unclear if SR4 optics will have the same MTTFPA issues with sending 64B/66B encoded data as we had with copper interfaces (what are the correlated error properties?)
    - Tradeoffs between latency (~100ns) and operational simplicity?
    - How does the 20m PMD fit into this discussion?
    - Impact on form factor and power?
  - Or is there some mechanism (AN?) to turn it on only when it is needed (fiber is long enough to require FEC)?
  - Current linecard designs won't support it, so they can't benefit from the increase in reach
  - Common form factors between copper and optical imply that if FEC is used we should choose the same FEC as defined in 802.3bj

Summary

- The low latency RS FEC defined in P802.3bj can be re-used for 4-lane PMDs
- We would need to answer some of the questions surrounding when to enable FEC for optics

Thanks!