4x25G “Asymmetric” electrical interfaces proposal

Marco Mazzini
Vinu Arumugham

References and supporters

latchman_0808.pdf
dove_01_0812_optx.pdf
Cisco_feedback_to_CAUI4.pdf

SUPPORTERS
Alessandro Cavaciuti – Cisco –
Brian Eldridge – Cisco –
Brice Achkir – Cisco –
Gary Nicholl – Cisco –
Jane Lim – Cisco –
Ken Ly – Cisco –
Matt Traverso – Cisco –
Pirooz Tooyserkani – Cisco –

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Asymmetric host to module – proposals

- **Note: these are not CAUI-4 proposal** - there's already consensus around a single 10dB chip-module budget which is compatible with VSR and 802.3bj passive copper cable.
  Are rules to agree to make existing standards/parts interoperate together, so to guarantee CEI-28G-VSR TP1a and TP4a host compliance by using other standard parts.

- This presentation focus on details for informative annex which provides host designers guidance on asymmetric host to module performance.
  - may not be compatible with passive copper (not verified)
  - ensure CEI-28G-VSR compliance TP1a and TP4a over an extended (PCB) budget.

- Two "asymmetric" hosts are possible leveraging on current OIF standards:
  - CEI-25G-LR to CEI-28G-VSR (25G)
  - CEI-28G-SR to CEI-28G-VSR (28G)

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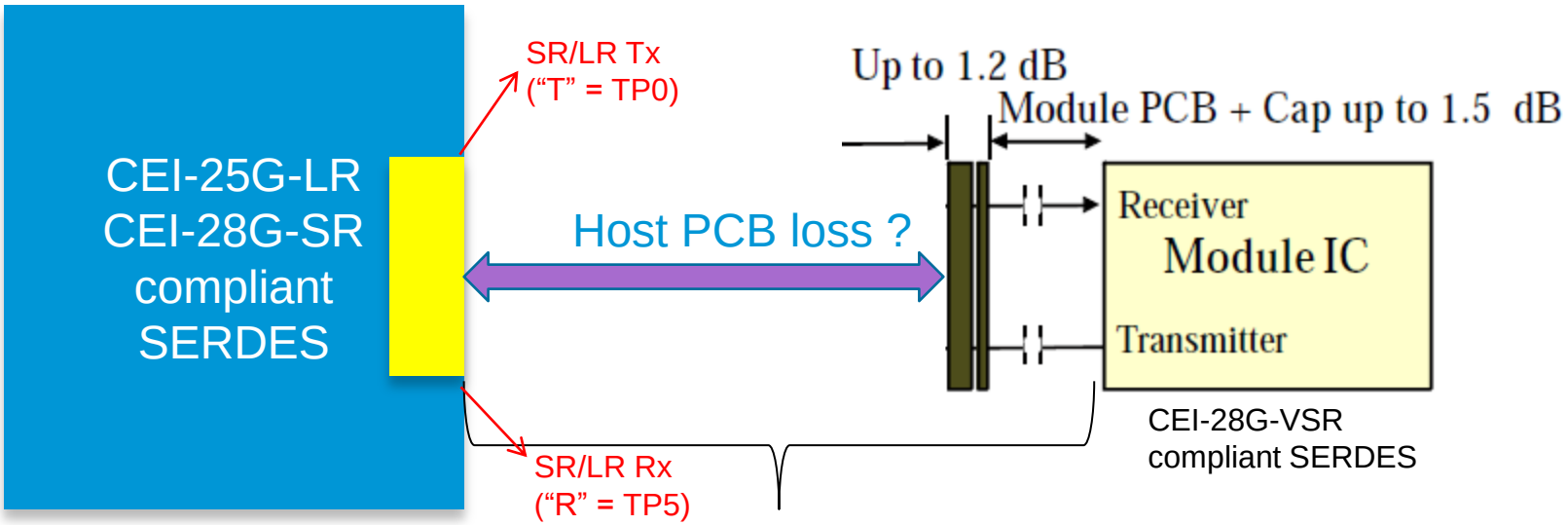
CEI-25G-LR (25G) or CEI-28G-SR (28G) to CEI-28G-VSR



How much for chip to module (total loss) ?

What is the maximum total loss we can support with a VSR interface in the module? The most challenging direction is from the SR/LR host Tx to module (VSR) Rx (left to right).

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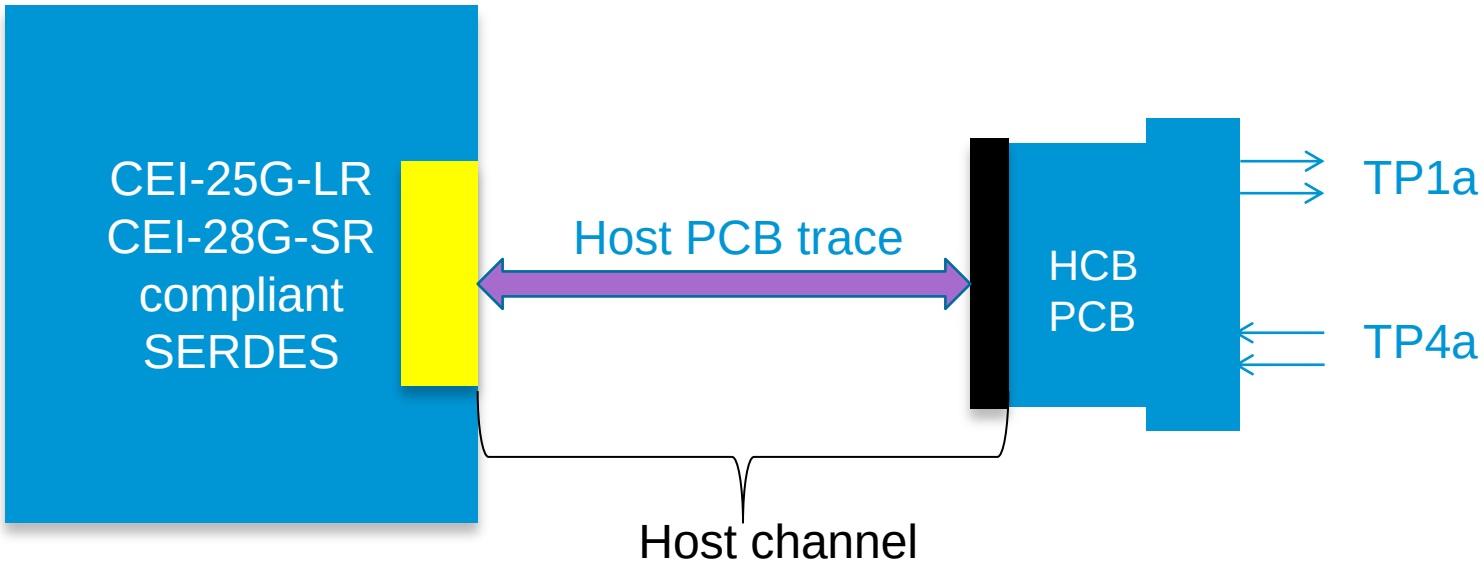
CEI-25G-LR (25G) or CEI-28G-SR (28G) to CEI-28G-VSR



Increasing the Host PCB loss, the VSR compliance @ TP1a becomes more challenging.

The main difference between CEI 28G SR TX and CEI 25G LR TX is the pre-cursor equalization capability (C-1).

Table 10-9. Coefficient range and step size

Coefficient	Normalized Amplitude		Normalized Step Size (%)
	Min (%)	Max (%)	
C_{-1}	-10	0	1.25 to 5
C_1	-25	0	1.25 to 5
C_0	40	100	1.25 to 5

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Simulation results

1. The topology included a TX BGA via, host trace, connector via, connector modeled with a 1" trace, connector via, HCB trace, SMA via.
2. Traces were 4.75 mil wide with 10.25 mil spacing, single stripline on Megtron 6, HVLP, 0.5 oz. copper.
3. All vias had a backdrill stub of 5 or 20 mil as shown in table above.
4. Tx post cursor de-emphasis was swept from 0-12 dB and the reported value provides the best performance.
5. Pulse response simulated in HSPICE and imported into StatEye to compute the statistical eye at a BER of 1e-15.

Case #	SR to VSR	25.8Gbps									
	Tx pre cursor (dB)	TX post cursor (dB)	CTLE (dB)	Host length (in)	Total loss (dB)	Host loss (dB)	Via stub length (mil)	TJ (UI)	EW15 (UI)	EH15 (mV)	
1	0	0	4	8	8.9	6	20	0.43	0.57	143	
2	0	5	0	11	11.2	8.3	20	0.47	0.53	140	
3	0	0	6	11	10.2	7.3	5	0.40	0.60	150	VSR budget
4	0	7	0	14	13.3	10.4	5	0.43	0.57	140	
5	1.3	7.7	0	14	13.3	10.4	5	0.47	0.53	120	
6	0.6	7.4	0	14	13.3	10.4	5	0.45	0.55	130	
7	0.6	4.3	2	14	13.3	10.4	5	0.47	0.53	120	
8	0	5	2	14	13.3	10.4	5	0.45	0.55	130	
9	0	0.9	6	14	13.3	10.4	5	0.42	0.58	113	
	SR to VSR	28Gbps									
4a	0	8	0	13	13.4	10.5	5	0.45	0.55	140	

This particular topology allow good EW15 / EH15 (0.6 UI / 150mV) for the “VSR budget” (case 3, green), against the CEI-28G-VSR limits of 0.46 UI / 100mV.

For the same topology and a total loss of 13.3dB (cases 4 to 9), we observe:

1. Similar EW15-EH15 numbers as in the VSR budget case (case 3 and 4).
2. Best case having Post-cursor ON, NO CTLE (better EH15, cases 4 and 9)
3. By turning on Pre-cursor (cases 4-5), results in some degradation on the eye opening.
4. No significant degradation between 25 and 28G (cases 4 and 4a).

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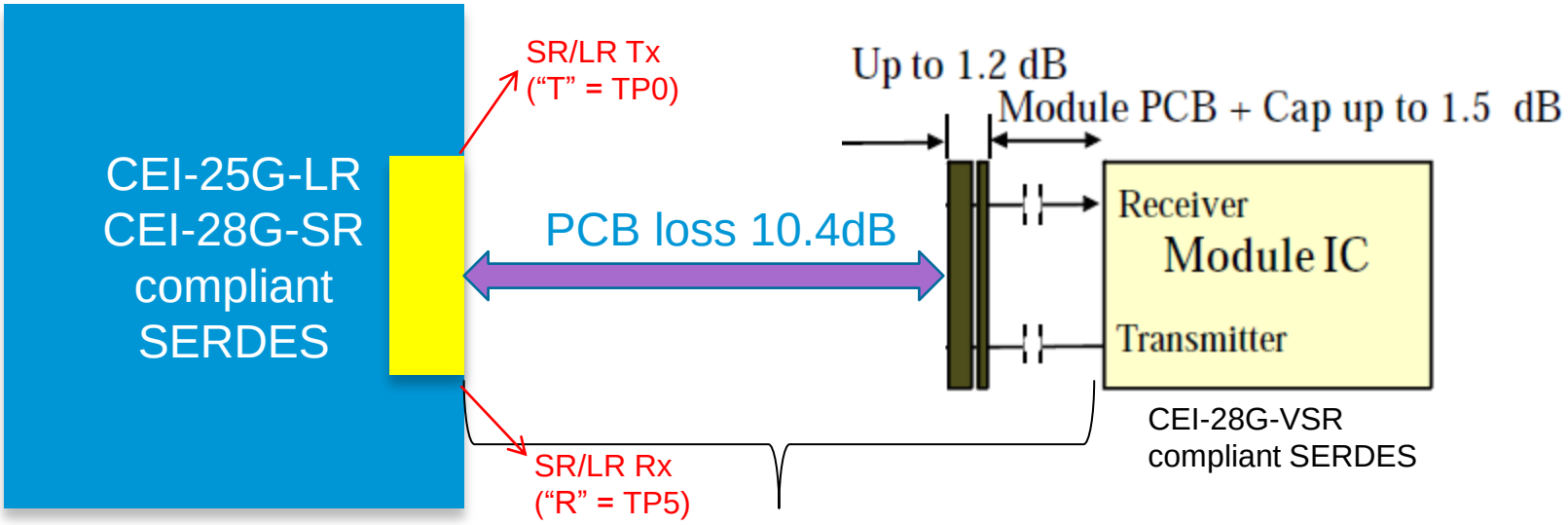
Comments



Total loss: 13.1dB

Seems Pre-cursor equalization to be not useful in this application, so CEI-25G-LR TX may not provide additional reach beyond CEI-28G-SR TX.

Our asymmetric host to module proposal is:
CEI-25G-LR/CEI-28G-SR to CEI-28G-VSR = 13.1dB, with host PCB loss of 10.4dB.

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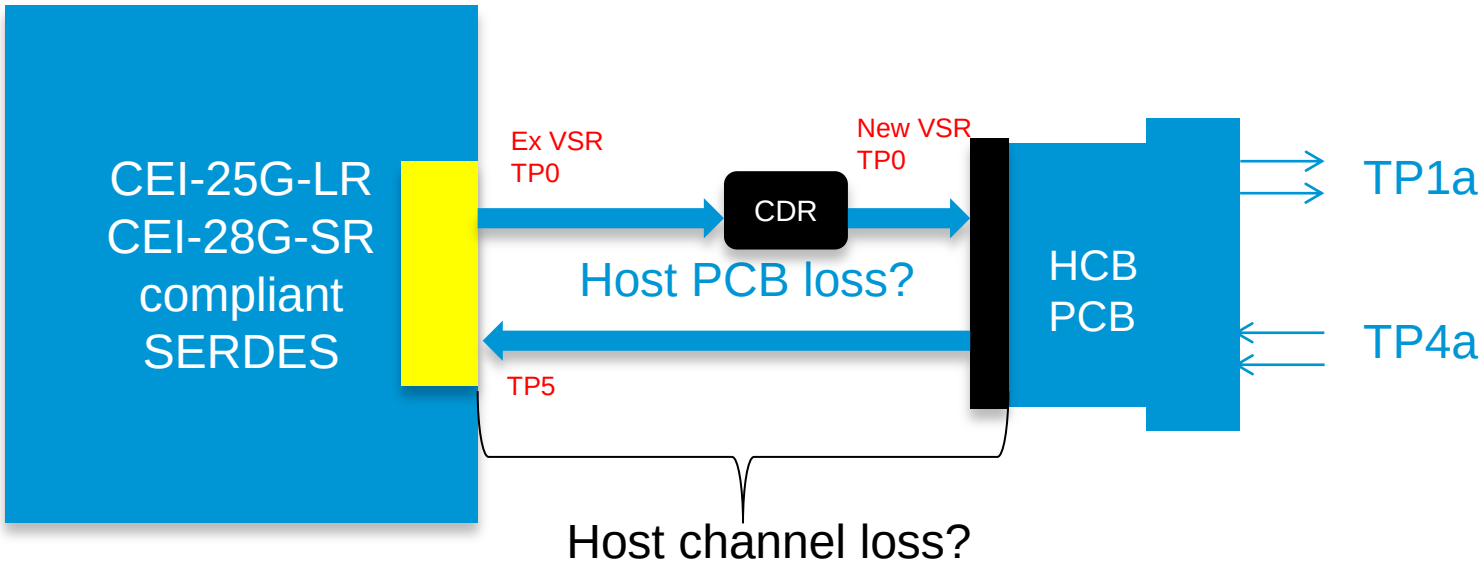
Asymmetric channel definition



Another option to increase PCB loss can be to put a retimer on the host between TP0 to TP1a. This will allow to remove the module VSR RX limitation (to compromise with added costs and design complexity), still leveraging on standard parts.

The asymmetric “channel” (different host loss for TX and RX paths):

(New) TP0 to TP1a: CEI-28G-VSR to CEI-28G-VSR

TP4a to TP5: CEI-28G-VSR to CEI-28G-SR (or CEI-25G-LR)

Cisco is considering this option too.

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Thank you.