EPoC Downstream Rate Adaption

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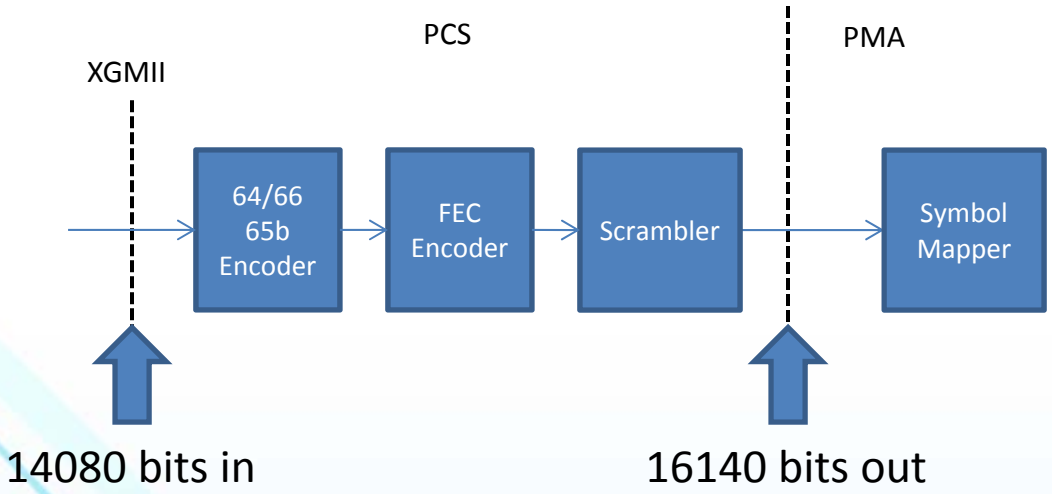
Overview

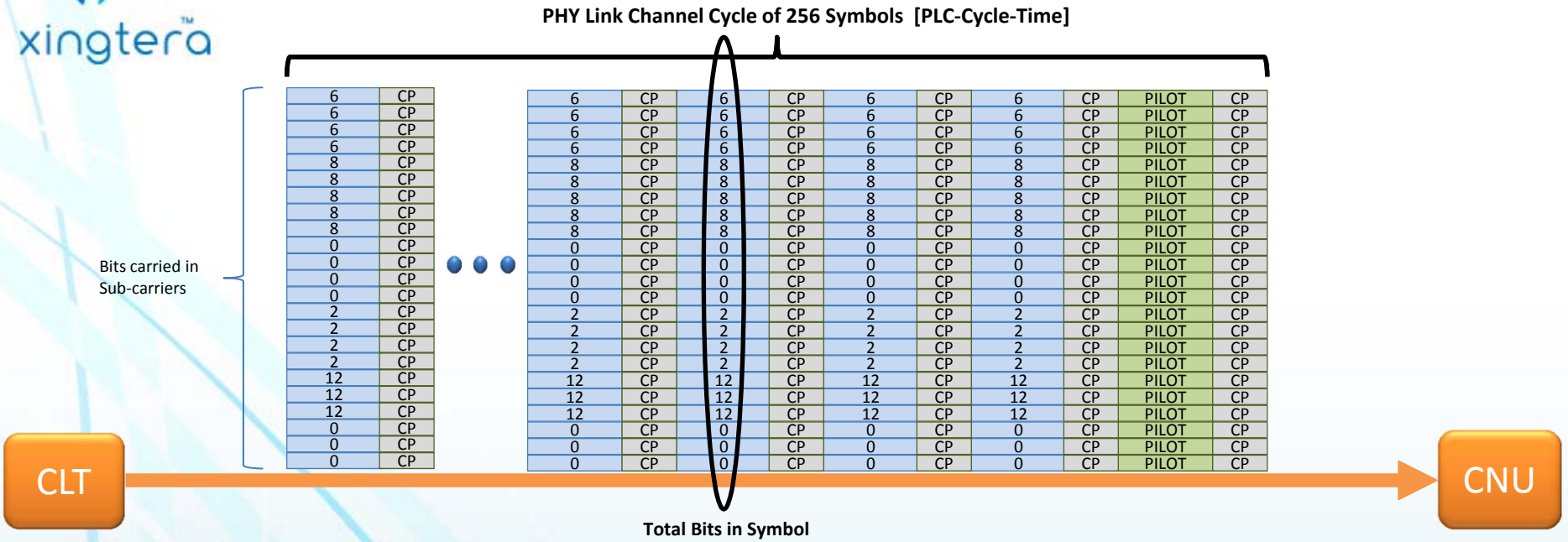
- This presentation describes the PCS & PMA to support a sub-rate downstream channel and downstream rate changes.
- A simple method to stream data from the PCS to PMA is considered.
- A modified Gearbox and IDLE deletion method is proposed.
- Disclaimers
  - For simplicity, this presentation uses 256 symbols for the number of symbols in a PLC cycle (assuming 20us symbol duration). It is easy to replace 256 symbols with 128 symbols or a different symbol size.

EPoC PCS Overhead



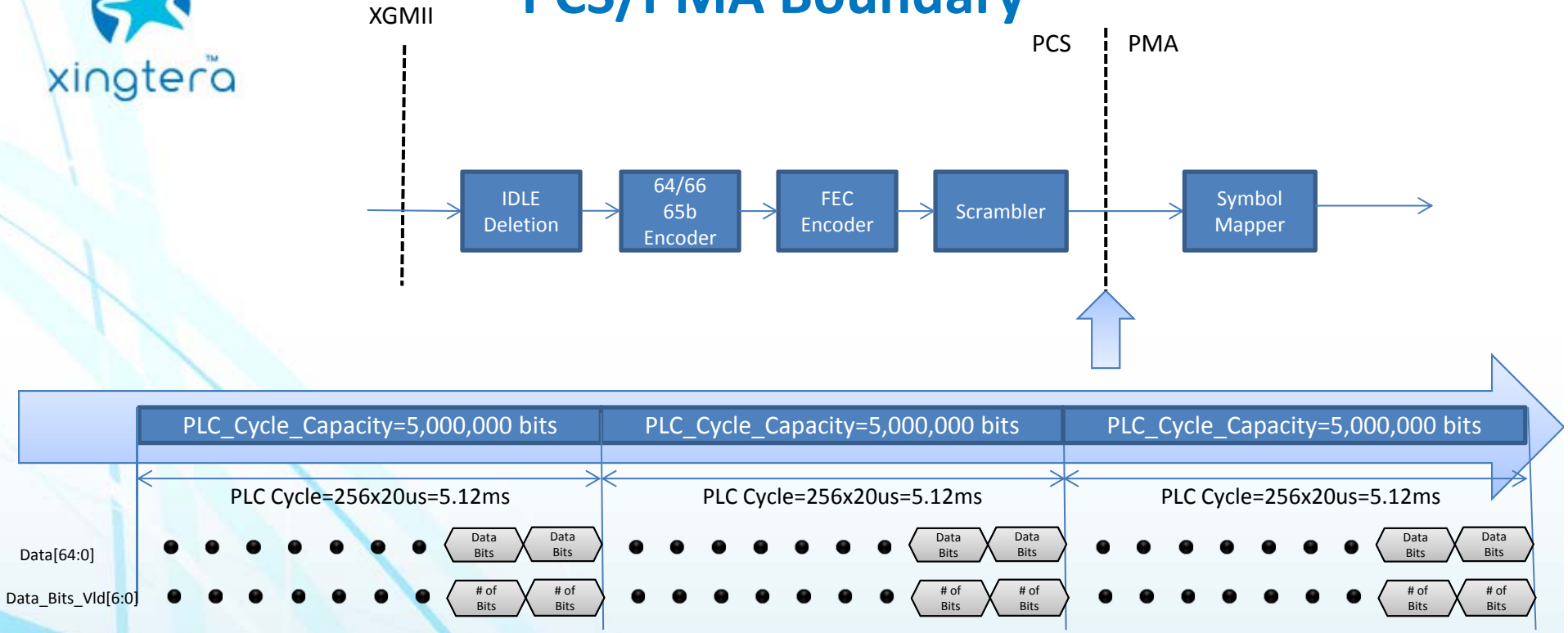
- Because of the fixed overhead 64/66 and single LDPC FEC code, the PCS has a known overhead from the input to the output.
  - Averaged over a single FEC block: 14080 bits into PCS produces 16140 bits out of PCS (87%)
- Data should be streaming at a constant rate from the PCS to the PMA.
- If the rate of PCS to PMA is known, the data rate at the XGMII can be determined for the IDLE deletion function.
- What is the streaming data rate at the PCS/PMA interface?

EPoC Downstream Rate at PCS/PMA Boundary



- Downstream MAC/PHY needs to have a known constant data rate.
  - Data Rate is averaged over PHY Link Cycle to absorb Pilots and cyclic prefix. (requires 1 symbol of delay)
  - Symbol Mapper will need to buffer 1 symbol worth of data to spread out over PLC cycle.
  - Pilots at the start of PLC cycle to avoid underrunning from streaming constant data.
    - Need to understand the implications of scattered pilots. Do we need to scatter the pilots? Do we need rules to avoid underrunning?
- Distribution of bits in sub-carriers or number of sub-carriers doesn't change Data Rate.
  - Only the total bits in symbol and the symbol/cyclic prefix size matter.
- PCS/PMA Data Rate is calculated…
  - PLC-Cycle-Capacity = Total-Bits-in-Symbol*(256-1)
  - PCS-PMA-Rate = PLC-Cycle-Capacity/PLC-Cycle-Time

PCS/PMA Boundary



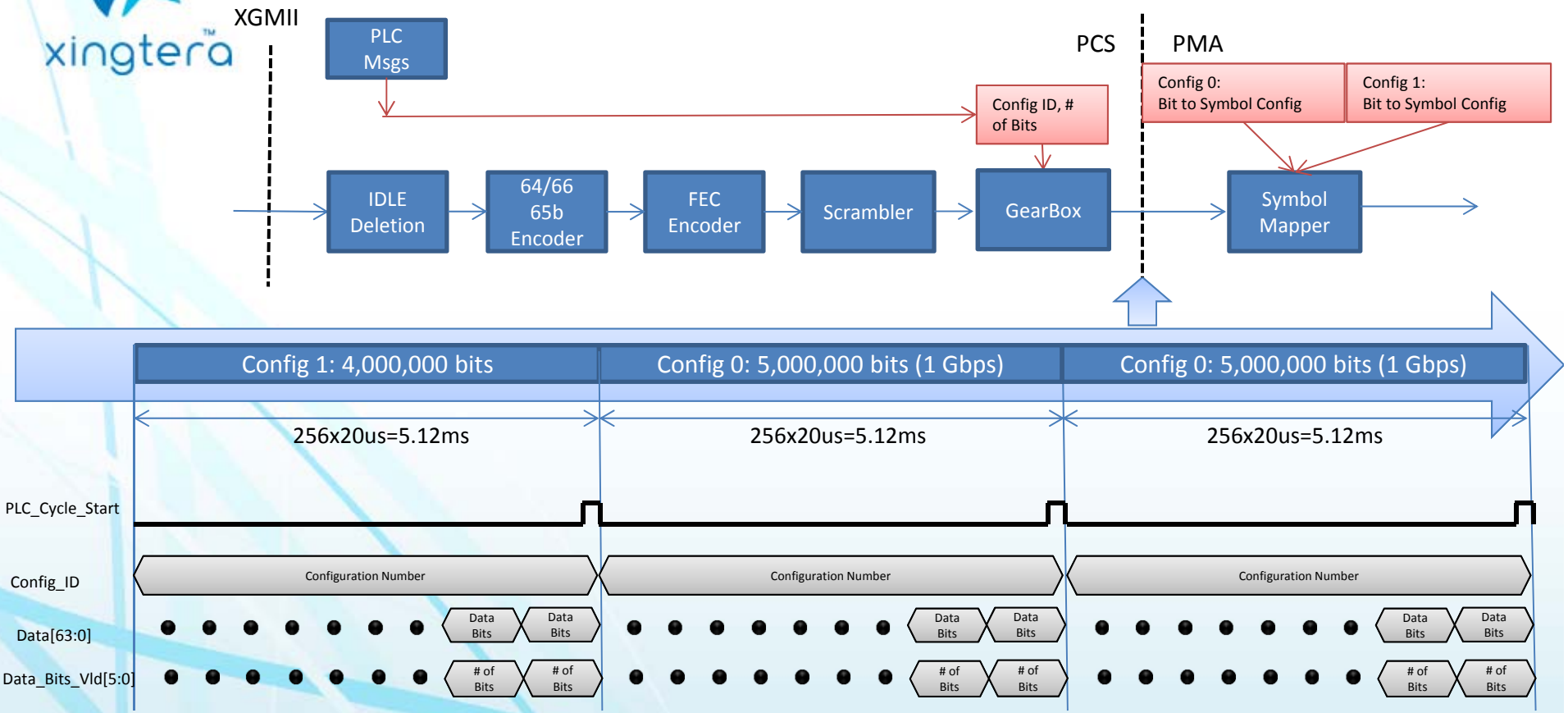
- PCS Streams data in 65 bit blocks to PMA.
  - Based on 204.8MHz clock, maximum data rate of 13.312 Gbps
- Data is spread evenly across entire PLC cycle.
  - PMA is responsible for buffering and smoothing data for Pilots

Configuration Switchover Review

- Goals
  - As CNUs register, the EPoC downstream maybe required to lower the bit loading to achieve a good BER.
  - During normal operation, interference may require the EPoC system to adapt the bit loading.
  - In both cases, it is important that EPoC provide a method to modify the bit loading table during normal operation and desirable that it be hitless (no packet loss) and non-service interrupting to the subscribers.
- Coordinating Switchover between MAC and PHY
  - MAC and PHY are not required to match transmit rates exactly.
  - The MAC TX rate must be equal to or less than PHY TX rate.
  - By selecting a proper order of operation, the TX can be safely changed
    - For decreasing rates: The MAC rate should be decreased before the PHY rate can be decreased.
    - For increasing rates: The PHY rate must be increased before the MAC rate is increased.
- Coordinating Switchover between CLT PHY and CNU PHY
  - The PLC Configuration ID allows for changing configuration at PLC Cycle boundaries.

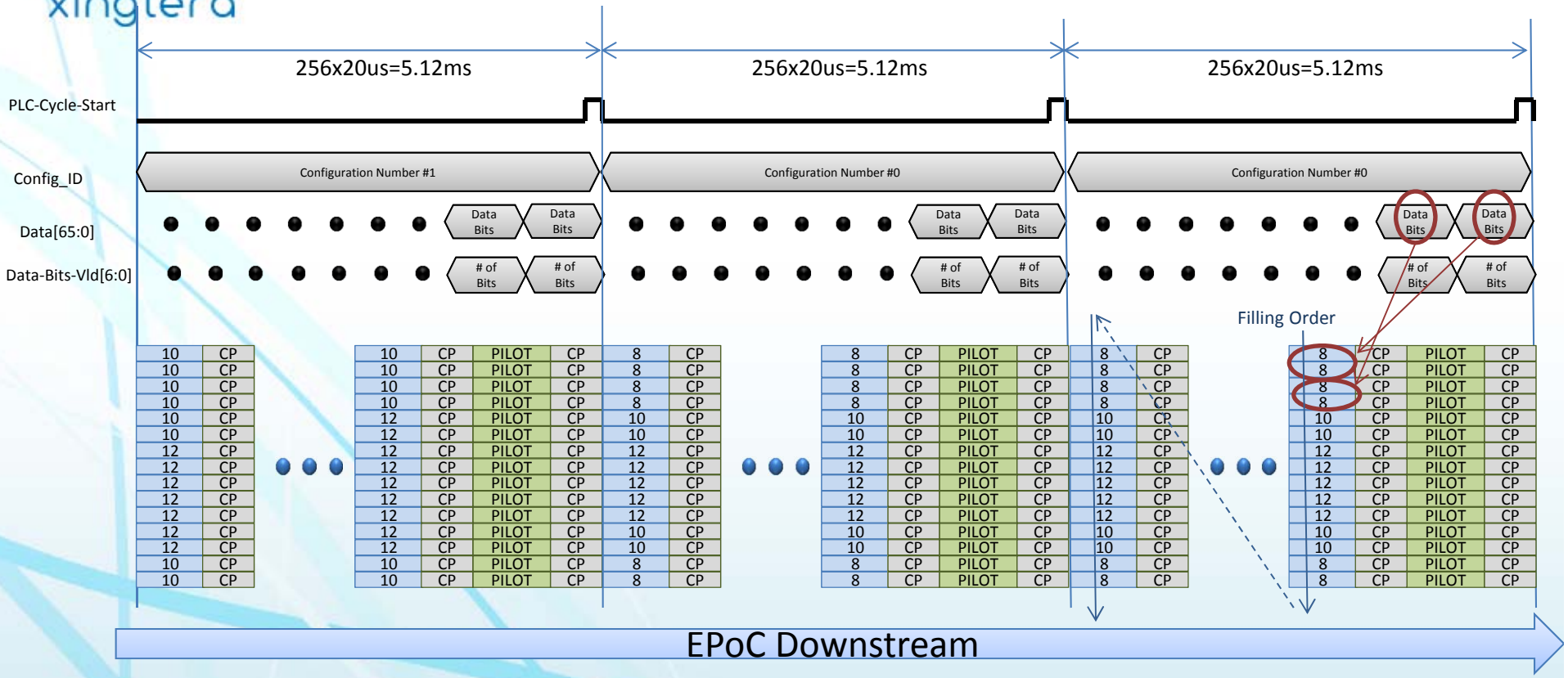
See boyd_3bn_02a_0313.pdf from the Orlando March 2013 meeting for additional details

PCS/PMA Boundary with Configuration Switch



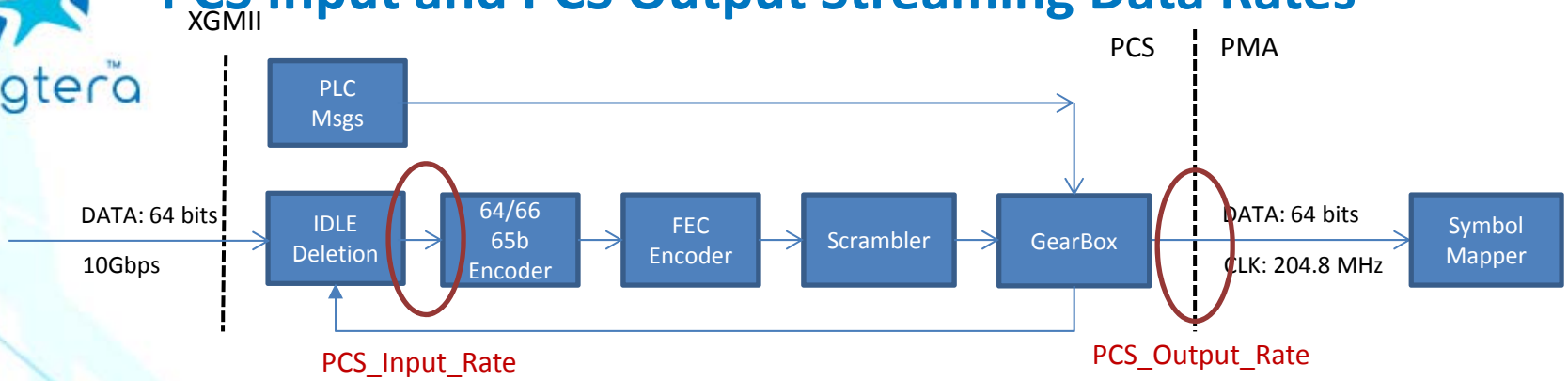
- PLC Cycle is a fixed duration and aligns with configuration boundaries.
- PLC Cycle Bit Capacity is based on configuration and could change over time.
- CLT PHY passes the configuration ID to the remote CNU PHY through the PLC Msgs.
- PLC Msgs block also passes the Configuration ID and bit capacity to the IDLE Deletion.
- PLC Cycle Start and Configuration ID are passed through the PCS to the PMA to clearly indicate the switchover between configurations on a PLC cycle boundary.

Downstream PMA Symbol Mapper (1D-to-2D)



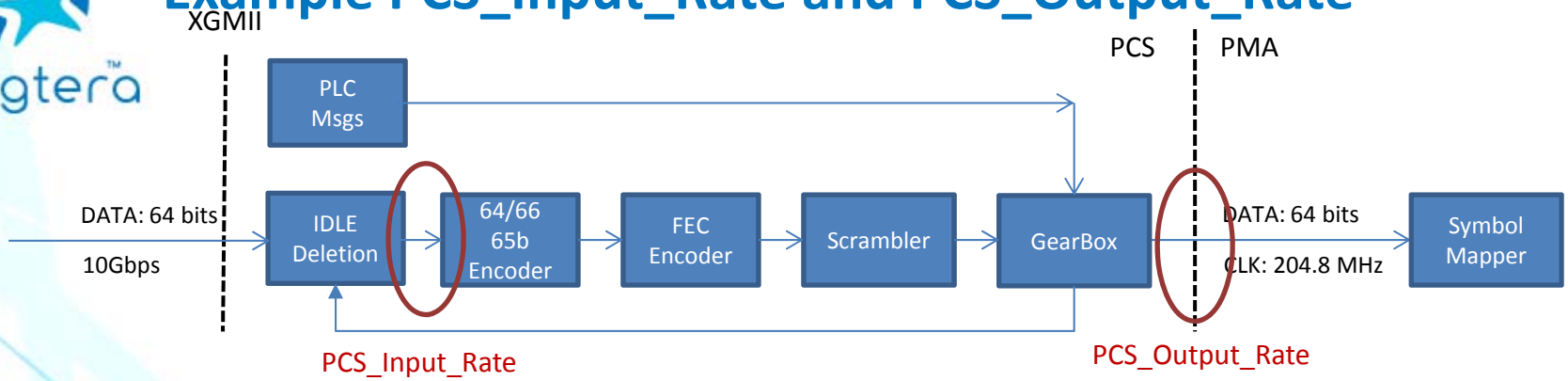
- A single Pilot Symbol is inserted on every sub-carrier at the start of the PLC cycle.
  - NOTE: Scattered Pilots could be considered as well but the pattern must guarantee than the output doesn't underflow.
- Streaming Data from the PCS is buffered and diced in a fixed order into the sub-carriers.
  - Frequency Interleaving would specify a different order for loading the data.
- Configuration changes (bit loading) will change the capacity of the entire PLC cycle and are aligned with new sub-carrier bit loading values for the PMA.

PCS Input and PCS Output Streaming Data Rates



- PCS_Output_Rate [Based on 204.8MHz clock counts]
  - PCS_Output_Rate = PLC_Cycle_Bits/PLC_Cycle_Clocks
- PCS_Input_Rate [Based on 204.8MHz clock counts]
  - PCS_Input_Rate = (65/66 Encoding Rate Ratio) * (FEC&CRC40 Rate Ratio) * PCS_Output_Rate
  - PCS_Input_Rate = (64/65)*(14300/16140)*PCS_Output_Rate [Substitute actual values based on current draft]
  - PCS_Input_Rate = (704/807)*PCS_Output_Rate [Algebra]
  - PCS_Input_Rate = (704/807)*(PLC_Cycle_Bits/PLC_Cycle_Clocks) [Substitute output rate equation]
  - PCS_Input_Rate = (704*PLC_Cycle_Bits)/(807*PLC_Cycle_Clocks) [Algebra]
- Based on configuration of the Symbol time, Cyclic Prefix, and Bit Loading, the PCS Input Rate and PCS Output Rate can be configured as a ratio of bits to 204.8MHz PMD clocks.

Example PCS_Input_Rate and PCS_Output_Rate



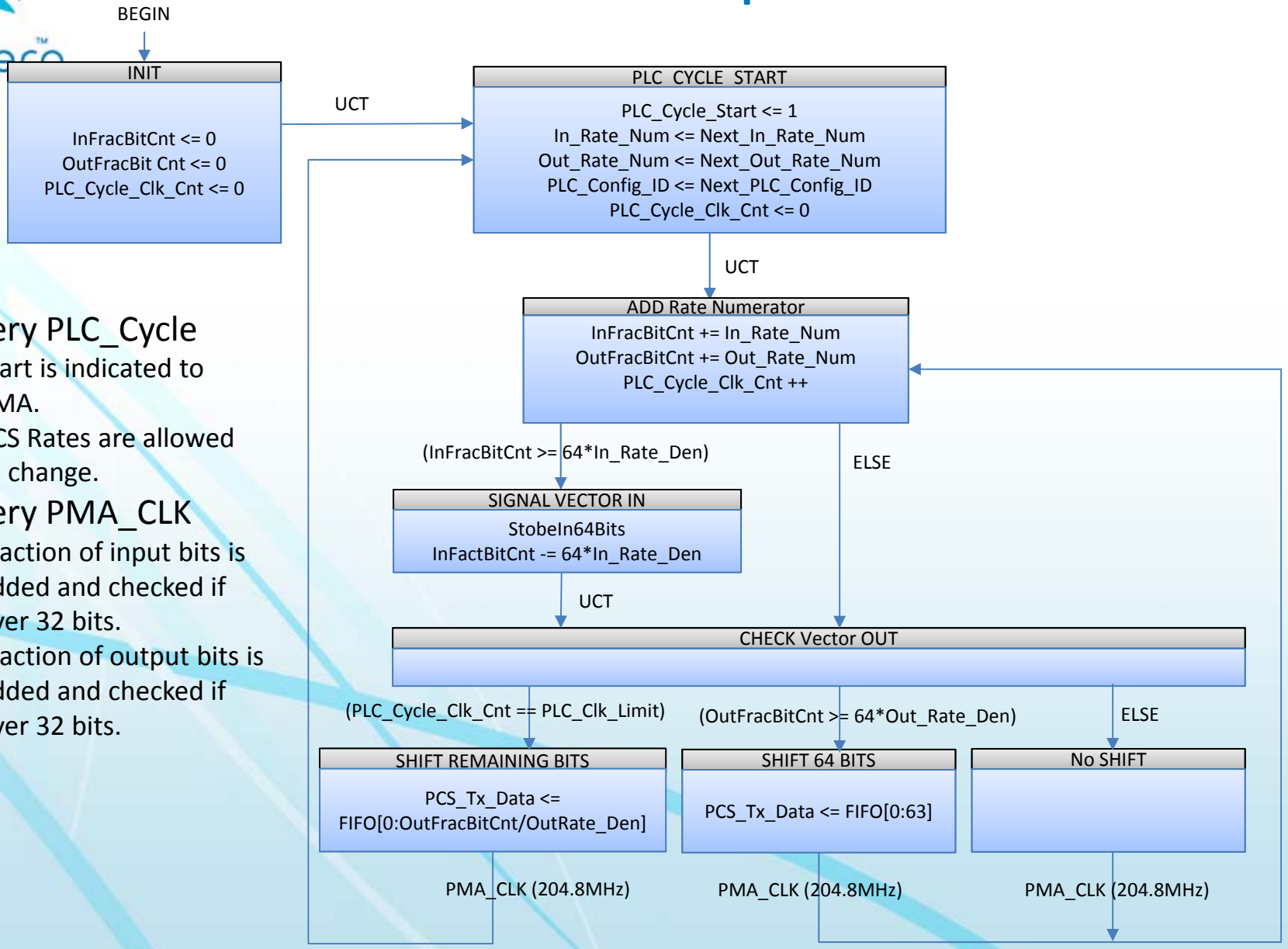
- PLC is configured for 20us symbol (4096 204.8MHz samples) and 1.25us CP (256 samples)
  - (4096 + 256)*256 = 1,114,112 clocks in a PLC Cycle Clocks
- For 1Gbps, the bit loading configuration would need to carry 5,440,000 bits of PCS output data in 255 Symbols.
- PCS_Output_Rate = 5,440,000/1,114,112 = ~4.88 bits/clk (For every 204.8 MHz clock, ~4.88 bits need to go from PMA to PCS)
- PCS_Input_Rate = (704*5,440,000)/(807*1,114,112)= ~4.26 bits/clk (For every 204.8MHz clock, ~4.26 bits need to come out of the IDLE Deletion function)

Gear Box Modifications

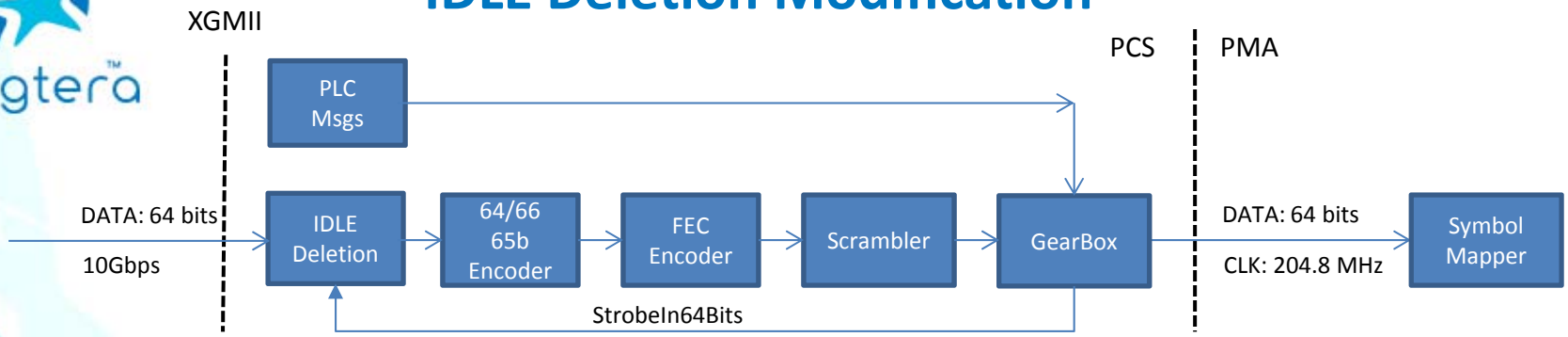
- The Gear Box generates the PCS interface signals to the PMA
  - PLC_Cycle_Start is indicated to the PMA from the PCS every PLC_Cycle.
  - 64 bits of data are shifted out of the PCS to the PMA based on the PCS_Output_Rate.
  - At the end of the PLC_Cycle, a final transfer of 64 bits or less is transferred to the PMA.
  - OutFracBitCnt counter in the state machine tracks the PCS_Output_Rate.
  - OutRateNum is the output rate numerator (PLC_Cycle_Bits)
  - OutRateDen is the output rate denominator (PLC_Cycle_Clocks)
- The Gear Box generates the PCS Input rate reference to the IDLE Deletion.
  - The PCS_Input_Rate equation is used to generate the GearBoxVecIn signal to the IDLE Deletion block.
  - GearBoxVecIn is pulsed whenever enough 204.8MHz PHY Clocks have passed to transmit 64 bits.
  - InFracBitCnt counter in the state machine tracks the PCS_Output_Rate.
  - InRateNum is the input rate numerator (704*PLC_Cycle_Bits)
  - InRateDen is the input rate denominator (807*PLC_Cycle_Clocks)
- PLC Cycle Boundaries
  - The PLC_Cycle_Clocks should be configured at initialization and not changed without re-init. (Symbol and CP size)
  - The InRateDen and OutRateDen are therefore configured but constant.
  - The InRateNum and OutRateNum will change based on bit loading at PLC cycle boundaries.

Gear Box - Rate Adapter

- On Every PLC_Cycle
  - Start is indicated to PMA.
  - PCS Rates are allowed to change.
- On Every PMA_CLK
  - Fraction of input bits is added and checked if over 32 bits.
  - Fraction of output bits is added and checked if over 32 bits.



IDLE Deletion Modification



- The IDLE Deletion function should be modified to accurately match the EPoC PHY.
  - The current ratio referenced to the XGMII transfers does not accurately represent the output rate at the PMA.
  - GearBox will pulse signal (StrobeIn64Bits) to give reference for PCS_Input_Rate.
  - Since GearBox is referenced to the PHY Line Clock (204.8MHz), it can accurately track the data rate of the PMA.
- The IDLE Deletion function should be able to support bit loading configuration changes
  - Configuration changes are triggered by the PLC and passed to the GearBox.
  - The GearBox will accurately track a rate change on a PLC Cycle.
  - The StrobeIn64Bits period will be adjusted by the GearBox for the rate change.
  - The IDLE Deletion block is not required to have any information on the rate change other than the StrobeIn64Bits.

IDLE Deletion Modifications

Current Draft

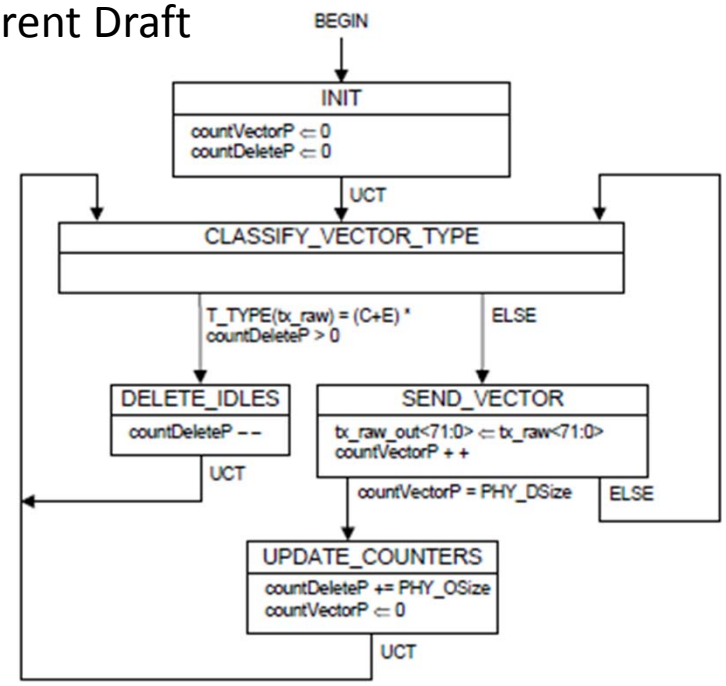
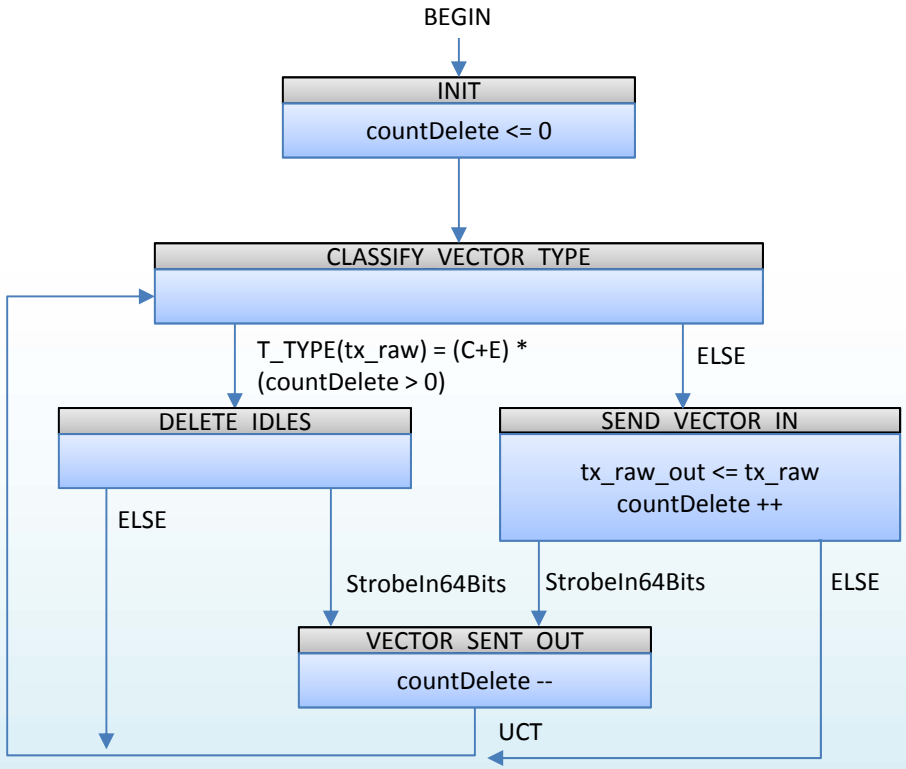


Figure 101–4—CLT Idle control character deletion process (data rate adaptation sub-process)

Proposed



- Increment countDelete whenever a vector is passed through IDLE Deletion block.
- Decrement countDelete whenever the Gear Box signals the transmit of a vector's worth of data.
- If (countDelete > 0) and vector is idle, drop the vector.

Downstream Data Rate Summary

- PMA Symbol Mapper
  - Single Symbol of Pilots is the simplest approach for insertion but Scattered pilots could work as well.
  - Symbol mapper should be defined to buffer 1 symbol of data to smooth data over PLC cycle.
- PCS/PMA Interface
  - 64 bit interface clocked at 204.8MHz (sampling clock locked)
  - Configuration ID and PLC Cycle Start should be included in the interface.
- GearBox
  - Uses PHY clock to accurately control data rate into and out of the PCS.
  - Changes data at PLC cycle boundaries to allow for hitless bit loading changes.
- IDLE Deletion
  - A single function based on the output streaming rate should be used. (combine FEC and sub-rate functions)
  - Input rate is signaled from GearBox.

Straw Poll

- Use this presentation as a starting point Baseline for the Downstream FDD GearBox including:
  - Accurate Rate control for the PCS-to-PMA
  - Accurate Rate control for the IDLE Deletion Function
  - Bit Loading Configuration Switchover at PLC Boundaries

- YES:
- NO:
- ABSTAIN:

Straw Poll

- Simplify the IDLE Deletion function into a single process with the data rate reference from the GearBox.

- YES:
- NO:
- ABSTAIN: