MANAGEMENT REGISTERS AND MIB OBJECTS

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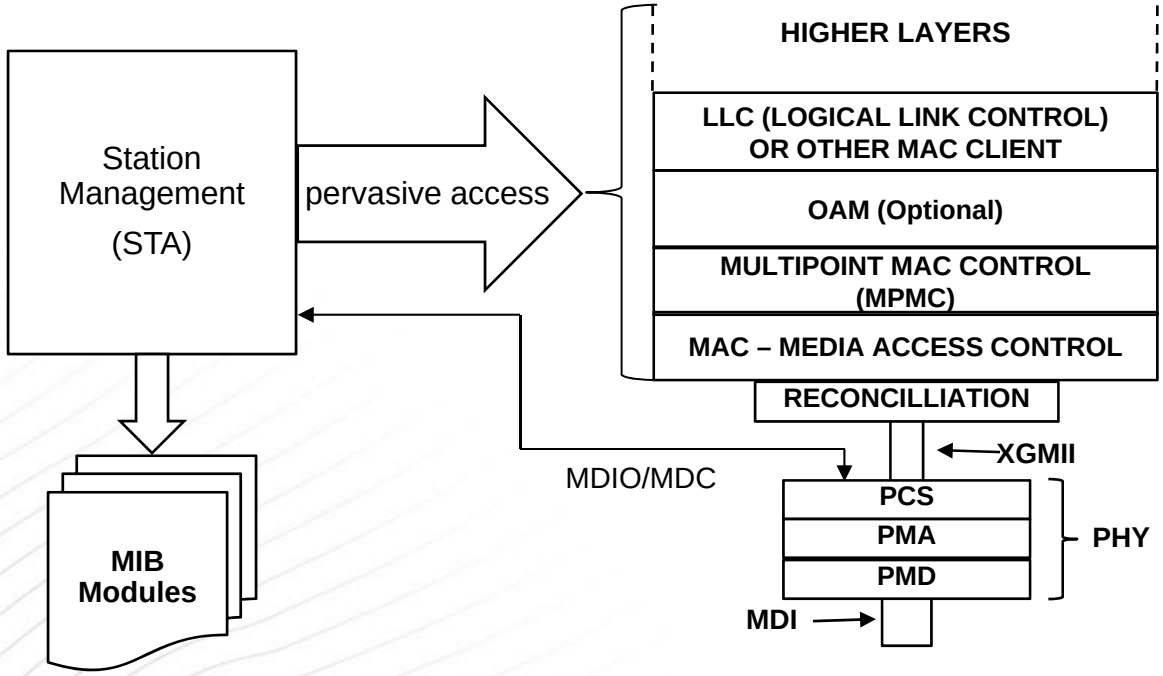
OUTLINE

- Layer model and interfaces
- Clause 45 management registers
- MDIO/MDC
- MIB modules and objects

LAYER MODEL AND INTERFACES



Relationship of Station Management to Ethernet sub-layers

PHY MMD LAYER MODEL

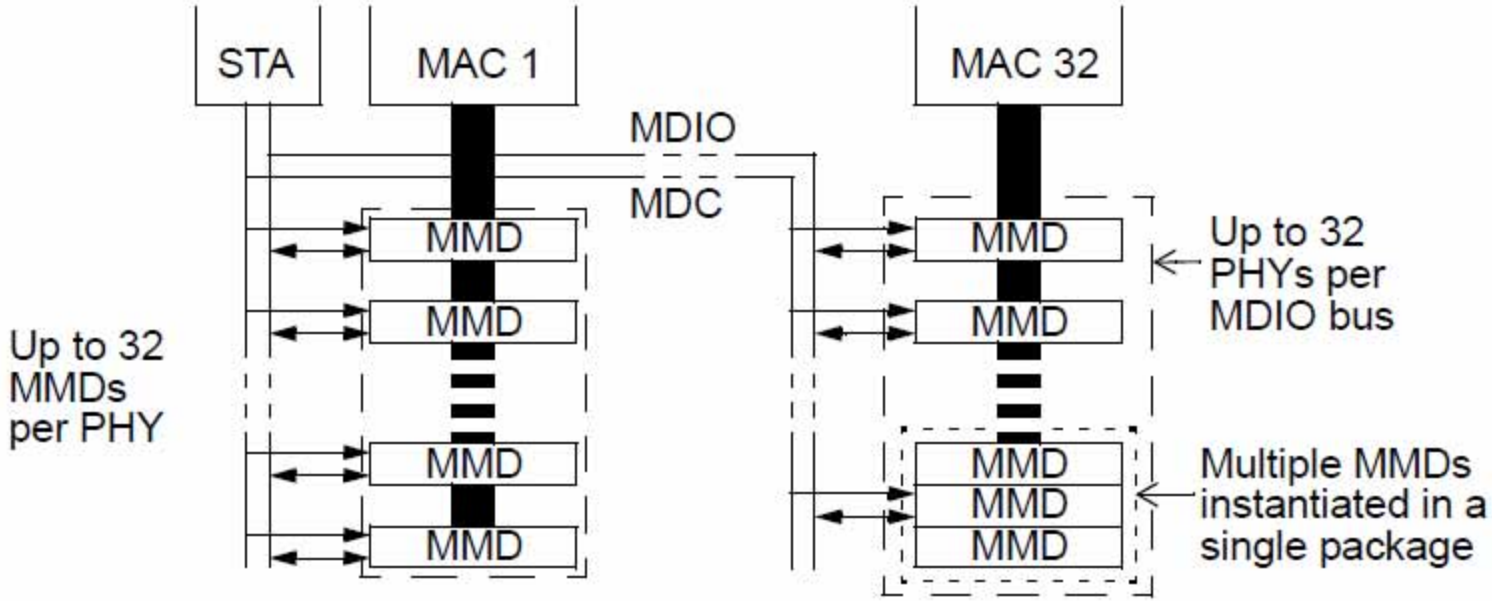


Figure 45–1—DTE and MMD devices

MMD = MDIO Manageable Device

up to a maximum of 65,536 registers in each MMD

CLAUSE 45 MMDS

Table 45–1—MDIO Manageable Device addresses

Device address	MMD name
0	Reserved
1	PMA/PMD
2	WIS
3	PCS
4	PHY XS
5	DTE XS
6	TC
7	Auto-Negotiation
8	Separated PMA (1)
9	Separated PMA (2)
10	Separated PMA (3)
11	Separated PMA (4)
12 through 28	Reserved
29	Clause 22 extension
30	Vendor specific 1
31	Vendor specific 2

EPoC may wish to specify new registers in these MMDs

CLAUSE 45 REGISTERS

- **Each MMD has a large addressable register space**
  - numbered 0 through 65,535
  - 0 through 32,767 defined by IEEE 802.3, or reserved for future definition by IEEE 802.3
  - 32,768 through 65,535 are allocated for vendor specific features
- **Each register is 16 bits wide**
  - numbered 0 through 15
- **MMD/Register/bit numbering convention:**

  MMD.Register.bit
- **Example: PMA/PMD reset bit, 1.0.15**

Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.0.15	Reset	1 = PMA/PMD reset 0 = Normal operation	R/W SC

CLAUSE 45 REGISTERS

- **Some have expressed concern that the Clause 45 register space is limited**
  - This is true for some MMDs, such as the PCS, which already have a large number of registers defined
- **However, there are ways to get around this limitation**
  - Define a new type of MMD
  - Define a new level of indirection
    - For example, define a sub-carrier index register

MDIO/MDC

- **MDIO/MDC is a very simple serial interface protocol that is easily implemented in just about any ASIC/SoC process**
- **It is, however, not all that speedy**
  - The minimum period for MDC is 400 ns
  - One bit may be transferred on each MDC cycle
  - Each register transfer of 16 bits requires an additional 16 bits of overhead
  - Thus, the nominal data transfer rate is about 1.25 Mb/s
  - Keep this in mind when sizing counters
- **MDIO/MDC is the only mechanism defined in IEEE Std 802.3 that provides access to PHY control and status registers**
  - Magical interfaces are vendor specific
- **The PHY is unique in this regard, because station management is assumed to have “pervasive access” to all other sub-layers (e.g. MAC, MPCP, OAM)**

MIB MODULES AND OBJECTS

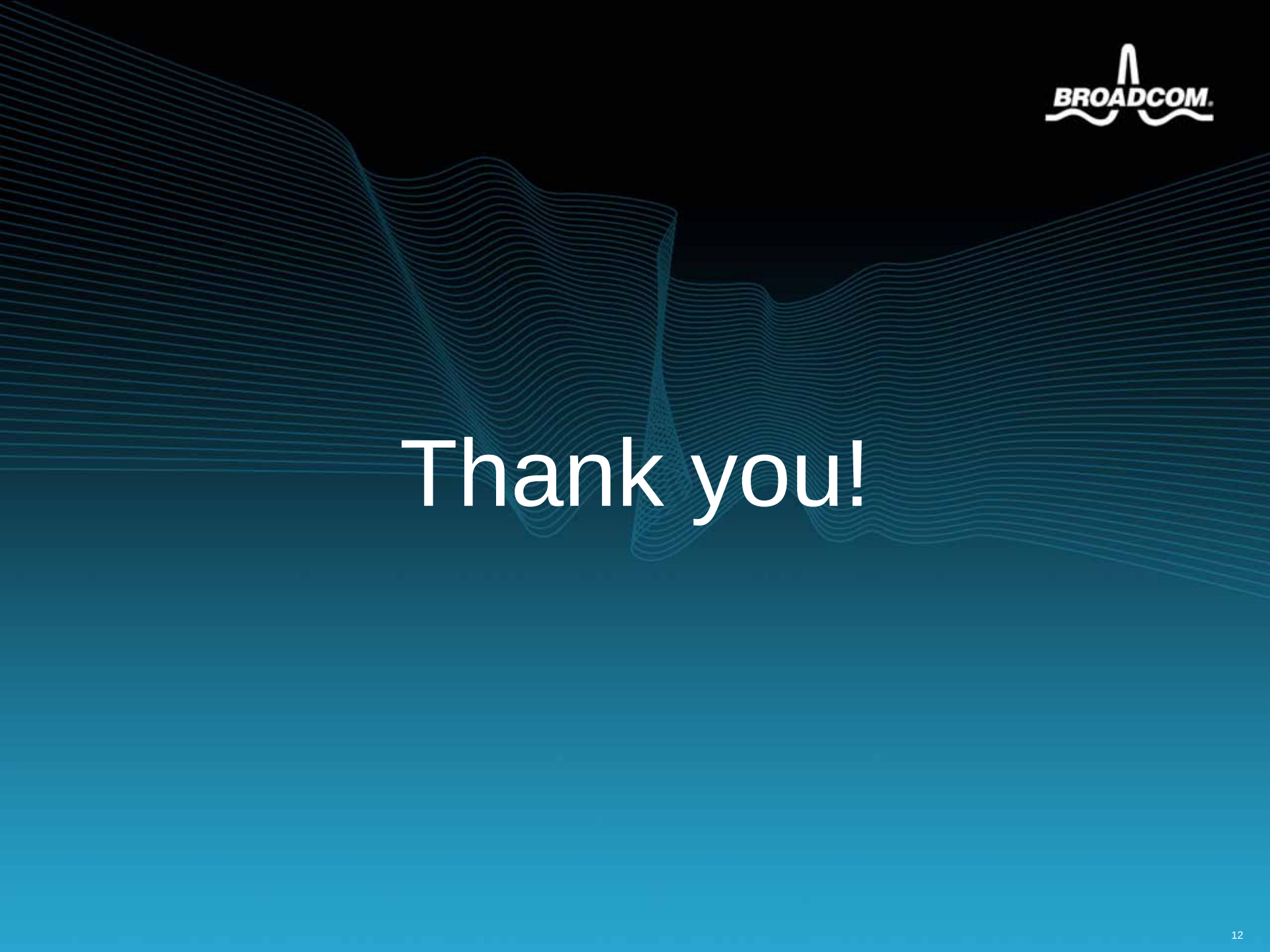
- **IEEE Std 802.3 defines managed attributes in a set of protocol-independent Management Information Base (MIB) modules**
  - Clause 30
- **In general, every attribute (e.g., each Clause 45 register) that must be exposed to a management entity is defined in Clause 30**
- **These definitions must be provided in the IEEE P802.3bn amendment**
- **An important rule for Clause 30 attributes is that we never define an attribute that can be readily derived from other attributes**
  - If C = A + B, we may define A and B, but we do not define C
- **Counters in the MIB modules can be larger than the corresponding counters in the PHY registers**

MIB MODULES AND OBJECTS

- **IEEE Std 802.3.1 defines MIB modules for use with the Simple Network Management Protocol (SNMP) using the Structure of Management Information version 2 (SMIv2)**
  - SMIv2 is a subset of ASN.1
- **Every attribute in IEEE Std Clause 30 has a corresponding object definition in IEEE Std 802.3.1**
- **Unlike Clause 30, the MIB modules in 802.3.1 may contain objects that are derived from other objects**
  - After all, it's only software
  - Go ahead, use 64 bit counters
- **There is no mechanism by which PHY control and status information can show up in a MIB module, other than by being transferred via MDIO/MDC**
  - Management does not have "pervasive access" to the PHY

MIB MODULES AND OBJECTS

- **IEEE Std 802.3.1 is a separate document from IEEE Std 802.3**
  - It is maintained, revised and amended by the MIB modules Task Force
  - The 802.3bn EPoC PHY Task Force does not need to worry about it
- **Once IEEE P802.3bn is completed, the Working Group will decide whether to kick off an amendment project on 802.3.1, or wait for the next revision project on 802.3.1**
- **Either way, I expect that the EPoC PHY will warrant a new MIB module in 802.3.1, due to the volume of new and unique managed objects**
  - It will probably also require “minimal augmentation” of some existing modules, such as OAM, EPON (aka MPCP) and MAU (aka PHY)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Thank you!