

EPoC PCS Status Update (Clause 101)

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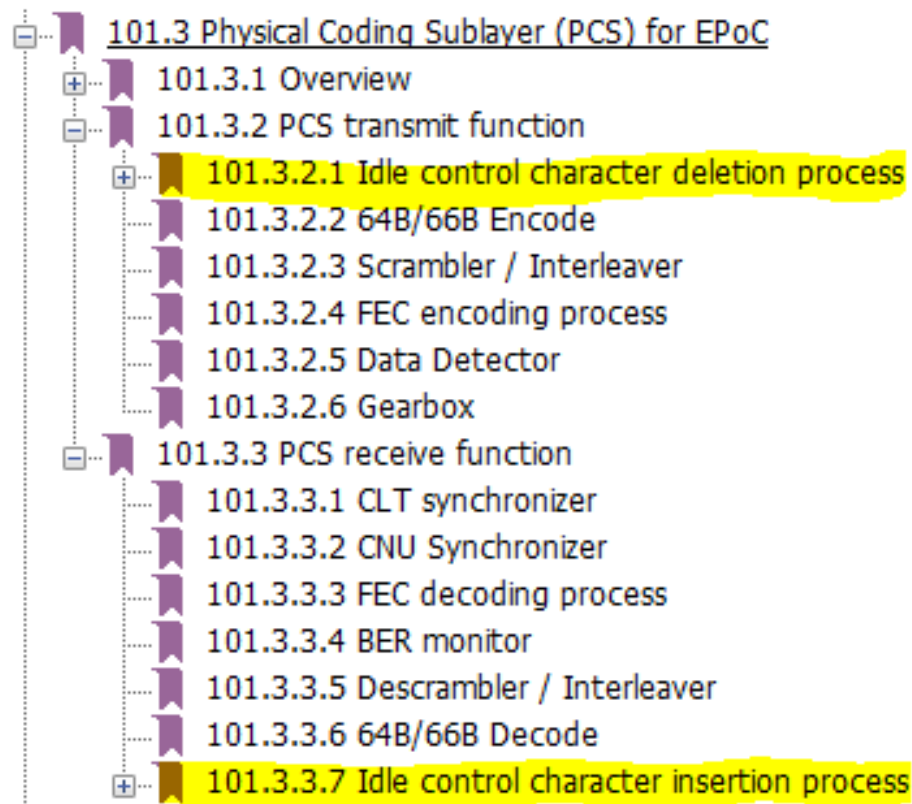
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Clause 101 Outline

- [-] 101. Reconciliation Sublayer, Physical Coding Sublayer, and Physical Media Attachment for EPoC
 - [-] 101.1 Overview
 - 101.1.1 Conventions
 - 101.1.2 Constraints for delay through RS, PCS, and PMA
 - [-] 101.2 Reconciliation Sublayer (RS) for EPoC
 - 101.2.1 Overview of EPoC RS operation
 - 101.2.2 Summary of major concepts
 - [+] 101.2.3 10 Gigabit Media Independent Interface (XGMII)
 - [+] 101.2.4 Functional specifications for multiple MAC instances
 - [-] 101.3 Physical Coding Sublayer (PCS) for EPoC
 - [+] 101.3.1 Overview
 - [+] 101.3.2 PCS transmit function
 - [+] 101.3.3 PCS receive function
 - 101.4 EPoC_PMD_Name PMA
 - 101.5 Power-saving capabilities
 - 101.6 TimeSync capability
 - [-] 101.7 Protocol implementation conformance statement (PICS) proforma for Clause 101,
 - 101.7.1 Introduction
 - [+] 101.7.2 Identification
 - 101.7.3 Major capabilities/options
 - [+] 101.7.4 PICS proforma tables for clause title

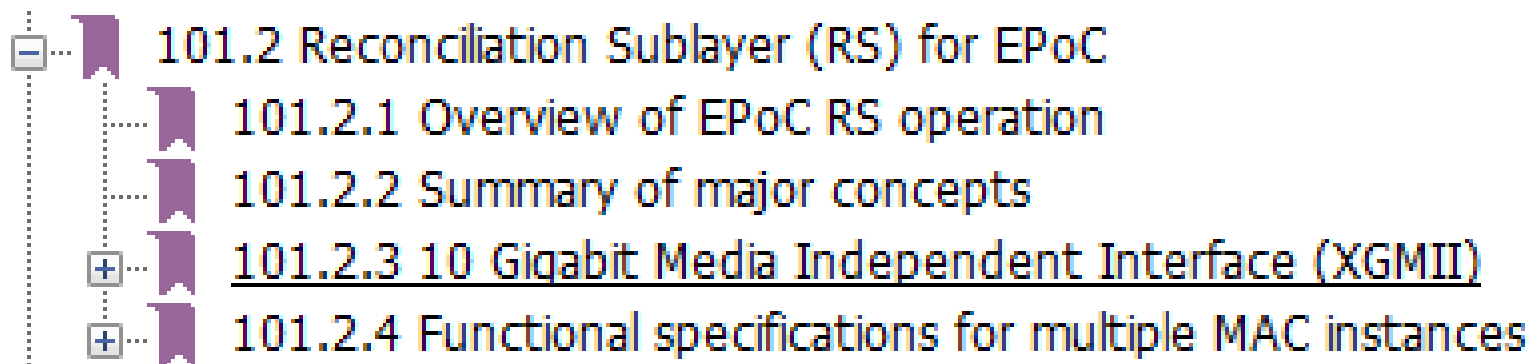
Accepted baselines (a)

- hajduczenia_3bn_01_0513.pdf covering technical decisions #43 and #45 (Idle Insertion and Idle Deletion processes)



Accepted baselines (b)

- hajduczenia_3bn_03_0513.pdf covering the definition of EPoC RS
 - Contribution into 101.2 was fairly complete
 - All subclauses within 101.2 are provided for and are ready for commenting

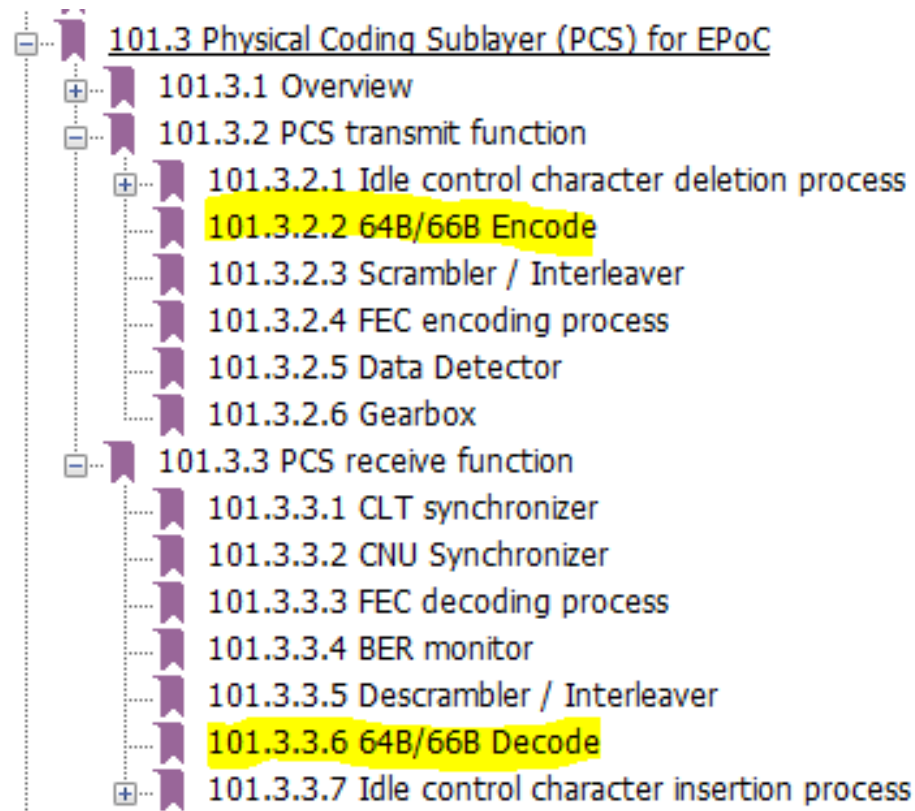


A table of contents for the 101.2 Reconciliation Sublayer (RS) for EPoC. It features a vertical dotted line on the left with icons: a minus sign in a square for the main section, and plus signs in squares for subclauses. Purple bookmark icons are placed to the right of the main section and to the left of each subclause. The subclause 101.2.3 is underlined.

[-]	101.2 Reconciliation Sublayer (RS) for EPoC
	101.2.1 Overview of EPoC RS operation
	101.2.2 Summary of major concepts
[+]	<u>101.2.3 10 Gigabit Media Independent Interface (XGMII)</u>
[+]	101.2.4 Functional specifications for multiple MAC instances

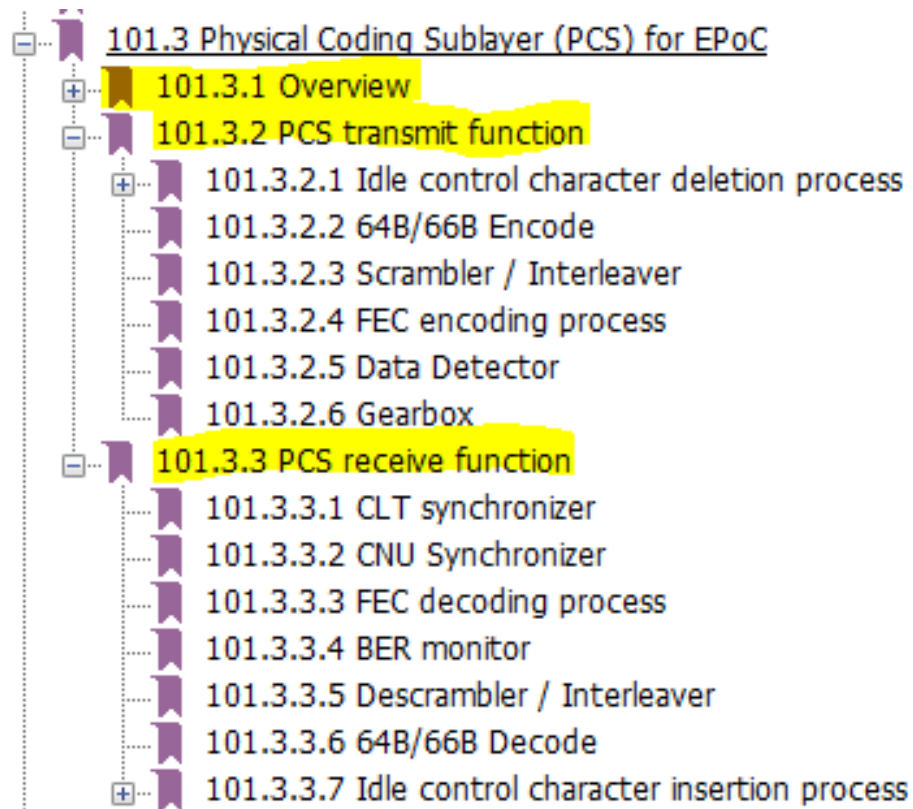
Accepted baselines (c)

- hajduczenia_3bn_04_0513.pdf covering the 64B/66B encode and decode processes (technical decision #20)



Accepted baselines (d)

- hajduczenia_3bn_06_0513.pdf covering the introduction text into 101.3 (PCS) and description of transmit and receive functions



Incoming contributions

- Here is the list of potential PCS-related baselines at this meeting:
 - CLT FEC encoder and CNU FEC decoder for FDD
- Other PCS-related contributions:
 - Discussion on data detector for TDD
 - PLC write-up (not sure where it really goes)

Status Summary

- Missing bit-ticket items
 - Data detector in CNU and CLT for FDD
 - Gearbox in Tx direction
 - Scrambler / Interleaver
 - Synchronizer in CNU and CLT
 - BER / FER monitor
 - TimeSync capability
 - Power Saving capability
- Big-ticket items under development
 - FEC (location, type, operation, etc.)
 - Data detector for TDD ?
- Missing discussion on aligning TDD and FDD PCS definitions into a single clause material (?)