

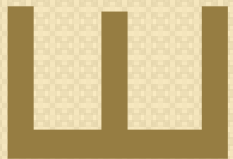
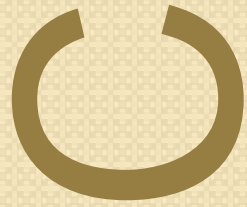


# EPoC PHY Link

A query & response protocol

# Agenda

- DS Frame Review
  - DS PHY Link frame
  - DS PHY Instruction
- US Frame Proposal
  - US PHY Link frame
  - US PHY Instruction Response
- Query Response protocol

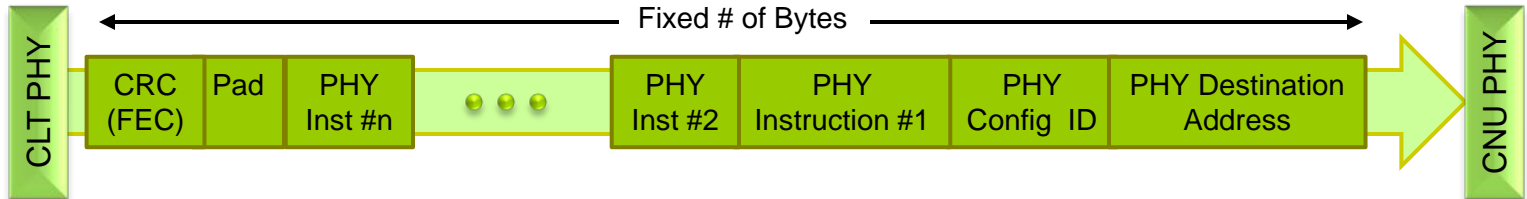


A review



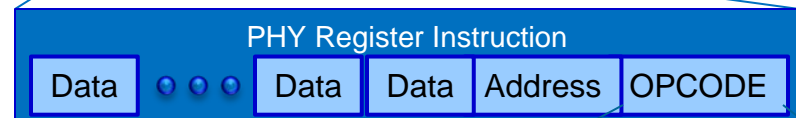
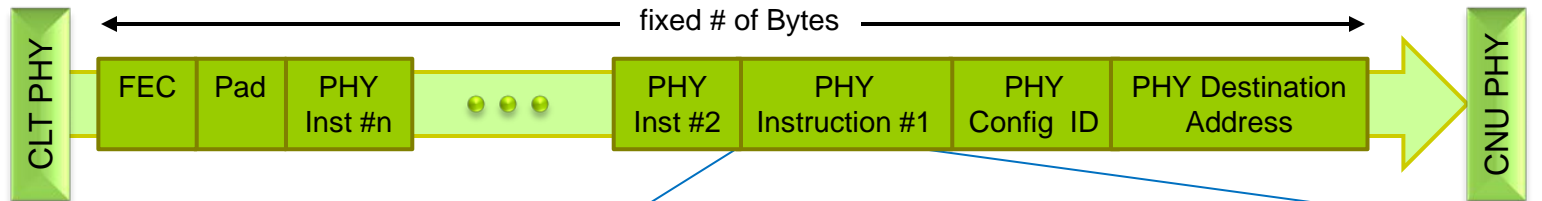
# **DS PHY FRAME & PHY INSTRUCTION**

# PHY Link Frame (DS)

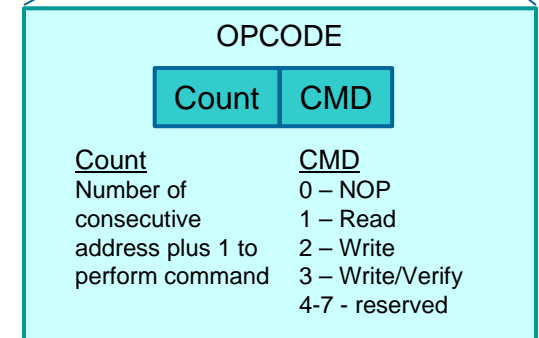


- A PHY Link Cycle will have one or more Downstream PHY Link Frames
- The PHY Link Frame will be a fixed size
- PHY Link Frame will contain a PHY Destination Address.
  - The MAC Address of the CNU maybe used as a PHY address.
  - CNU PHYs will receive instructions from the Broadcast Address or Unicast Address.
- The PHY Link Frame will contain a 2-bit PHY Configuration Identifier to allow for hitless switchover of select PHY configurations. (SP#10-11)
- The PHY Link Frame will contain one or more instructions to a remote PHY's registers.
- The PHY Link Frame may contain a CRC-? for error detection (TBD)
- The PHY Link Frame will contain forward error correction. (M#23)

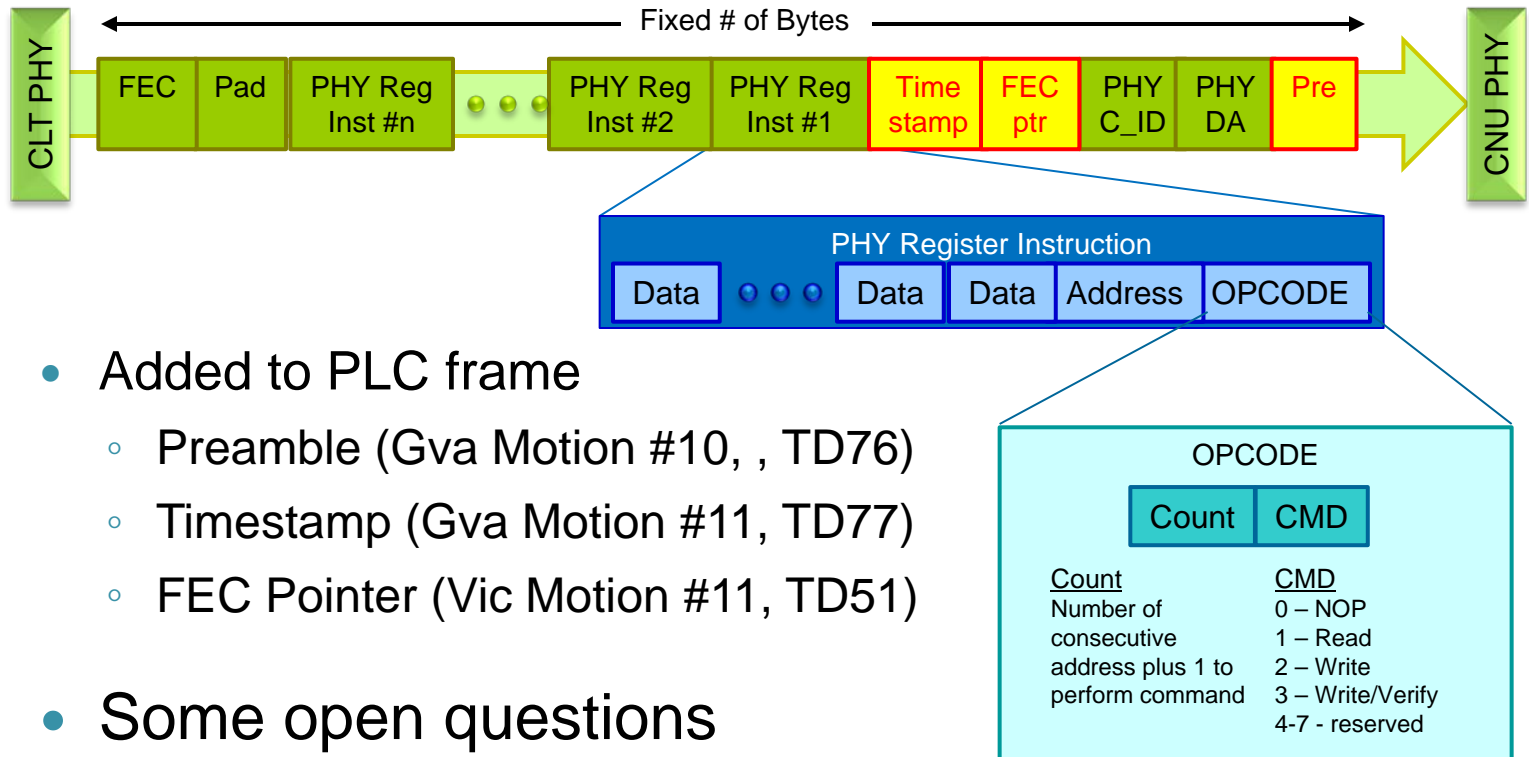
# PHY Link Frame (DS)



- PLC frame contains 1 or more PHY Instructions
- PHY Instruction is variable length based on the OPCODE used
- OPCODEs support reading & writing MDIO registers
- The write/read verify command allows for an acknowledged write
- Up to 32 consecutive addresses can be operated on with a single command
  - Example for writing 8 addresses in the PHY
    - With Consecutive Address: Opcode (1B) + Address (2B) + 8xWriteData (2B) = 19 Bytes
    - Without Consecutive Address: [Opcode (1B) + Address (2B) + WriteData(2B)] x 8 = 40 Bytes



# PHY Link Frame (DS)



- Added to PLC frame
  - Preamble (Gva Motion #10, , TD76)
  - Timestamp (Gva Motion #11, TD77)
  - FEC Pointer (Vic Motion #11, TD51)
- Some open questions
  - What does the US PLC frame look like?
    - Must be aligned with US OFDM frame
  - What controls access to US PLC?

# What about PHY Address?

- Do we really need 48 bits of DA?
  - Instead of 48b MAC address could use a 9-10b CNU ID (500-1000 end stations)
  - assigned to a CNU by the PHY on bring up
  - Used as DA
  - Include a few reserved values for broadcast addresses

# PHY\_Config & FEC\_Ptr

- As discussed in boyd\_3b\_02\_0513 (Victoria Motion #13) and boyd\_3b\_04\_0513 (Victoria motion #11)
  - PHY Config – 2 bits
  - FEC pointer – 16 bits
- Either could be part of frame overhead (every frame) or be in an MDIO register (transmitted as required)



# Timestamp

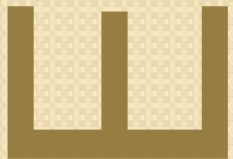
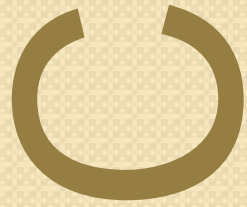
- Proposed in kilger\_3bn\_01b\_0713 but no details
- Proposal – see separate presentation

# PHY Instruction

- Proposed in several PHY Link calls
- 4 fields
  - OPCODE (8b)
    - Command sub-field(3b)
      - read, write, nop, write/verify
    - Register Count (5b)
      - the number of MDIO Register values included in this instruction
  - Register Address (16b)
    - the starting MDIO register address of this instruction
  - Register Data (n x 16b)
    - data to be written or as read from MDIO registers starting at the PHY Register Address, 0 to 31 possible registers

# FEC

- Selected in Geneva
  - LDPC (384,288)



A proposal

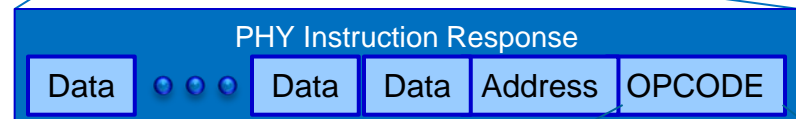
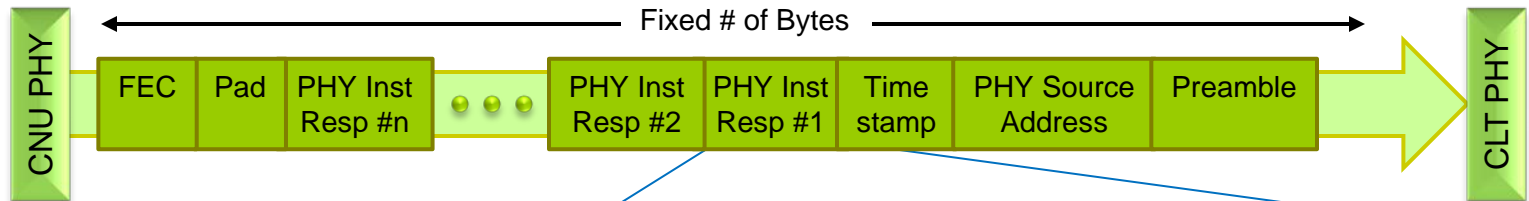


# **US PHY FRAME & PHY INSTRUCTION RESPONSE**

# Overview

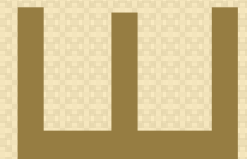
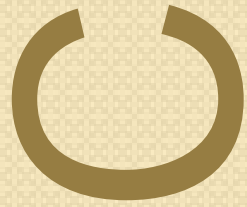
- Model after DS frame structure
  - Preamble
    - Need not be as large as DS (does not support a correlation protocol except during PHY Discover (see separate presentation))
    - Could we omit it totally?
    - Special preamble defined for initial ranging (see separate presentation)
  - Fixed header
    - SA – could use MAC address of CNU or some smaller CNU\_ID
    - Timestamp (tentative, see separate presentation)
    - Pad
    - FEC
  - PHY Instruction Response

# US PHY Link Frame



- Preamble (1 symbol?)
- Fixed header
  - PHY Source Address – could use MAC address or some shortened version
  - Timestamp
- PHY Instruction Response
  - OPCODE (8b) w/ two fields
    - ACK/NACK (3b) – acknowledgment (or not)
    - Count (5b) – same as in DS
  - Address – same as in DS
  - Data – same as in DS

OPCODE	
Count	ACK/NACK
Count	ACK/NACK
Number of consecutive address plus 1 to perform command	0 – NOP ACK 1 – Read ACK 2 – Write ACK 3 – Write/Verify ACK 4 – Read NACK 5 – Read NACK 6 – Write NACK 7 – Write/Verify NACK



# QUERY RESPONSE PROTOCOL

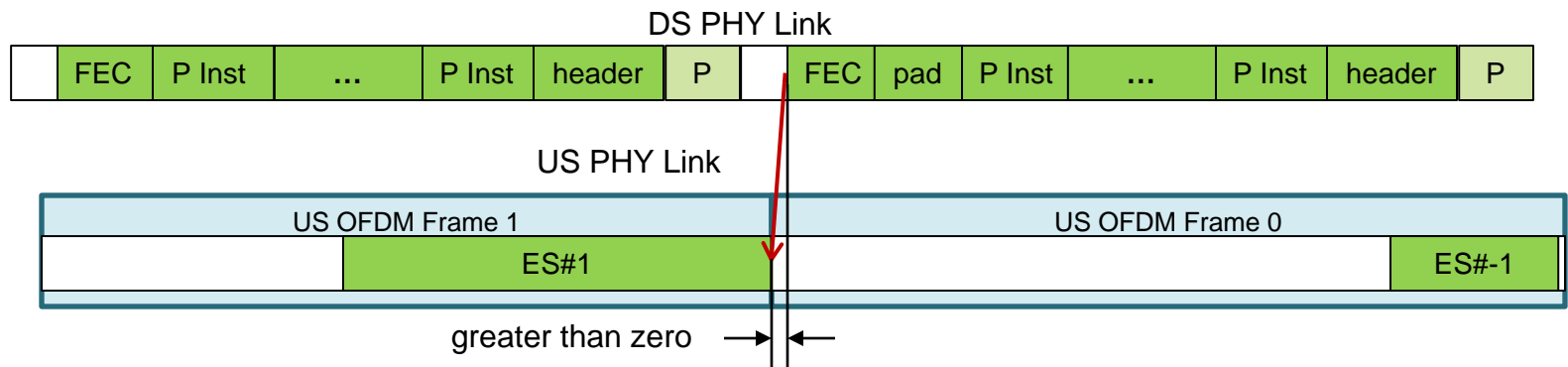
# Query Response

- One DA per PHY Register Instruction implies:
  - All instructions in a frame are directed to a single CNU (or possibly a group of CNUs for write instructions)
  - At most one responder
  - As long as RTT is less than PLC Frame time there is no issue



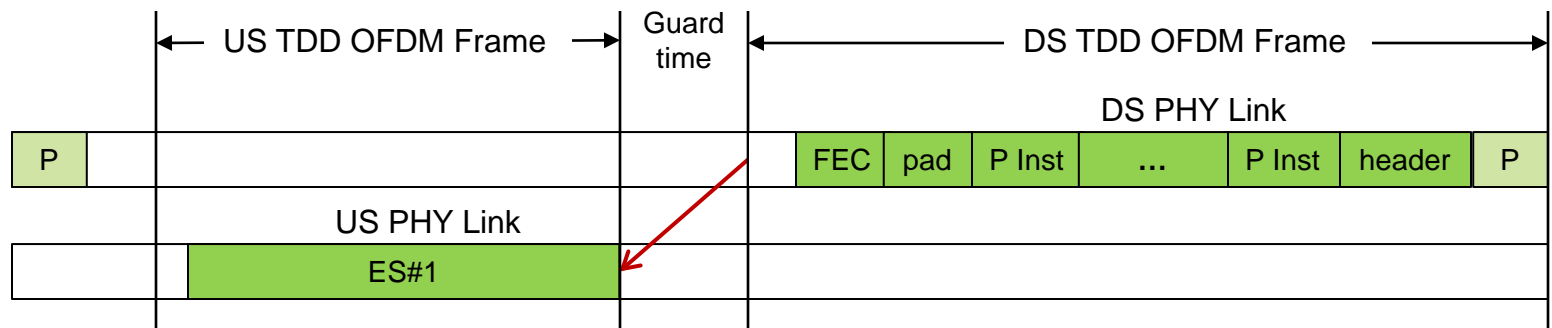
# Access to US PHY Link

- A Read or a Write/Verify instruction implies an US access opportunity
  - The instruction is clear about length (amount of data to transfer)
  - But when does it start?
- Assume it starts in the next US PHY-Link frame



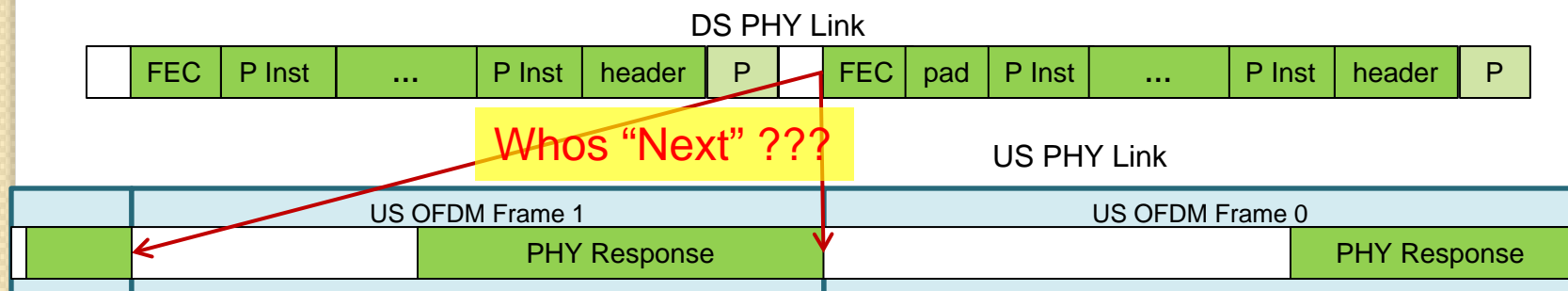
# Access to US PHY Link - TDD

- TDD case is simple as US/DS frames always have a well known phase relationship
- The CNU transmission starts in the next US OFDMA frame



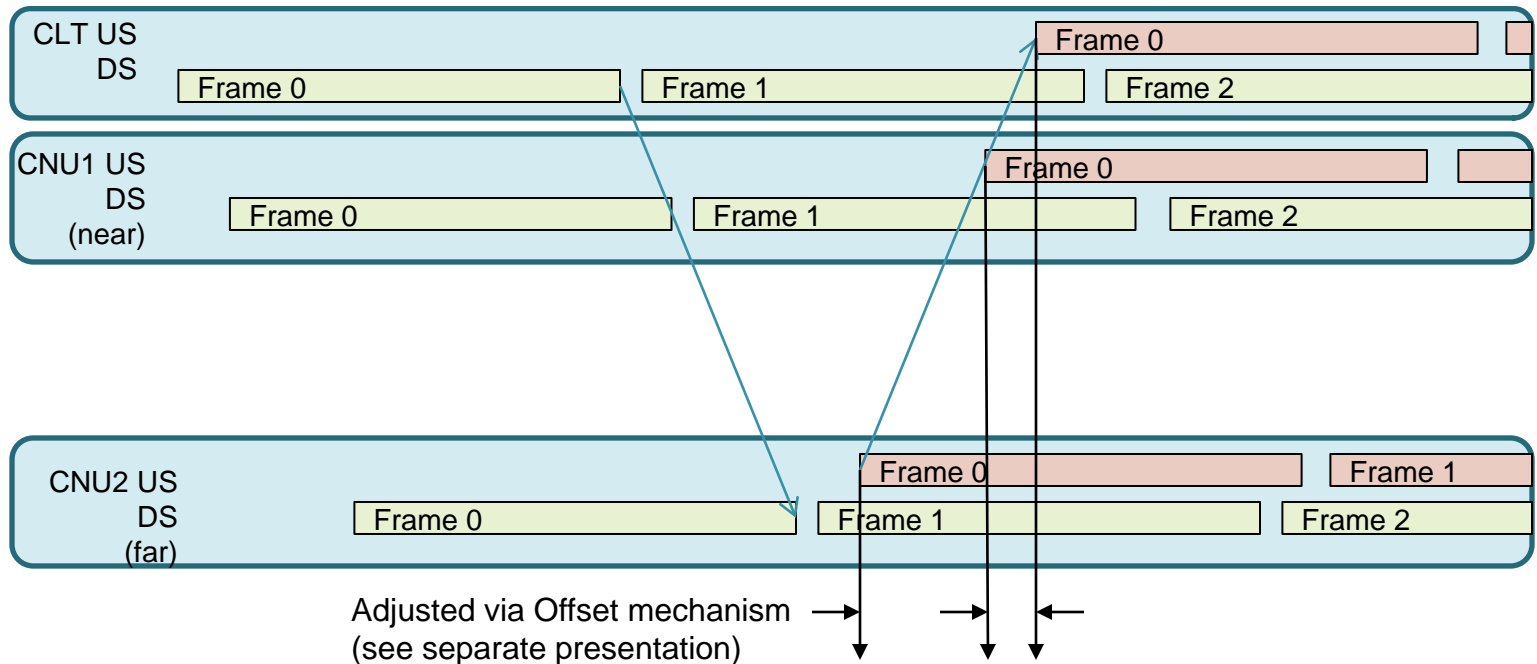
# Access to PHY Link - FDD

- But what if US/DS frames are closely aligned?
  - Could we force frame alignment?
    - Alignment at one CNU would not guarantee alignment at another
    - A new CNU could result in a new alignment
  - Should we include some positive indication of transmission time?



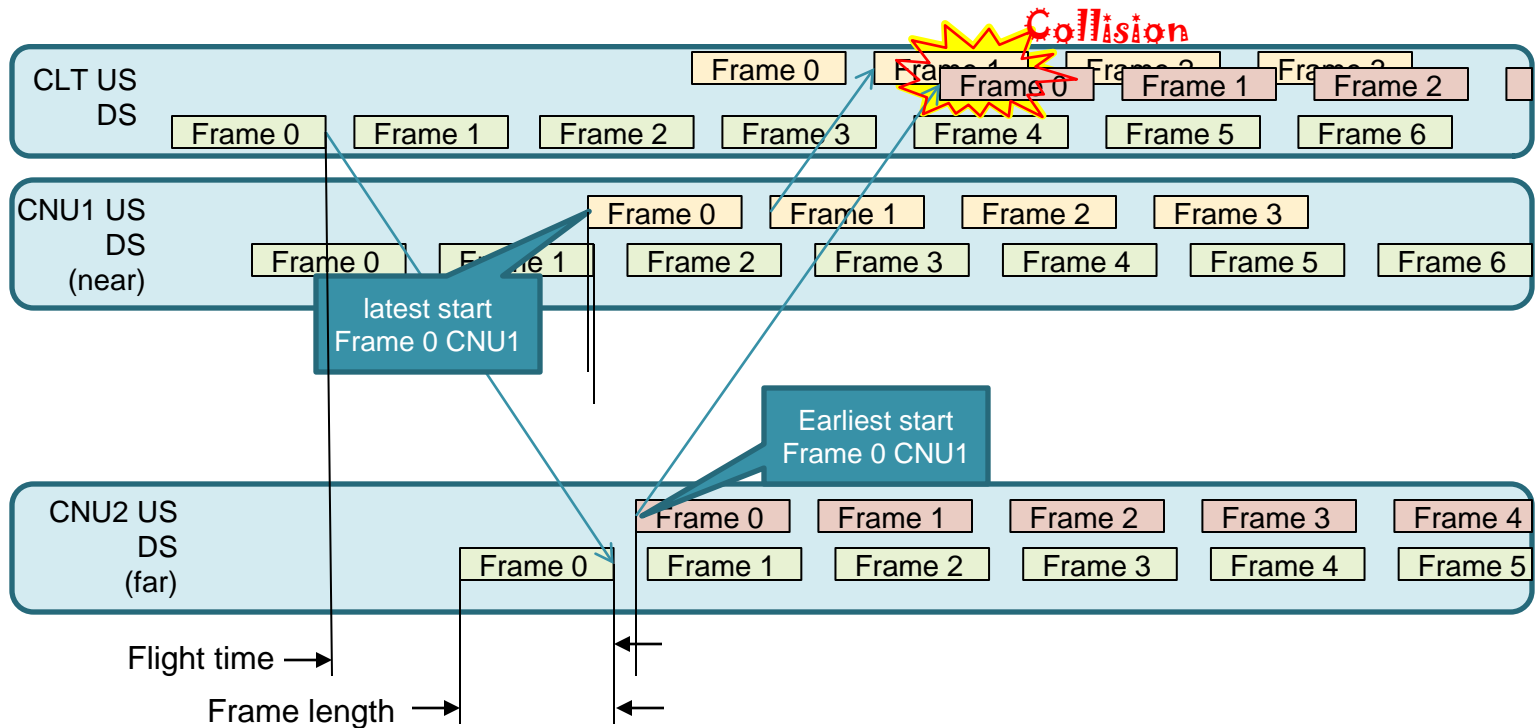
# PHY Frame length restrictions

- IF PHY Link frame is greater than flight time there is no issue



# PHY Frame length restrictions

- However, if the PHY Frame is less than the flight time (plus any PHY delay) then collisions can occur

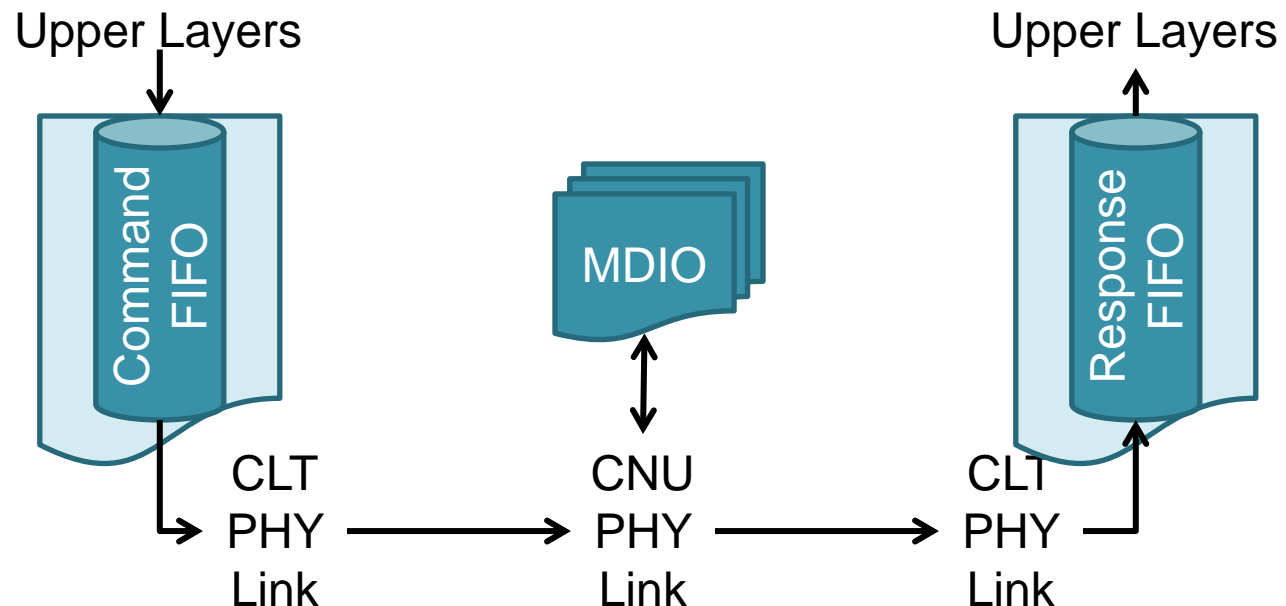


# Conclusions

- Unless some explicit response time is included in the DS PHY Link the PHY Frame time for FDD must be greater than the one way flight time plus any PHY Delay of the PHY Link path
- For FDD US and DS PHY Frames must be the same size
- These restrictions do not apply to TDD where it is assumed that the PHY Link frame is aligned with the TDD frame, in this case other restrictions apply

# How does PHY Link interact with upper layers?

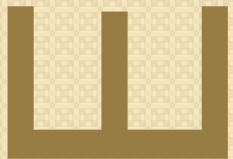
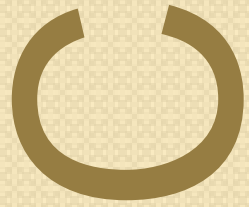
- This could be accomplished through a MDIO register space that emulates a command & response FIFO



# Command Response FIFO

- Command structure
  - OP CODE (8b)
  - DA
  - Data (0..31)
- Response structure
  - ACK/NACK (8b)
  - SA
  - Data (0..31)
- One MDIO Register indicating size remaining (in 16b words)





**THANK YOU**