97.5.2 Test modes

The test modes described below shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop and BER testing.

These test modes shall be enabled by setting a 3-bit control register as shown in Table 97–??. The test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

Table 97-?: MDIO management registers settings for test modes

0 0 0	Normal operation.
0 0 1	Test mode 1—Setting MASTER and SLAVE PHYs for transmit clock jitter test in normal mode.
0 1 0	Test mode 2—Transmit MDI jitter test in MASTER mode.
0 1 1	Reserved.
1 0 0	Test mode 4—Transmit distortion test.
1 0 1	Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
1 1 0	Test mode 6—Transmitter droop test mode.
1 1 1	Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

Test mode 1 enables testing of timing jitter on MASTER and SLAVE transmitters. MASTER and SLAVE PHYs are connected over a link segment defined in 97-7 (?). When in this mode, the PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK125. This 125 MHz test clock is one sixth frequency divided version of TX_TCLK that times the transmitted symbols.

Test mode 2 is for transmitter jitter testing on MDI when transmitter is in MASTER timing mode. When test mode 2 is enabled, the PHY shall transmit three {+1} symbols followed by three {-1} symbols continually with the transmitted symbols timed from its local clock source of 750MHz. The transmitter output is a 125MHz signal.

Test mode 3 is not defined and the corresponding register is reserved for future use.

Test mode 4 is for transmitter linearity testing. When test mode 4 is enabled, the PHY shall transmit the sequence of symbols generated by the following scrambler generator polynomial:

$$g(x) = 1 + x^9 + x^{11}$$

The maximum-length shift register used to generate the sequences defined by this polynomial shall be updated once per symbol interval (1/750MHz). The bits stored in the shift register delay line at a particular time *n* are denoted by $Scr_n[10:0]$. At each symbol period the shift register is advanced by one bit and one

new bit represented by $Scr_n[0]$ is generated. Bits $Scr_n[8]$ and $Scr_n[10]$ are exclusive OR'd together to generate the next $Scr_n[0]$ bit. The bit sequences $x0_n$, $x1_n$ and $x2_n$ generated from combinations of the scrambler bits as shown in the following equations, shall be used to generate the ternary symbols, $T0_n$ and $T1_n$, as shown in Table 97–??. The transmitter shall time the transmitted symbols from a 750MHz ± 0.01% clock in the MASTER timing mode. The transmit signal level and spectral shaping in this mode shall be same as normal operation mode. A typical transmitter output for transmitter test mode 4 is shown in Figure 97–??.

$$x0_n = Scr_n[0]$$
$$x1_n = Scr_n[1] \wedge Scr_n[4]$$
$$x2_n = Scr_n[1] \wedge Scr_n[5]$$

Table 97-?: Transmit test mode 4 symbol mapping

$x2_n$	$x1_n$	$x0_n$	$T1_n$	$T0_n$
0	0	0	-1	-1
0	0	1	0	-1
0	1	0	-1	0
0	1	1	-1	+1
1	0	0	+1	0
1	0	1	+1	-1
1	1	0	+1	+1
1	1	1	0	+1

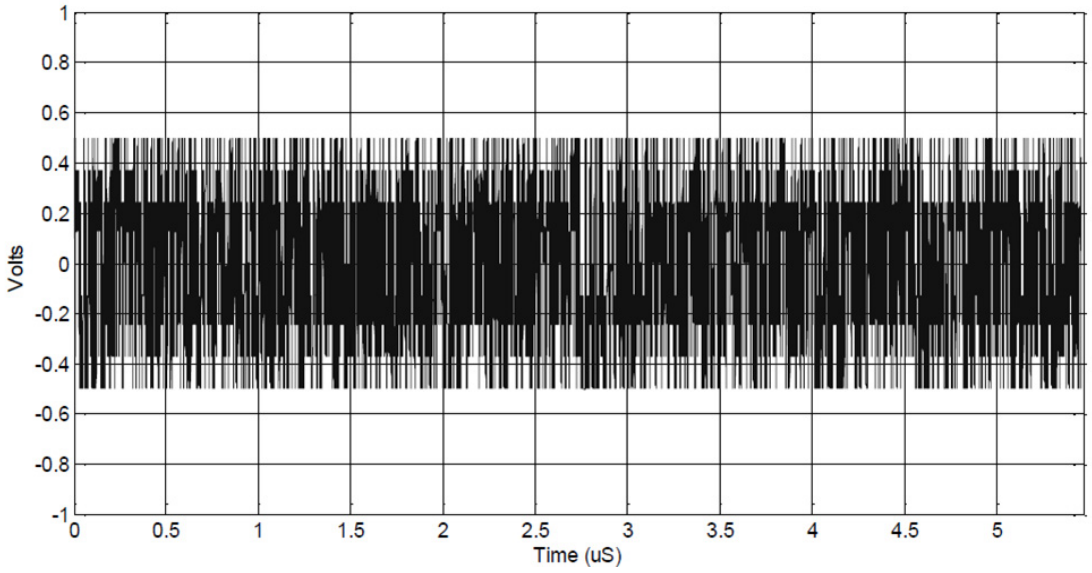

Figure 97-xx: Example of Transmitter Test Mode 4 waveform (1 cycle)

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, the PHY shall transmit as in normal operation and in MASTER data mode with data set to zero.

Test mode 6 is for testing transmitter droop. When test mode 6 is enabled, the PHY shall transmit fifteen {+1} symbols followed by fifteen {-1} symbols continually with the transmitted symbols timed from its local clock source of 750MHz. The transmitter output is a 25MHz signal

Test mode 7 is for enabling measurement of the bit error ratio of the link including the FEC encoder/ decoder, transmit and receive analog front ends of the PHY and a cable connecting two PHYs. This mode reuses the 1000BASE-T1 normal mode with zero data pattern. Instead of encoding received data from MAC, continuous zero data pattern is encoded. In the receive side, after FEC and 80/81 decoding, zero data sequence is expected with no error. Any no zero data bit received is counted as error and calculated in BER.

97.5.2.1 Test fixtures

The following fixtures, or their equivalents, as shown in Figure 97-??, Figure 97-??, Figure 97-??, Figure 97-??, and Figure 97-??, in stated respective tests, shall be used for measuring the transmitter specifications for data communication only. The tolerance of resistors shall be +/- 0.1%.

In figure 97-??, the sinusoidal disturbing signal Vd, shall have amplitude of 3.6 volts peak-to-peak differential, and frequency given by one-sixth of the symbol rate (125MHz) synchronous with the test pattern. The generator of the disturbing signal must have sufficient linearity and range so it does not introduce any appreciable distortion when connected to the transmitter output.

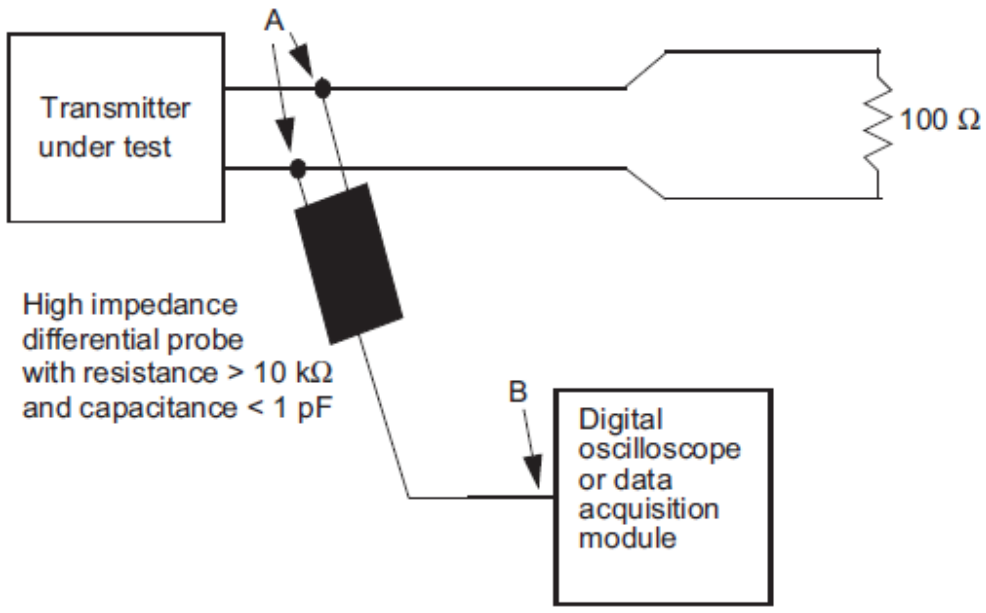

Figure 97-??: Transmitter test fixture 1 for transmitter droop measurement

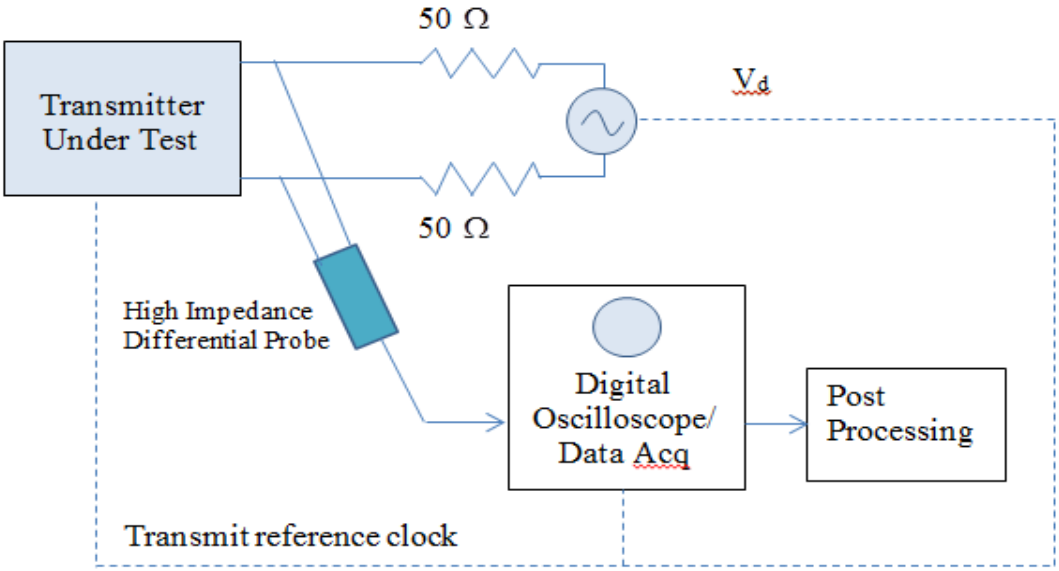

Figure 97-??: Transmitter test fixture 2 for transmitter distortion measurement

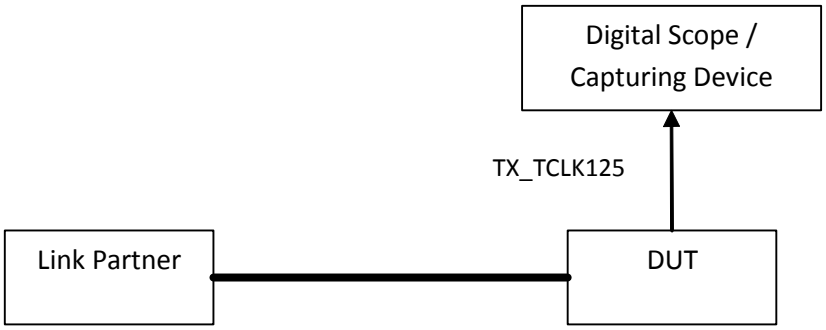

Figure 97-??: Transmitter test fixture 3 for MASTER and SLAVE clock jitter measurement

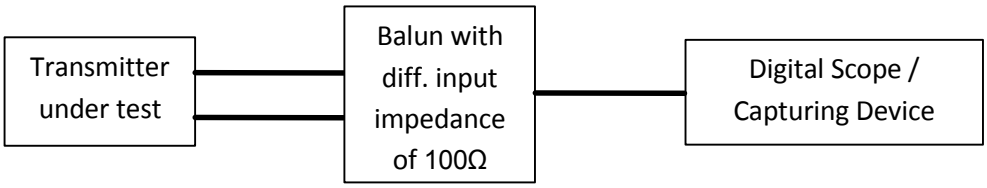

Figure 97:??: Transmitter test fixture 4 for MDI jitter measurement

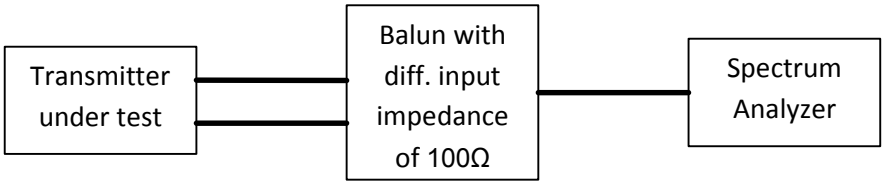

Figure 97-??: Transmitter test fixture 5 for power spectral density measurement and transmit power level measurement

97.5.3 Transmitter electrical specifications

The PMA provides the Transmit function specified in 97.4.2.2 (?) in accordance with the electrical specifications of this clause. The PMA shall operate with AC coupling to the MDI. Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100Ω resistive differential load connected to the transmitter output.

97.5.3.1 Maximum output droop

With the transmitter in test mode 6 and using the transmitter test fixture 1, the magnitude of both the positive and negative droop shall be less than 50%, measured with respect to an initial value at 4ns after the zero crossing and a final value at 16ns after the zero crossing. (12ns period)

97.5.3.2 Transmitter distortion

Transmitter distortion is measured by capturing the test mode 4 waveform using transmitter test fixture 2. The peak distortion is determined by sampling the differential signal output with the symbol rate clock at an arbitrary phase and processing a block of consecutive samples with MATLAB code given below or an equivalent. The captured block of signal shall be at least 40us long with 10 times the transmit symbols rate (7.5Gs/s).

The peak distortion values, measured at a minimum of 10 equally-spaced phases of a single symbol period, shall be less than 10mV. Notice the peak signal level is normalized to 1V in the processing code. The MATLAB code removes the sinusoidal disturbing signal from the measured data and computes the peak distortion. The code assumes the disturber signal and the data acquisition clock are frequency locked to the DUT transmit clock.

```
% Post processing MATLAB code for 1000BASE-T1 transmitter distortion
clear
Ns=2^11-1; % Scrambler length
Nc=70;  % Canceler length

% Generate scrambler sequence
scr=ones(Ns,1);
for i=12:Ns
  scr(i)=mod(scr(i-11) + scr(i-9),2);
end
```

```
% 1000BASE-T1 2D-PAM3 assignment
tm4=ones(Ns,1);
map=[-1 -1;-1 0;0 -1;1 -1;0 1;-1 1;1 1;1 0];
scr3=[mod(circshift(scr,1) + circshift(scr,5),2), ...
      mod(circshift(scr,1) + circshift(scr,4),2),scr];
data = 4*scr3(:,3)+ 2*scr3(:,2)+scr3(:,1);
for n=1:length(data)
       tm4([2*n-1,2*n]) =map(data(n)+1,:);
end
Ns=2*Ns;

% Test mode4 matrix
for i=1:Nc
    X0(i,:)=circshift(tm4,1-i);
end

% Read captured data file, 40us long, 7.5GSample/sec, high resolution capture
fid=fopen('RawData.bin','r');
tx = fread(fid,inf,'double');
fclose(fid);

% LPF 375MHz
[A,B]=butter(2,1/10,'low');
tx=filter(A,B,tx);

% HPF 12MHz
tx = filter([1,-1],[1,-exp(-2*pi/625)],tx);

% Select six periods, 10x oversampling, a row vector
tx=tx((1:6*Ns*10)+2e3)'; % removes HPF transient

% Disturber removal and integration (average) of six periods
TX=fft(tx);
tx=ifft(TX(1:6:end));

% Level normalization to 1V
tx=tx/(max(tx)-min(tx))*2;

% Compute distortion for 10 clock phases
for n=1:10
tx1=tx(n:10:end);

% Align data and test pattern
temp=xcorr(tx1,tm4);
index=find(abs(temp)==max(abs(temp)));
X=circshift(X0, [0, mod(index(1)+Nc-10,Ns)]);

% Compute coefficients that minimize squared error
coef=tx1/X;

% Linear canceller
err=tx1-coef*X;
```

```
% Peak distortion
dist(n) = max(abs(err));
end

% Print distortion in mV (normalized) for 10 sampling phases
format bank
peakDistortion_mV = 1000*dist'
```

97.5.3.3 Transmitter timing jitter

Transmitter timing jitter is measured by capturing TX_TCLK125 waveform for both MASTER and SLAVE while in test mode 1 using transmitter test fixture 3 shown in figure 97-??.

When in test mode 1 and the link is up and the two PHYs are in the normal mode of operation, the RMS value of the MASTER TX_TCLK125 jitter relative to an un-jittered reference shall be less than 5ps. The Peak-to-Peak value of the MASTER TX_TCLK125 jitter relative to an un-jittered reference shall be less than 50ps.

When in test mode 1 and the link is up and the two PHYs are in the normal mode of operation, the RMS value of the SLAVE TX_TCLK125 jitter relative to an un-jittered reference shall be less than 10ps. The Peak-to-Peak value of the SLAVE TX_TCLK125 jitter relative to an un-jittered reference shall be less than 100ps.

TX_TCLK125 jitter shall be measured over an interval of 1ms+/-10%. The band-pass bandwidth of the capturing device shall be larger than 2MHz. Un-jittered reference is a constant clock frequency extracted from each record of captured TX_TCLK125. The un-jittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

For PHYs supporting LPI mode, in order for the transmit jitter to be similar to normal operation, the clock reference used to clock transmit-symbols shall be continuous going from normal mode into and out of LPI mode.

In addition to jitter measurement for transmit clock, MDI jitter is measured when in test mode 2 and using test fixture 4 as shown in Figure 97.??. The RMS value of the MDI output jitter relative to an un-jittered reference shall be less than 5ps. The Peak to Peak value of the MDI output jitter relative to an un-jittered reference shall be less than 50ps. Jitter shall be measured over an interval of 1ms+/-10%. The band-pass bandwidth of the measurement device shall be larger than 2MHz. Un-jittered reference is a constant clock frequency extracted from each record of captured differential output on MDI. The un-jittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

97.5.3.4 Transmitter Power Spectral Density (PSD) and power level

In test mode 5 (normal operation with no power back-off), the transmit power shall be less than 5dBm and the power spectral density of the transmitter, measured into a 100Ω load using the test fixture 5 shown in Figure 97–?? shall be between the upper and lower masks specified in Equations (97–??) and (97–??). The masks are shown graphically in Figure 97–??. The measurements need to be calibrated for insertion loss of the differential Balun used in the test. Resolution bandwidth of 100KHz and sweep time of larger than 1s are considered in PSD measurement.

$$UpperPSD(f)) = \begin{cases} -80 & \text{dBm/Hz} & 0 < f_{\text{MHz}} \le 100 \\ (-76 - f_{\text{MHz}}/25) & \text{dBm/Hz} & 100 < f_{\text{MHz}} \le 400 \\ (-86 - f_{\text{MHz}}/62.5) & \text{dBm/Hz} & 400 < f_{\text{MHz}} \le 600 \end{cases}$$

$$LowerPSD(f)) = \begin{cases} -86 & \text{dBm/Hz} & 40 < f_{\text{MHz}} \le 100 \\ (-86 - f_{\text{MHz}}/25) & \text{dBm/Hz} & 100 < f_{\text{MHz}} \le 400 \end{cases}$$

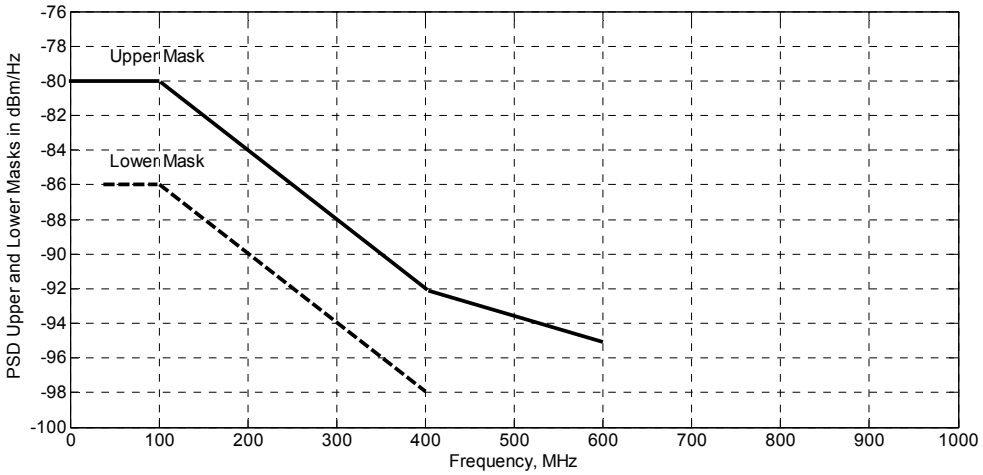

Figure 97-??: Transmitter Power Spectral Density, Upper and Lower Masks