MDI Return Loss Limit Proposal for 1000BASE-T1

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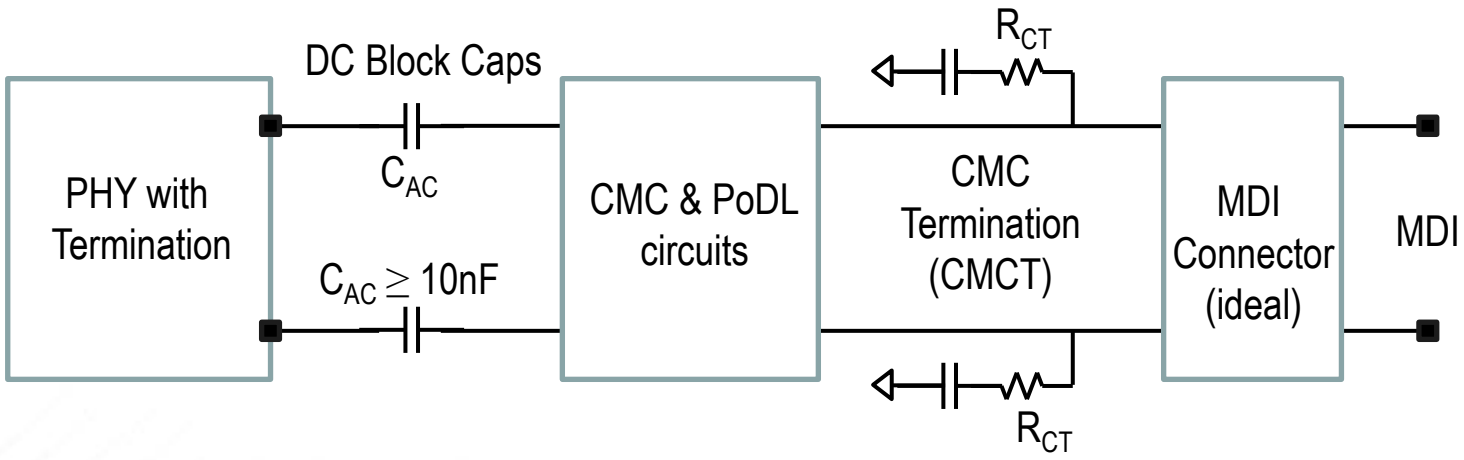
Why do we care about the MDI Return Loss (RL)?

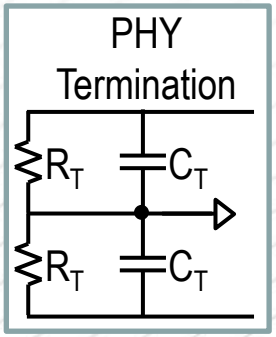
- Finite RL necessitates digital echo cancellation
  - Increased signal processing cost
- Excessive echo reduces effective ADC dynamic range
  - Lower SNR and shorter cable reach
- High freq. echo amplifies jitter to noise conversion
  - Lower SNR and shorter cable reach
  - Slower timing recovery and longer startup
- Serial reflections cause system resonance
  - Degraded driver stability
  - More DM/CM conversions

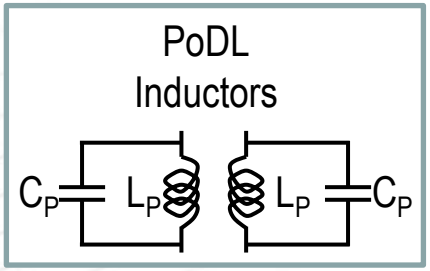
What are the imperfections causing reflections?

- PHY
  - Parasitics from driver output, ESD diodes, and routings
  - On-chip termination variations with process and temperature
- PoDL (see chini_3bp_02_1114.pdf)
  - Parasitic coupling between inductor turns and grounds
  - Finite inductance and variation with temperature and power
- CMC
  - Parasitic DC resistance, skin effects, etc.
  - Parasitic inductance due to differential mismatch
- UTP
  - Impedance variation with process, material, temperature, etc.

An MDI model for simulating the return loss

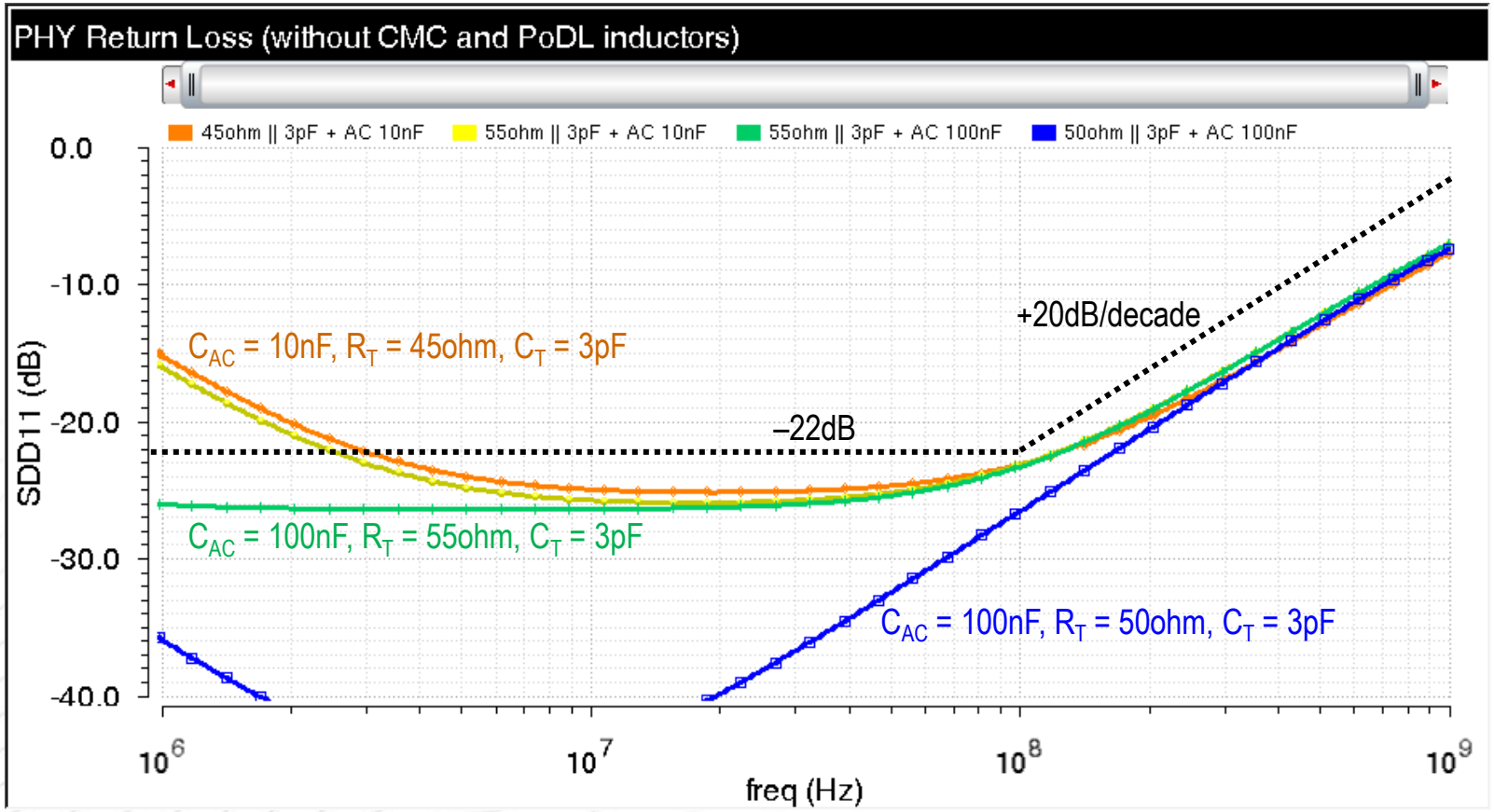




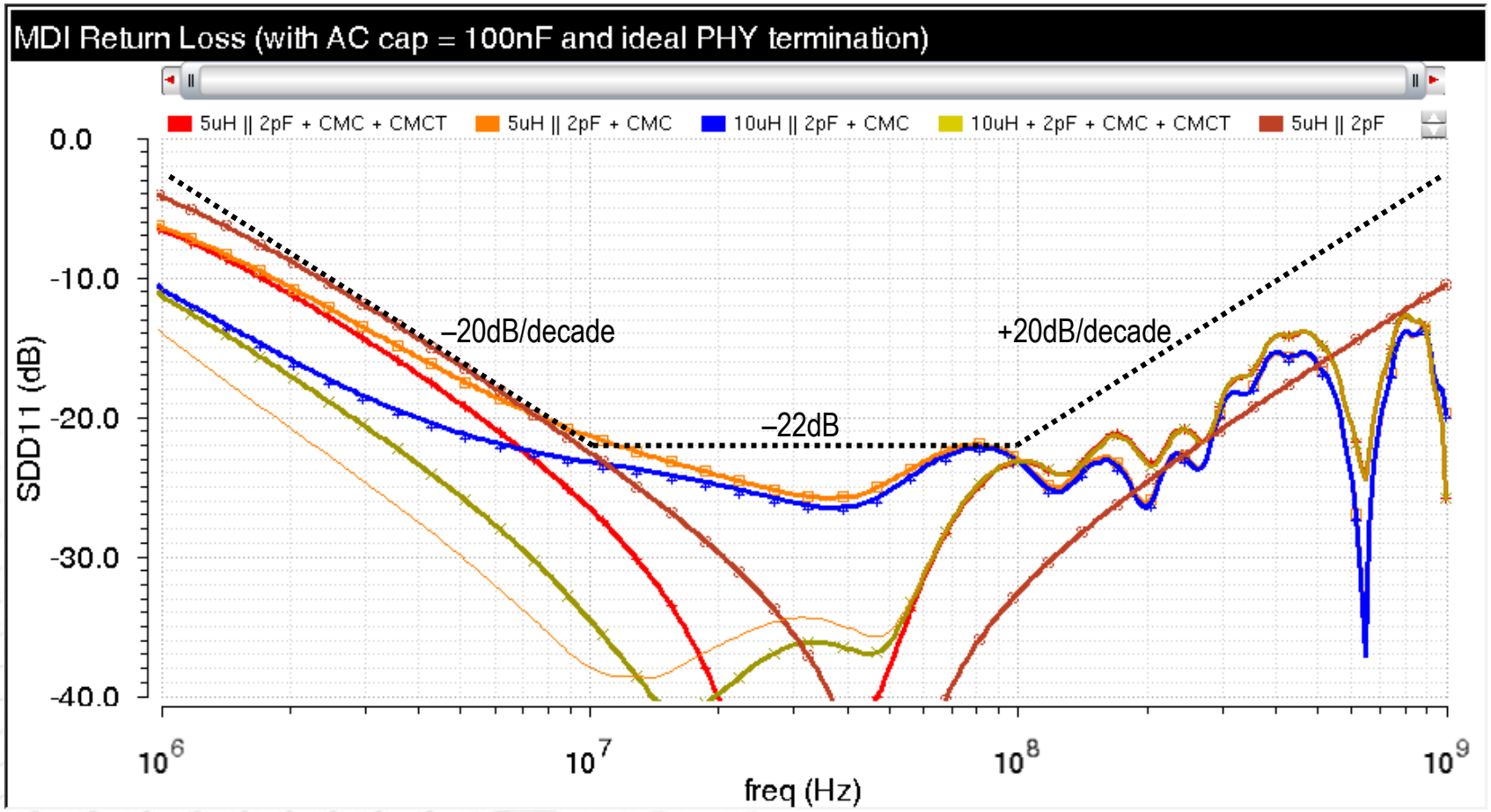


		min	nom	max
R_T	Ω	45		55
C_T	pF		3	5
L_P	µH	5	10	30
C_P	pF	1		2

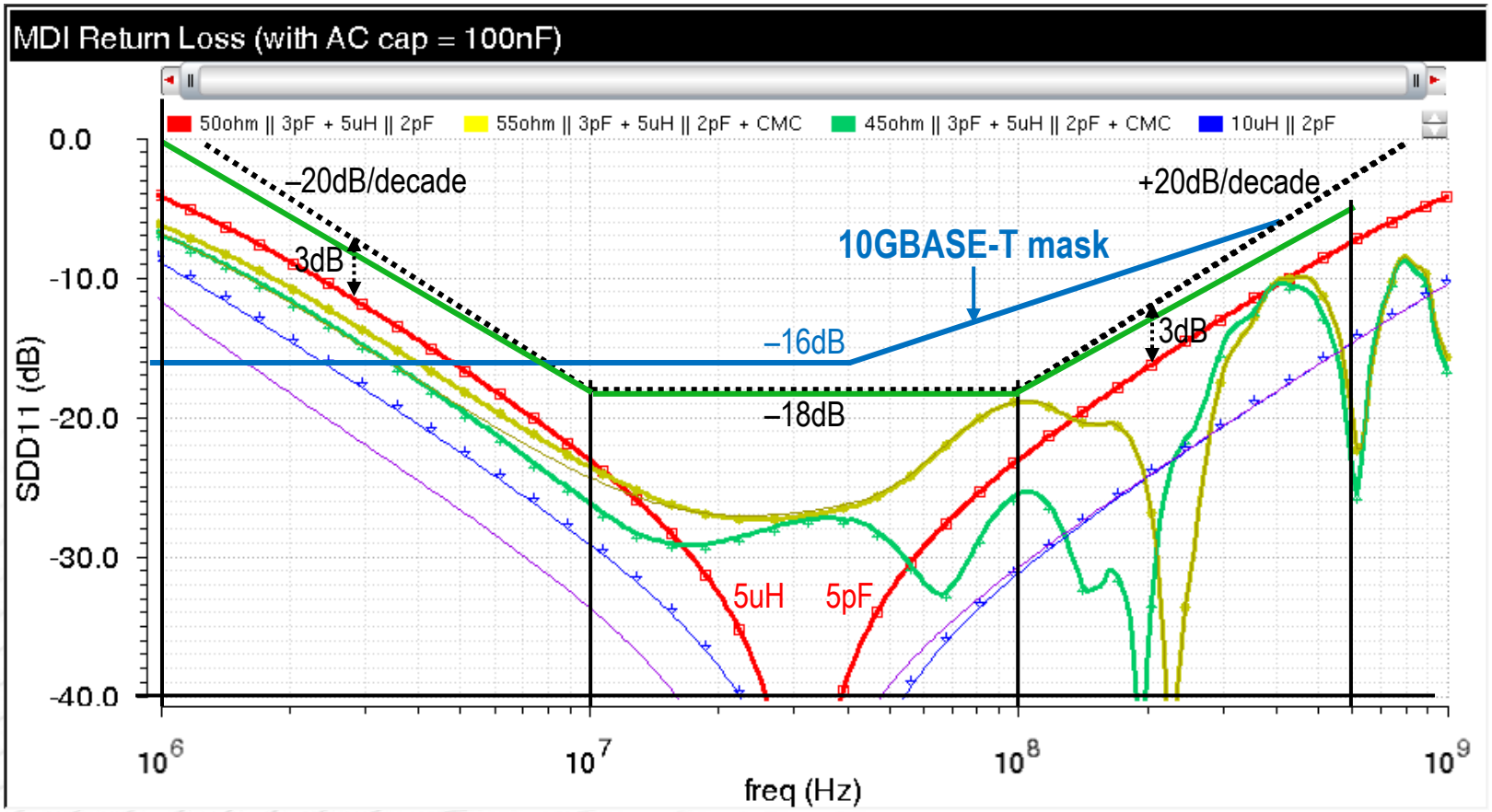
How is the RL affected by on-chip (PHY) imperfections?



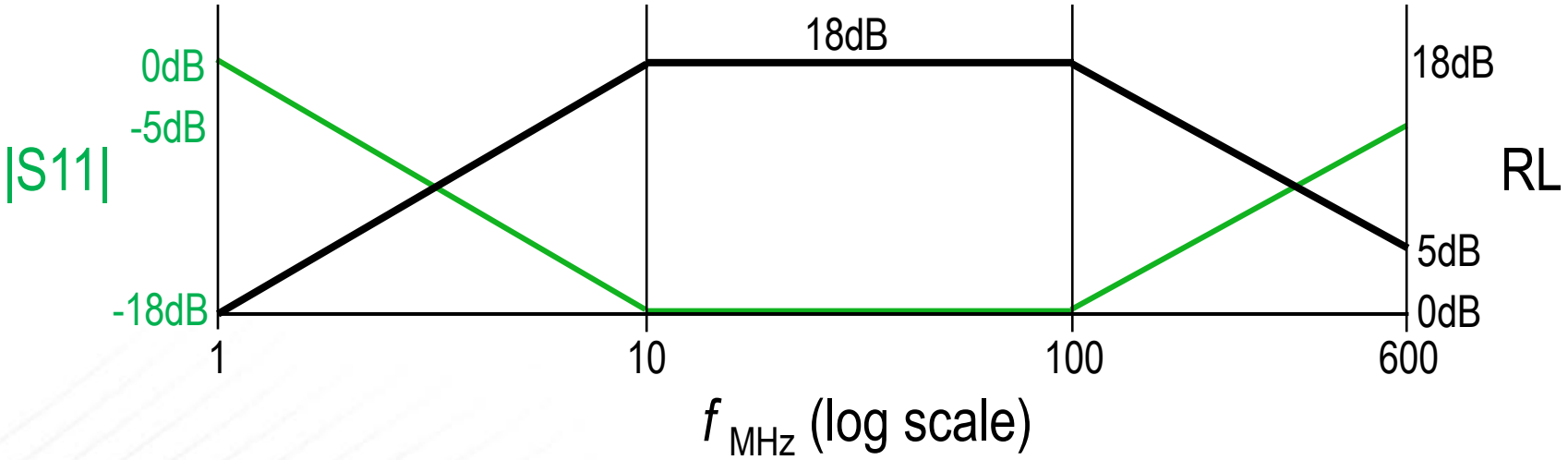
How is the RL affected by off-chip (PoDL+CMC) imperfections?



How is the RL affected by the overall imperfections?



Proposed MDI Return Loss (|S11|) Limit



$$\text{Return Loss} \geq \begin{cases} 18 - 18\log_{10}(10/f_{MHz}) & \text{(dB)} & 1 \leq f_{MHz} \leq 10 \\ 18 & \text{(dB)} & 10 < f_{MHz} \leq 100 \\ 18 - 16.7\log_{10}(f_{MHz}/100) & \text{(dB)} & 100 < f_{MHz} \leq 600 \end{cases}$$

Conclusions

- The PoDL inductors and the capacitive parasitics dominate the RL roll-off at low and high frequencies, respectively.
- ±10% termination impedance variations and the CMC parasitics set max mid-freq. RL to 18dB for f from f_L = 10MHz to f_H =100MHz.
- An MDI RL limit is proposed that rolls off from 18dB beyond (f_L, f_H) with ~2dB margin at Nyquist for 5uH PoDL inductance and 5pF capacitance.
- The proposal is a reasonable tradeoff between cost and performance:
  - The 5uH minimum PoDL inductance, a total of 5pF parasitic capacitance, and ±10% total impedance variations are feasible at reasonable cost.