Encoder / FEC / PAM3 Proposal

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Agenda

- Propose a uniform way for everyone to calculate latency
- Propose several RS options with 11-bit to 7-PAM3 symbol mapping
- Compare against other proposed mapping
- Conclusions and recommendation

Latency Definitions

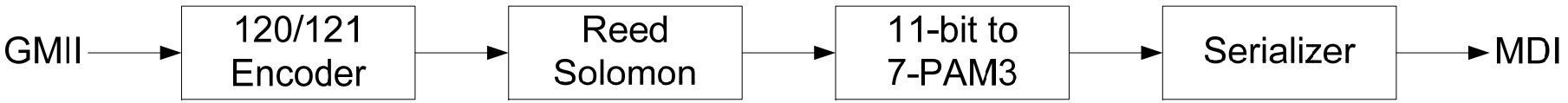
- **Algorithmic Latency**
  - Amount of time waiting to collect data before algorithm can be applied
    - Aggregate data in 8N/(8N+1) encoder
    - RS TX data delay to avoid underflow
    - RS RX frame aggregation
- **Implementation Latency**
  - Circuit latency
    - Pipelining, FIFOing
    - RS parity computation
    - RS Error correction
    - DSP processing
    - Circuit propagation delays
- **Total Latency = Algorithmic + Implementation for round trip**
  - GMII → TX → RX → GMII

Algorithmic Latency

- Assume implementation latency = 0 since it is vendor dependent
- Algorithmic latency is the minimum theoretical latency
- Definitions
  - Y = bytes in 8Y/(8Y + 1) encoder
  - RS(N, K, 2^M): N frame symbols, K data symbols, M bits per symbol
  - P = S-PAM3 /T-bits Number of PAM3 symbols / RS bit (i.e. 7/11, 2/3, 7/10)
  - R = Baud rate in ns (i.e. 750 MHz is 1.3333ns)
- Algorithm Delay = A + B + C + D + E + F
  - A = 8Y/(8Y + 1) encoder = 8 x Y x 1ns
  - B1 = RS encoder underflow prevention (no interleaving) = (N-K) x M x P x R
  - B2 = RS encoder underflow prevention with 1 interleave = 2 x B1
  - C = Bit to PAM3 conversion = 0 since data delayed in B1 or B2
  - D = PAM3 to bit conversion = S x R
  - E1 = RS decoder frame aggregation (no interleaving) = N x M x P x R
  - E2 = RS decoder frame aggregation with 1 interleave = 2 x E1
  - F = (8Y + 1)/8Y decoder = 0 since data delayed in E1 or E2

Proposed encoder options

- **Uses 120/121 Encoder**
  - 8N/(8N+1) N = 15
  - Lo_3bp_02_0314,pdf, Lo_3bp_01_0514.pdf
- **Reed Solomon FEC**
  - For 100ns, 200ns, 400ns, 800ns burst correction (double for erasure correction)
  - At 700MHz, 725MHz, 750 MHz
- **11-bit to 7 PAM3 symbols**
  - liu_3bp_01a_0314.pdf, liu_3bp_01_0714.pdf
  - Can be alternate mapping as long as bandwidth preserved



Boundary Condition

- **11 bit RS symbols for all options**
  - 7 PAM3 symbols completely map into one 11-bit RS symbol
  - No need to gray code PAM3 mapping since all 7 PAM3 symbols are protected as one
- **Self Contained FEC block**
  - Exactly 700/725/750 MHz with no padding
  - Integer number of 120/121 blocks
  - Integer number of 11-bit to 7-PAM3 symbol mapping

Reed Solomon Options – Main proposal

Baud Rate (MHz)	n	k	n - k	FEC Block (ns)	Correction (ns)	Algorithmic Latency (ns)	# 120/121 blocks	# 11 to 7
700	240	220	20	2400	100.0	2730.0	20	240
700	480	440	40	4800	200.0	5330.0	40	480
700	960	880	80	9600	400.0	10530.0	80	960
700	1920	1760	160	19200	800.0	20930.0	160	1920
725	261	231	30	2520	144.8	2939.3	21	261
725	435	385	50	4200	241.4	4812.4	35	435
725	783	693	90	7560	434.5	8558.6	63	783
725	1479	1309	170	14280	820.7	16051.0	119	1479
750	180	154	26	1680	121.3	2052.0	14	180
750	360	308	52	3360	242.7	3974.7	28	360
750	630	539	91	5880	420.0	6858.7	49	630
750	1260	1078	182	11760	849.3	13588.0	98	1260

Other PAM3 Mapping: 3-bit to 2 PAM3, 9-bit RS symbol

- **N = 10 (80/81 encoder)**

Baud Rate (MHz)	n	k	n - k	FEC Block (ns)	Correction (ns)	Algorithmic Latency (ns)	# 80/81 blocks	# 3 to 2
700	672	> 511, Not a Solution			102.9			
700	1344	> 511, Not a Solution			205.7			
700	2632	> 511, Not a Solution			402.9			
700	5264	> 511, Not a Solution			805.7			
725	377	351	26	3120	107.6	3417.9	39	1131
725	725	> 511, Not a Solution			206.9			
725	1421	> 511, Not a Solution			405.5			
725	2813	> 511, Not a Solution			802.8			
750	270	243	27	2160	104.0	2458.7	27	810
750	510	459	51	4080	200.0	4570.7	51	1530
750	1020	> 511, Not a Solution			408.0			
750	2010	> 511, Not a Solution			800.0			

Other PAM3 Mapping: 3-bit to 2 PAM3, 12-bit RS symbol

- **N = 10 (80/81 encoder)**

Baud Rate (MHz)	n	k	n - k	FEC Block (ns)	Correction (ns)	Algorithmic Latency (ns)	# 80/81 blocks	# 3 to 2
700	504	486	18	5760	102.9	6048.6	72	2016
700	1008	972	36	11520	205.7	12014.3	144	4032
700	1960	1890	70	22400	400.0	23282.9	280	7840
700	3920	3780	140	44800	800.0	46482.9	560	15680
725	290	270	20	3200	110.3	3503.4	40	1160
725	551	513	38	6080	209.7	6582.1	76	2204
725	1073	999	74	11840	408.3	12739.3	148	4292
725	2117	1971	146	23360	805.5	25053.8	292	8468
750	210	189	21	2240	106.7	2546.7	28	840
750	390	351	39	4160	202.7	4658.7	52	1560
750	780	702	78	8320	416.0	9234.7	104	3120
750	1500	1350	150	16000	800.0	17682.7	200	6000

Other PAM3 Mapping: 10-bit to 7 PAM3, 10-bit RS symbol

- **N = 14 (112/113 encoder)**

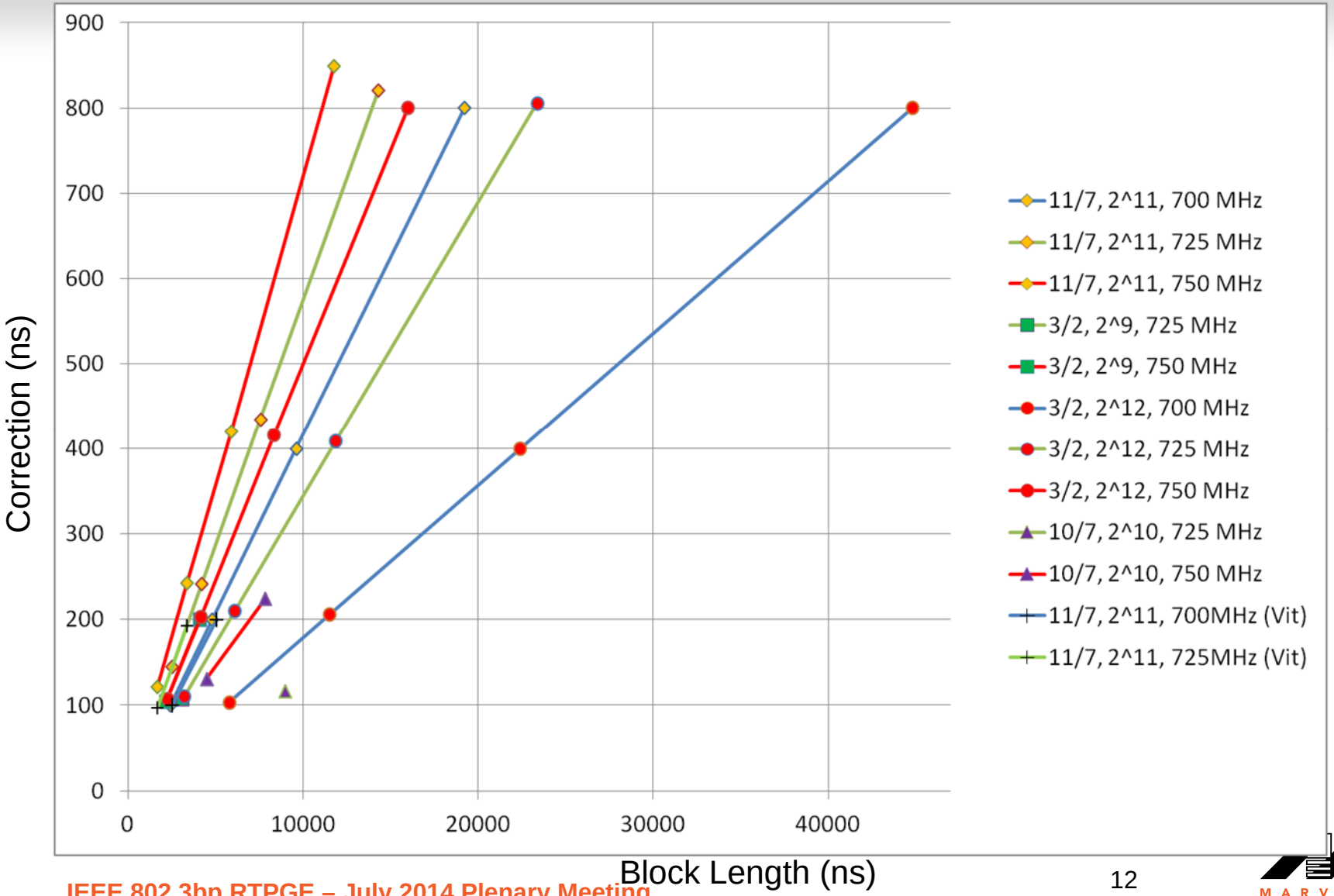
Baud Rate (MHz)	n	k	n - k	FEC Block (ns)	Correction (ns)	Algorithmic Latency (ns)	# 112/113 blocks	# 10 to 7
700	Impossible, PAM3 conversion is already 700MHz							
725	928	904	24	8960	115.9	9313.4	80	928
725	1624	> 1023, Not a Solution			202.8			
725	3248	> 1023, Not a Solution			405.5			
725	6496	> 1023, Not a Solution			811.0			
750	480	452	28	4480	130.7	4862.7	40	480
750	840	791	49	7840	224.0	8418.7	70	840
750	1560	> 1023, Not a Solution			420.0			
750	3000	> 1023, Not a Solution			812.0			

With Interleave: 11-bit to 7 PAM3, 11-bit RS symbol

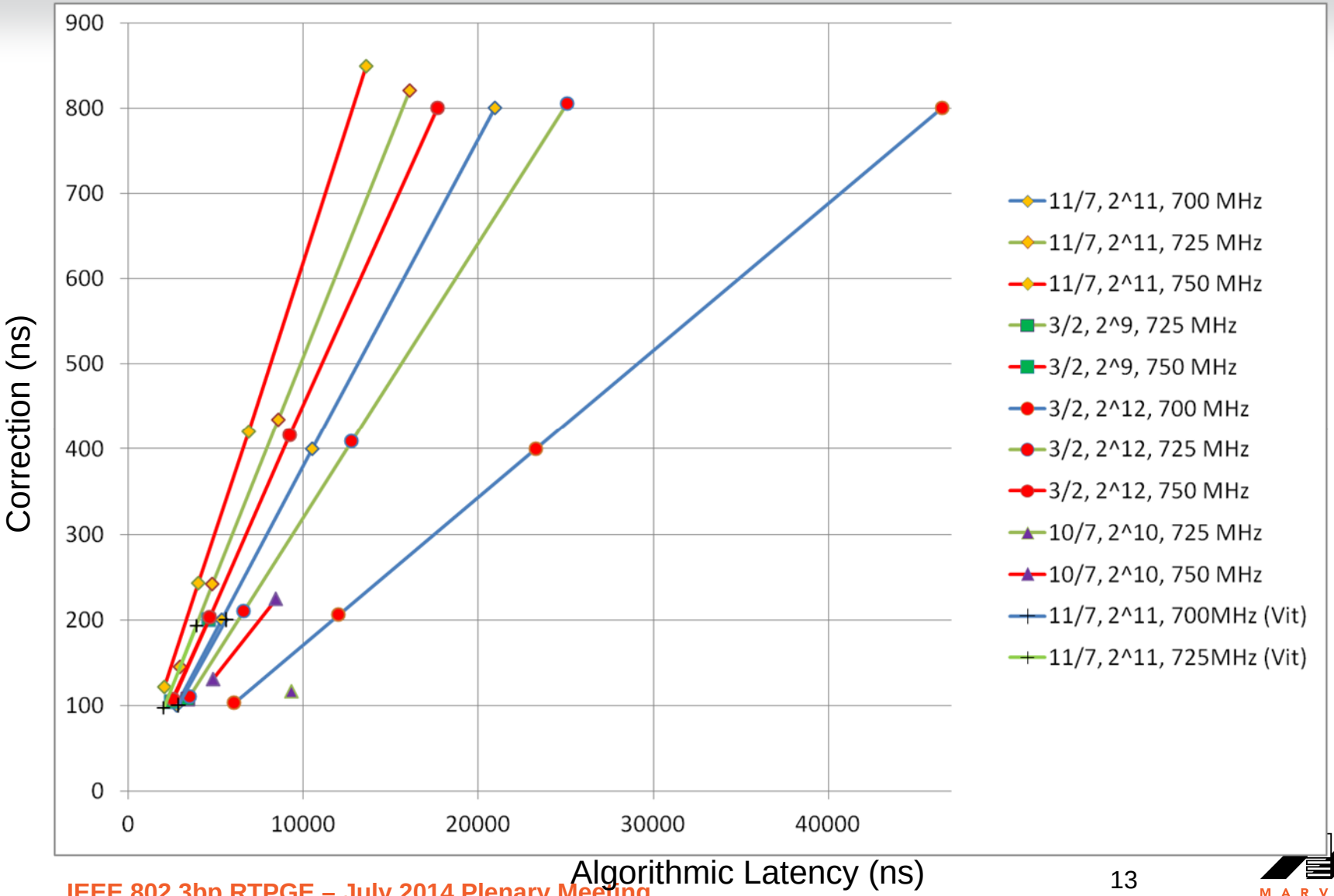
- **100 ns no interleave, 200 ns with interleave, header padding**

Baud Rate (MHz)	n	k	n - k	FEC Block (ns)	Correction (ns)	Algorithmic Latency (ns)	# 120/121 blocks	# 11 to 7
700	251	231	20	2520	100.0	2850.0	21	251
700	251	231 (interleaved)	20	5040	200.0	5570.0	42	502
700		Not proposed			400.0			
700		Not proposed			800.0			
725	174	154	20	1680	96.6	2002.8	14	174
725	174	154 (interleaved)	20	3360	193.1	3875.9	28	348
725		Not proposed			400.0			
725		Not proposed			800.0			
750		Not proposed			100.0			
750		Not proposed			200.0			
750		Not proposed			400.0			
750		Not proposed			800.0			

Comparison Summary Correction vs. Block Length



Comparison Summary Correction vs. Algorithmic Latency



Conclusions

- 11-bit to 7-PAM3 symbol mapping yields shortest latency at a fixed correction duration and baud rate
- Higher baud rate yields shorter latency at a fixed correction duration
- With flexible 8N/(8N+1) encoder it is possible to find RS parameters that exactly fit into 25MHz friendly baud rate for all proposed PAM3 mapping schemes
- Can use chart on slide 12 and 13 to extrapolate latency vs. correction for the 3 baud rates.
  - RS codes can be tuned to meet correction requirements

Marvell's Recommendation

- **Pick 750 MHz**
  - Semiconductor companies can find ways to reduce power
  - But cannot overcome algorithmic latency once baked in
- **Pick 11-bit to 7-PAM3 mapping**
  - Most bandwidth efficient and lowest latency
- **Pick RS(360, 308, 2^{11})**
  - FEC block time 1680 ns
  - Algorithmic Latency 3975 ns
  - 242 ns correction
  - 485 ns erasure

THANK YOU

BACKUP

Other possible options at 750MHz

Baud Rate (MHz)	n	k	n - k	FEC Block (ns)	Correction (ns)	Algorithmic Latency (ns)	# 120/121 blocks	# 11 to 7
750	180	154	26	1680	121.3	2052.0	14	180
750	270	231	39	2520	177.3	3013.3	21	270
750	360	308	52	3360	242.7	3974.7	28	360
750	450	385	65	4200	298.7	4936.0	35	450
750	540	462	78	5040	364.0	5897.3	42	540
750	630	539	91	5880	420.0	6858.7	49	630
750	720	616	104	6720	485.3	7820.0	56	720
750	810	693	117	7560	541.3	8781.3	63	810
750	900	770	130	8400	606.7	9742.7	70	900
750	990	847	143	9240	662.7	10704.0	77	990
750	1080	924	156	10080	728.0	11665.3	84	1080
750	1170	1001	169	10920	784.0	12626.7	91	1170
750	1260	1078	182	11760	849.3	13588.0	98	1260