IEEE 802.3bp 1000BaseT1

- 1. Stream FEC Proposal
- 2. Latency Model Proposal



VITESSE

Making next-generation networks a reality.

Tom Brown March 2014

IEEE 802.3bp 1000BaseT1 Task Force - March 2014

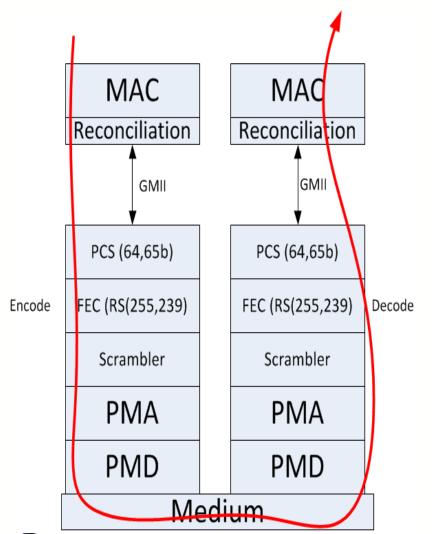
Agenda

- Stream FEC Proposal
 - Layered View
 - Encoding
 - Decoding
 - Benefits
- Latency Background
 - Proposed Latency Model
 - Latency Standards IEEE RFC2544, key parameters
 - Latency Recommendations





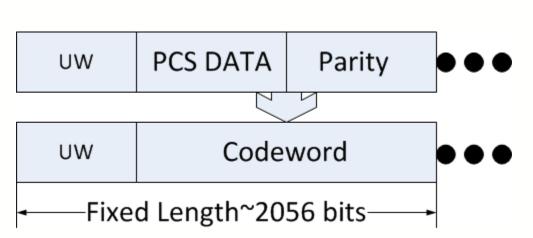
Stream FEC Proposal



- Layered Model
 - ▶ FEC is shim between PCS and Scrambler
- ▶ FEC computes parity over N blocks of PCS words.
- ▶ The parity and synchronization Unique Word are inserted into the bit stream
- ➤ Similar model to 10G EPON and 802.3ba (100G Ethernet)



Stream FEC Encoding\Decoding



Encoding

- PCS blocks are collected to fill the info field of the codeword, padded as necessary, and parity is calculated and inserted into the bit stream.
- A Unique Word- is used for synchronization purposes and coupled with a fixed length stream is used to provide a robust synchronization method in a noisy environment. A UW length of 16 bits may be sufficient, avoiding falsing by taking fixed length into account.

Decoding

- UW and fixed length allows for error tolerant synchronization
- DATA and Parity are run through decoder
- Corrected data is handed back to the PCS layer as though nothing had happened.





Stream FEC Benefits, Other considerations

Benefits

- All Ethernet Data and PCS special characters are protected equally
- ▶ FEC sublayer is unaware of Ethernet Frame boundaries and special codes
- ▶ Simple mechanism and used by 10G EPON, IEEE 802.3ba
- Low overhead

Other considerations

- Rate adjustment (assumed required)
 - Adjust clocks to account for overhead to maintain 1G thruput
- Clocking scheme and tolerances must be worked out
- UW and Synchronization needs to be worked out





Latency Background

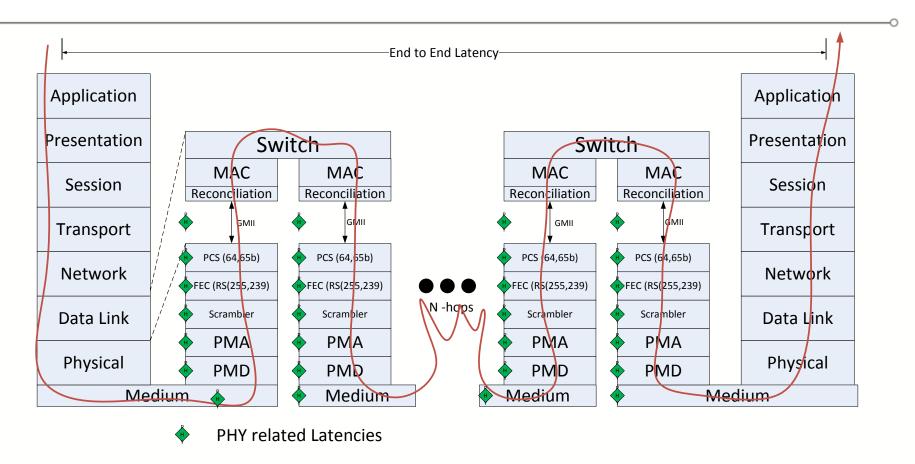
Background

- ▶ During the FEC talk at Indian Wells, OEMs were asking about Latency in the PHY especially when we talked about interleaving over multiple frames. The discussion on the reflector after the meeting was an "apples to oranges" discussion. I was talking about FEC decoder delay and the OEMs rolled up the latency requirements from the an "End to End" multi-hop application.
- ▶ "End to End" latencies cross the PHY and MAC boundaries, plus other layers.
- 1000BaseT1 can only specify requirements for layers we control
- ▶ Latency (end-to-end) is a very important topic for OEMs, so I recommend we work out a plan for a top down latency method to budget our "1000BaseT1" layers and specify worst case numbers with some margin for MFGr differentiation.





Latency model



- ▶ OEMs talk latency at Application layer, "End to End", like measured in RFC2544.
 - 1000BaseT1 can only speak to layers we are defining.



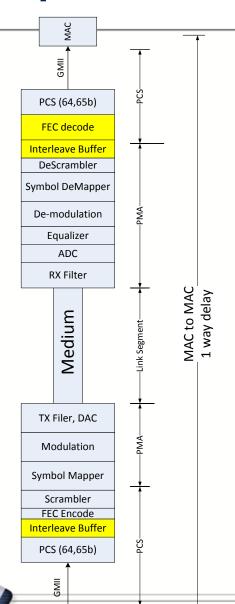
Latency according to RFC2544

- ▶ IEEE RFC2544 provides an industry accepted method for measuring latency for store and forward devices.
- ▶ Latency is either one-way or round trip time (RTT).
 - One way is often quoted as RTT/2 because it can be measured from one clock.
- ▶ RFC2544 stipulates frame size testing with
 - ▶ 64,128,256,512,1024,1280, and 1518 bytes
- Other methods to measure latency
 - Netperf, Ping Pong



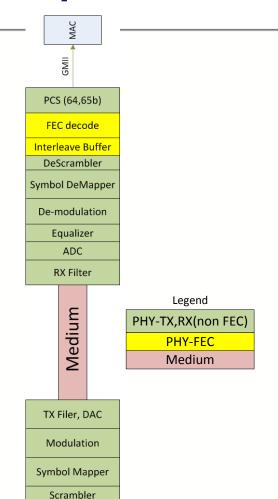


Proposed PHY Latency Model



- MAC to MAC one way model
 - ▶ PHY Layers consist of many sub-blocks, many of which have low latencies < 20 BT (bit times)
 - ▶ FEC Buffering, Interleaving, decoding will dominate the latency in the PHY, >90% of latency.
 - We are not trying to make a fixed latency PHY
 - Mfgrs. will have different solutions to various layers making tradeoffs between power, area, latency targeting their customers.

Proposed PHY Latency Model



- ▶ Lump latency into 3 areas
 - ▶ PHY (non FEC related), TX, RX
 - PHY- FEC related
 - Medium
- Specify Max Latencies for each area
 - Use units of Bit Times (BTs)
- ▶ Medium use 802.3 Table 42-4

Excerpt from 802.3 Table 42-4 Conversion Table for Cable Delay:

Speed		
relative		
to c	ns/meter	BT/meter
0.4	8.34	8.34
0.5	6.67	6.67
0.6	5.56	5.56
0.7	4.77	4.77
0.8	4.17	4.17

FEC Encode
Interleave Buffer
PCS (64,65b)

Proposed PHY Latency Model

Example (Interleave=1)	Min	Max
PHY (non FEC related)	-	500
FEC - Interleave	-	2040
FEC -Deinterleave	-	2040
FEC -Decode	-	1000
Medium (assume speed=0.7*c, 15m)	-	72
Total Latency (BTs)		5652

	Latency	Model	Examp	les
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- ► Showing Interleave factor = 1,2
- ► The FEC related latencies dominate the overall PHY latency

Example (Interleave=2)	Min	Max
PHY (non FEC related)	-	500
FEC - Interleave	-	4080
FEC -Deinterleave	-	4080
FEC -Decode	-	1000
Medium (assume speed=0.7*c, 15m)	-	72
Total Latency (BTs)		9732

Decode latency is another area where tradeoffs in power, area, latency can be made to differentiate features.



Latency recommendations

- ▶ Agree on a model for latency specification for 1000BaseT1 and the layers we control.
- ▶ Socialize this model with OEMs (when complete). Agree on which methods and\or tools will be used to model latency for "End-End".
- ▶ Based on the Latency model for the PHY that we agree upon, and knowing the latency test methodology used to "end to end" measurements and the key parameters, specify in 1000BaseT1, the worst case latencies based on packet sizes that the OEMS will be using.

