45 Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Editor to insert registers in this section into table 45-3

45.2.1.(X) BASE-T1 PMA Control Register (Register 1.2304)

The assignment of bits in the BASE-T1 control register is shown in Table 45–YY0.

Table 45-YY0 –BASE-T1 PMA Control Register

Bit(s)	Name	Description	R/W
1.2304.15	Reset	1 = PMA/PMD reset 0 = Normal operation	R/W SC
1.2304.14:12	Reserved	Set to 0s	R/W
1.2304.11	Low power	1 = Low-power mode 0 = Normal operation	R/W
1.2304.10:5	Reserved	Set to 0s	R/W
1.2304.4	Master/Slave	1 = Master 0 = Slave	R/W
1.2304.3:0	PHY Type	BASE-T1 PHY speed when Auto-negotiation is disabled 0000 = Reserved 0001 = Reserved 0010 = 1000BASE-T1 Else = Reserved	R/W

45.2.1.(X).1 BASE-T1 Reset (1.2304.15)

Resetting a PMA/PMD is accomplished by setting bit 1.2304.15 to a one. This action shall set all PMA/PMD registers to their default states. As a consequence, this action may change the internal state of the PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a PMA/PMD shall return a value of one in bit 1.2304.15 when a reset is in progress; otherwise, it shall return a value of zero. A PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.2304.15. During a reset, a PMD/PMA shall respond to reads from register bits 1.2304.15 and 1.8.15:14. All other register bits should be ignored.
NOTE—This operation may interrupt data communication.

45.2.1.(X).2 BASE-T1 Low power (1.2304.11)

A PMA/PMD may be placed into a low-power mode by setting bit 1.2304.11 to a one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the PMA/PMD. The behavior of the PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.2304.11 is zero.
NOTE—This operation will interrupt data communication. The data path of a PMD, depending on type and temperature, may take many seconds to run at optimum error ratio after exiting from reset or low-power mode.

45.2.1.(X).3 BASE-T1 Master/Slave (1.2304.4)

When Auto-Negotiation is disabled, this bit is used to configure the PHY to be master or slave. When set as a one the PHY is configured to be a master. When set as a zero the PHY is configured to be a slave. The setting of this bit shall be ignored when Auto-Negotiation is enabled.

45.2.1.(X).4 BASE-T1 PHY Type (1.2304.3:0)

When Auto-Negotiation is disabled these bits are used to configure the PHY type. The setting of these bits shall be ignored when Auto-Negotiation is enabled.

45.2.1.(X+1) 1000BASE-T1 PMA Status Register (Register 1.2305)

The assignment of bits in the 1000BASE-T1 training register is shown in Table 45–YY1.

Table 45-YY1 – 1000BASE-T1 Training Register

Bit(s)	Name	Description	R/W
1.2305.15:12	Reserved	Set to 0s	RO
1.2305.11	OAM Ability	1 = PHY has OAM ability 0 = PHY does not have OAM ability	RO
1.2305.10	EEE Ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2305.9	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	
1.2305.8	Low-power ability	1 = PMA/PMD supports low-power mode 0 = PMA/PMD does not support low-power mode	RO
1.2305.7:3	Reserved	Ignore when read	RO
1.2305.2	Receive Polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2305.1	Receive Fault	1 = Fault condition detected 0 = Fault condition not detected	RO/LH
1.2305.0	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL

45.2.1.(X+1).1 1000BASE-T1 OAM Ability (1.2305.11)

When read as a one, this bit indicates that the PHY supports OAM. When read as a zero, this bit indicates that the PHY does not support OAM.

45.2.1.(X+1).2 1000BASE-T1 EEE Ability (1.2305.10)

When read as a one, this bit indicates that the PHY supports EEE. When read as a zero, this bit indicates that the PHY does not support EEE.

45.2.1.(X+1).3 1000BASE-T1 Receive fault ability (1.2305.9)

When read as a one, bit 1.2305.9indicates that the PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2305.9 indicates that the PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.(X+1).4 1000BASE-T1 Low-power ability (1.2305.8)

When read as a one, bit 1.2305.8 indicates that the PMA/PMD supports the low-power feature. When read as a zero, bit 1.2305.8 indicates that the PMA/PMD does not support the low-power feature. If a PMA/PMD supports the low-power feature, then it is controlled using the low-power bit 1.2304.11.

45.2.1.(X+1).5 1000BASE-T1 Receive Polarity (1.2305.2)

When read as zero, bit 1.2305.2 indicates that the polarity of the receiver is not reversed. When read as one, bit 1.2305.2 indicates that the polarity of receiver is reversed.

45.2.1.(X+1).6 1000BASE-T1 Receive Fault (1.2305.1)

When read as a one, bit 1.2305.1 indicates that the PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.2305.1 indicates that the PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.2305.9. A PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit.

45.2.1.(X+1).7 1000BASE-T1 Receive link status (1.2305.0)

When read as a one, bit 1.2305.0 indicates that the PMA/PMD receive link is up. When read as a zero, bit 1.2305.0 indicates that the PMA/PMD receive link is down. The receive link status bit shall be implemented with latching low behavior.

45.2.1.(X+2) 1000BASE-T1 Training Register (Register 1.2306)

The assignment of bits in the 1000BASE-T1 training register is shown in Table 45–YY2.

Table 45-YY2 – 1000BASE-T1 Training Register

Bit(s)	Name	Description	R/W
1.2306.15:11	Reserved	Set to 0s	R/W
1.2306.10:4	User Field	7 bit user defined field to send to the link partner	R/W
1.2306.1	OAM Advertisement	1 = OAM ability advertised to link partner 0 = OAM ability not advertised to link partner	R/W
1.2306.0	EEE Advertisement	1 = EEE ability advertised to link partner 0 = EEE Ability not advertised to link partner	R/W

45.2.1.(X+2).1 1000BASE-T1 User Field (1.2306.10:4)

This register is a user defined 7 bit field that is transmitted to the link partner during training.

45.2.1.(X+2).2 1000BASE-T1 OAM Advertisement (1.2306.1)

When set as a one, this bit indicates to the link partner that the PHY is advertising OAM capability. When set as a zero, this bit indicates to the link partner that the PHY is not advertising OAM capability. This bit shall be set to 0 if the PHY does not support OAM.

45.2.1.(X+2).3 1000BASE-T1 EEE Advertisement (1.2306.0)

When set as a one, this bit indicates to the link partner that the PHY is advertising EEE capability. When set as a zero, this bit indicates to the link partner that the PHY is not advertising EEE capability. This bit shall be set to 0 if the PHY does not support EEE.

45.2.1.(X+3) 1000BASE-T1 Link Partner Training Register (Register 1.2307)

The assignment of bits in the 1000BASE-T1 link partner training register is shown in Table 45–YY3. The values in this register are not valid until link is up.

Table 45-YY3 – 1000BASE-T1 Link Partner Training Register

Bit(s)	Name	Description	R/W
1.2307.15:11	Reserved	Ignore when read	RO
1.2307.10:4	Link Partner User Field	7 bit user defined field received from the link partner	RO
1.2307.3:2	Reserved	Ignore when read	RO
1.2307.1	Link Partner OAM Advertisement	1 = Link partner has OAM ability 0 = Link partner does not have OAM ability	RO
1.2307.0	Link Partner EEE Advertisement	1 = Link partner has EEE ability 0 = Link partner does not have EEE ability	RO

45.2.1.(X+3).1 1000BASE-T1 Link Partner User Field Register (1.2307.10:4)

This register is a user defined 7 bit field that is received from the link partner during training.

45.2.1.(X+3).2 1000BASE-T1 Link Partner OAM Advertisement Register (1.2307.1)

When read as a one, this bit indicates the link partner is advertising OAM capability. When read as a zero, this bit indicates the link partner is not advertising OAM capability. OAM capability shall be enabled only when both PHY and link partner are advertising OAM capability.

45.2.1.(X+3).3 1000BASE-T1 Link Partner EEE Advertisement Register (1.2307.0)

When read as a one, this bit indicates the link partner is advertising EEE capability. When read as a zero, this bit indicates the link partner is not advertising EEE capability. EEE capability shall be enabled only when both PHY and link partner are advertising EEE capability.

45.2.1.(X+3) 1000BASE-T1 Test mode control (Register 1.2308)

The assignment of bits in the 1000BASE-T1 Test mode control register is shown in Table 45–YY4. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45-YY4 – 1000BASE-T1 Test mode control Register

Bit(s)	Name	Description	R/W
1.2308.15:13	Test mode control	15 14 13 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Reserved 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal operation	R/W
1.2308.12:0	Reserved	Set to 0s	R/W

45.2.1.(X+3).1 1000BASE-T1 Test mode control (1.2308.15:13)

Transmitter test mode operations defined by bits 1.2307.15:13, are described in 97.5.2 and Table 97-10. The default value for bits 1.2308.15:13 is zero.

97.4.2.5.10 PHY Control Registers

Editors Note: Remove table 97-9 since it is moved to table 45-YY3 above. Also table 45-YY1 was baselined in tu_3bp_01a_0215.pdf page 8 but was not included in D1.30. Replace with the text below.

The PHY control registers are shown in table 97-9.

Table 97-9 – PHY Control Registers

Variable	Name	Register Mapping
force_config (see 97.6.1.1)	Master/Slave	1.2304.4
force_PHY_type (see 97.6.1.1)	PHY Type	1.2304.3:0
	OAM Ability	1.2305.11
	EEE Ability	1.2305.10
PMA_state<7:6> = 00, Oct10<7:1>	User Field	1.2306.10:4
PMA_state<7:6> = 00, Oct10<0>	OAM Advertisement	1.2306.1
PMA_state<7:6> = 00, Oct9<7>	EEE Advertisement	1.2306.0
LP PMA_state<7:6> = 00, Oct10<7:1>	Link Partner User Field	1.2307.10:4
LP PMA_state<7:6> = 00, Oct10<0>	Link Partner OAM Advertisement	1.2307.1
LP PMA_state<7:6> = 00, Oct9<7>	Link Partner EEE Advertisement	1.2307.0

45.2.2 PCS registers

Editor to insert registers in this section into table 45-119

45.2.2.(X) BASE-T1 PCS Control Register (Register 3.2304)

The assignment of bits in the BASE-T1 control register is shown in Table 45–ZZ0. The default value for each bit of the PCS control 1 register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

Table 45- ZZ0–BASE-T1 Control Register

Bit(s)	Name	Description	R/W
3.2304.15	Reset	1 = PMA/PMD reset 0 = Normal operation	R/W SC
3.2304.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2304.13:0	Reserved	Set to 0s	R/W

45.2.2.(X).1 BASE-T1 Reset (3.2304.15)

Resetting a PCS is accomplished by setting bit 1.2304.15 to a one. This action shall set all PCS registers to their default states. As a consequence, this action may change the internal state of the PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and a PCS shall return a value of one in bit 1.2304.15 when a reset is in progress; otherwise, it shall return a value of zero. A PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.2304.15. During a reset, a PCS shall respond to reads from register bits 3.2304.15 and 3.8.15:14. All other register bits should be ignored.
NOTE—This operation may interrupt data communication.

45.2.2.(X).2 BASE-T1 Low power (3.2304.14)

The PCS shall be placed in a loopback mode of operation when bit 3.2304.14 is set to a one. When bit 3. 2304.14 is set to a one, the PCS shall accept data on the transmit path and return it on the receive path.
The default value of bit 3.2304.14 is zero.

45.2.2.(X+1) BASE-T1 PCS Status 1 Register (Register 3.2305)

The assignment of bits in the BASE-T1 Status 1 register is shown in Table 45–ZZ1. All the bits in the PCS status 1 register are read only; a write to the PCS status 1 register shall have no effect.

Table 45- ZZ1–BASE-T1 Status 1 Register

Bit(s)	Name	Description	R/W
3.2305.15:12	Reserved	Ignore when read	RO
3.2305.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2305.10	Rx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2305.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2305.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2305.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.2305.6:3	Reserved	Ignore when read	RO
3.2305.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2305.1:0	Reserved	Ignore when read	RO

45.2.2.(X+1).1 BASE-T1 Transmit LPI received (3.2305.11)

When read as a one, bit 3.2305.11 indicates that the transmit PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2305.11 indicates that the PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.2.(X+1).2 BASE-T1 Receive LPI received (3.2305.10)

When read as a one, bit 3.2305.10 indicates that the receive PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2305.10 indicates that the PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.2.(X+1).3 BASE-T1 Transmit LPI indication (3.2305.9)

When read as a one, bit 3.2305.9 indicates that the transmit PCS is currently receiving LPI signals. When read as a zero, bit 3.2305.9 indicates that the PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.2.(X+1).4 BASE-T1 Receive LPI indication (3.2305.8)

When read as a one, bit 3.2305.8 indicates that the receive PCS is currently receiving LPI signals. When read as a zero, bit 3.2305.8 indicates that the PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.1.(X+1).5 BASE-T1 Fault (3.2305.7)

When read as a one, bit 3.1.7 indicates that the PCS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 3.1.7 indicates that the PCS has not detected a fault condition.

45.2.1.(X+1).6 BASE-T1 PCS receive link status (3.2305.2)

When read as a one, bit 3.2305.2 indicates that the PCS receive link is up. When read as a zero, bit 3.2305.2 indicates that the PCS receive link is down. This bit is a latching low version of bit 3.2306.10. The receive link status bit shall be implemented with latching low behavior.

45.2.2.(X+2) BASE-T1 PCS Status 2 Register (Register 3.2306)

The assignment of bits in the BASE-T1 Status 2 register is shown in Table 45–ZZ2. All the bits in the PCS status 2 register are read only; a write to the PCS status 2 register shall have no effect. .

Table 45- ZZ2–BASE-T1 PCS Status 2 Register

Bit(s)	Name	Description	R/W
3.2306.15:11	Reserved	Ignore when read	RO
3.2306.10	Receive link status	1 = PCS receive link up 0 = PCS receive link down	RO
3.2306.9	PCS high BER	1 = PCS reporting a high BER 0 = PCS not reporting a high BER	RO
3.2306.8	PCS block lock	1 = PCS locked to received blocks 0 = PCS not locked to received blocks	RO
3.2306.7	Latched high BER	1 = PCS has reported a high BER 0 = PCS has not reported a high BER	RO/LL
3.2306.6	Latched block lock	1 = PCS has block lock 0 = PCS does not have block lock	RO/LL
3.2305.5:0	BER	BER counter	RO/NR

45.2.1.(X+2).1 BASE-T1 Receive link status (3.2306.10)

When read as a one, bit 3.2306.10 indicates that the PCS is in a fully operational state. When read as a zero, bit 3.2306.10 indicates that the PCS is not fully operational. This bit is a reflection of the PCS_status variable defined in 97.3.7.1

45.2.1.(X+2).2 BASE-T1 PCS high BER (3.2306.9)

When read as a one, bit 3.2306.9 PCS receiver is detecting a BER of > 4×10^{-4}. When read as a zero, bit 3.32.1 indicates that the receiver is detecting a BER of > 4×10^{-4}. This bit is a direct reflection of the state of the hi_rfer variable defined in 97.3.7.1.

45.2.1.(X+2).3 BASE-T1 PCS block lock (3.2306.8)

When read as a one, bit 3.2306.8 indicates that the receiver has block lock. When read as a zero, bit 3.2306.8 indicates that the receiver has not achieved block lock. This bit is a direct reflection of the state of the block_lock variable defined in 97.3.7.1

45.2.1.(X+2).4 BASE-T1 Latched high BER (3.2306.7)

When read as a one, bit 3.2306.7 indicates that the PCS has detected a high BER. When read as a zero, bit 3.2306.7 indicates that the PCS has not detected a high BER. The latched high BER bit shall be implemented with latching high behavior. This bit is a latching high version of the PCS high BER status bit (3.2306.9).

45.2.1.(X+2).5 BASE-T1 Latched block lock (3.2306.6)

When read as a one, bit 3.2306.6 indicates that the PCS has achieved block lock. When read as a zero, bit 3.2306.6 indicates that the PCS has lost block lock. The latched block lock bit shall be implemented with latching low behavior. This bit is a latching low version of the PCS block lock status bit (3.2306.8)

45.2.1.(X+2).6 BASE-T1 BER count (3.2306.5:0)

The BER counter is a six bit count as defined by RFER_count in 97.3.7.2. These bits shall be reset to all zeros when the PCS status 2 register is read by the management function or upon execution of the BASE-T1 PCS reset. These bits shall be held at all ones in the case of overflow.

In section 97.7.3 including all subsections make the register substitutions:
3.TBD0 ➔ 3.2308
3.TBD1 ➔ 3.2309
3.TBD2 ➔ 3.2310
3.TBD3 ➔ 3.2311
3.TBD4 ➔ 3.2312
3.TBD5 ➔ 3.2313
3.TBD6 ➔ 3.2314
3.TBD7 ➔ 3.2315
3.TBD8 ➔ 3.2316
3.TBD9 ➔ 3.2317

Move sections 97.7.3.1 to 97.7.3.4 into 45.2.2.(x+4) to 45.2.2.(x+7). Do not move the text and table in 97.7.3
All references in section 97.7 that points to 97.7.3.1 to 97.7.3.4 must point to the new sections in 45.2.2.(x+4) to 45.2.2.(x+7) respectively.

45.2.7 Auto-Negotiation registers

Editor to insert registers in this section into table 45-200

45.2.7.15 BASE-T1 AN control register (Register 7.512)

The assignment of bits in the AN control register is shown in Table 45–XX0. The default value for each bit of the AN control register has been chosen so that the initial state of the device upon power up or completion of reset is a normal operational state without management intervention.

Table 45-XX0 BASE-T1 AN control register bit definitions

Bit(s)	Name	Description	R/W
7.512.15	AN reset	1 = AN reset 0 = AN normal operation	R/W SC
7.512.14:13	Reserved	Value always 0	RO
7.512.12	Auto-Negotiation enable	1 = enable Auto-Negotiation process 0 = disable Auto-Negotiation process	R/W
7.512.11:10	Reserved	Value always 0	RO
7.512.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation process 0 = Auto-Negotiation in process, disabled, or not supported	R/W SC
7.512.8:0	Reserved	Value always 0	RO

45.2.7.15.1 AN reset (7.512.15)

Resetting AN is accomplished by setting bit 7.512.15 to a one. This action shall set all BASE-T1 AN registers to their default states. As a consequence, this action may change the internal state of AN and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and AN shall return a value of one in bit 7.512.15 when a reset is in progress and a value of zero otherwise. AN is not required to accept a write transaction to any of its registers until the reset process is complete. The reset process shall be completed within 0.5 s from the setting of bit 7.512.15. During an AN reset, AN shall respond to reads from register bit 7.512.15. All other register bits should be ignored.

The default value for bit 7.512.15 is zero.

NOTE—This operation may interrupt data communication.

45.2.7.15.2 Auto-Negotiation enable (7.512.12)

The Auto-Negotiation function shall be enabled by setting bit 7.512.12 to a one. If bit 7.512.12 is set to one, then PHY type bits 1.2304.3:0 Master/Slave bits 1.2304.4 shall have no effect on the link configuration, and the Auto-Negotiation process determines the link configuration. If bit 7.512.12 is cleared to zero, then bits 1.2304.3:0 and 1.2304.4 determines the link configuration regardless of the prior state of the link configuration and the Auto-Negotiation process.

The default value of bit 7.512.12 is one, unless the PHY reports via bit 7.513.3 that it lacks the ability to perform Auto-Negotiation, in which case the default value of bit 7.512.12 is zero.

45.2.7.15.3 Restart Auto-Negotiation (7.512.9)

If the PMA/PMD reports (via bit 7.513.3) that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, the PMA/PMD shall return a value of zero in bit 7.512.9 and any attempt to write a one to bit 7.512.9 shall be ignored.

Otherwise, the Auto-Negotiation process shall be restarted by setting bit 7.512.9 to one. This bit is self-clearing, and a PMA/PMD shall return a value of one in bit 7.512.9 until the Auto-Negotiation process has been initiated. If Auto-Negotiation was completed prior to this bit being set, the process shall be reinitiated. The Auto-Negotiation process shall not be affected by clearing this bit to zero.

The default value for 7.0.9 is zero.

45.2.7.16 BASE-T1 AN status (Register 7.513)

The assignment of bits in the AN status register is shown in Table 45–XX1. All the bits in the AN status register are read only; therefore, a write to the AN status register shall have no effect.

Table 45-XX1 BASE-T1 AN status register

Bit(s)	Name	Description	R/W
7.513.15:7	Reserved	Value always 0	RO
7.513.6	Page received	1 = A page has been received 0 = A page has not been received	RO LH
7.513.5	Auto-Negotiation complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO
7.513.4	Remote fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO LH
7.513.3	Auto-Negotiation ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO
7.513.2	Link status	1 = Link is up 0 = Link is down	RO LL
7.513.1	Reserved	Value always 0	RO
7.513.0	Link partner Auto-Negotiation ability	1 = LP is able to perform Auto-Negotiation 0 = LP is not able to perform Auto-Negotiation	RO

45.2.7.16.1 Page received (7.513.6)

The Page received bit (7.513.6) shall be set to one to indicate that a new link codeword has been received and stored in the BASE-T1 AN LP Base Page ability registers 7.517 to 7.519 or BASE-T1 AN LP NEXT PAGE ability registers 7.523 to 7.525. The contents of the BASE-T1 AN LP Base Page ability registers 7.517 to 7.519 are valid when bit 7.513.6 is set the first time during the Auto-Negotiation. The Page received bit shall be reset to zero on a read of the BASE-T1 AN status register (Register 7.513).

45.2.7.16.2 Auto-Negotiation complete (7.513.5)

When read as a one, bit 7.513.5 indicates that the Auto-Negotiation process has been completed, and that the contents of the Auto-Negotiation register 7.514 to 7.516 and 7.517 to 7.519 are valid. When read as a zero, bit 7.513.5 indicates that the Auto-Negotiation process has not been completed, and that the contents of 7.517 through 7.525 registers are as defined by the current state of the Auto-Negotiation protocol, or as written for manual configuration. A PMA/PMD shall return a value of zero in bit 7.513.5 if Auto-Negotiation is disabled by clearing bit 7.512.12. A PMA/PMD shall also return a value of zero in bit 7.513.5 if it lacks the ability to perform Auto-Negotiation.

45.2.7.16.3 Remote fault (7.513.4)

When read as one, bit 7.513.4 indicates that a remote fault condition has been detected. The type of fault as well as the criteria and method of fault detection is AN specific. The remote fault bit shall be implemented with a latching function, such that the occurrence of a remote fault causes the bit 7.513.4 to become set and remain set until it is cleared. Bit 7.513.4 shall be cleared each time register 7.513 is read via the management interface, and shall also be cleared by a AN reset.

45.2.7.16.4 Auto-Negotiation ability (7.513.3)

When read as a one, bit 7.513.3 indicates that the PMA/PMD has the ability to perform BASE-T1 Auto-Negotiation. When read as a zero, bit 7.513.3 indicates that the PMA/PMD lacks the ability to perform BASE-T1 Auto-Negotiation.

45.2.7.16.5 Link status (7.513.2)

When read as a one, bit 7.513.2 indicates that the PMA/PMD has determined that a valid link has been established. When read as a zero, bit 7.513.2 indicates that the link has been invalid after this bit was last read. Bit 7.513.2 is set to one when the variable link_status equals OK and is cleared to zero when the variable link_status equals FAIL. The link status bit shall be implemented with a latching function, such that the occurrence of a link_status equals FAIL condition causes the link status bit to become cleared and remain cleared until it is read via the management interface. Bit 7.513.2 shall be cleared upon AN reset. This status indication is intended to support the management attribute defined in 30.5.1.1.4, aMediaAvailable.

45.2.7.16.6 Link partner Auto-Negotiation ability (7.513.0)

The link partner Auto-Negotiation ability bit shall be set to one to indicate that the link partner is able to participate in the Auto-Negotiation function. This bit shall be reset to zero if the link partner is not Auto-Negotiation able.

45.2.7.17 BASE-T1 AN advertisement register (7.514, 7.515, and 7.516)

The Selector field (7.514.4:0) is set to the IEEE 802.3 code as specified in Annex 98A. The Acknowledge bit (7.514.14) is set to zero.

The technology ability field, as defined in 98.2.1.2, represents the technologies supported by the local device. Only bits representing supported technologies may be set. Management may clear bits in the technology ability field and restart Auto-Negotiation to negotiate an alternate common mode.

The management entity initiates renegotiation with the link partner using alternate abilities by setting the Restart Auto-Negotiation bit (7.512.9) in the AN control register to one.

Any writes to this register prior to completion of Auto-Negotiation, as indicated by bit 7.513.5, should be followed by a renegotiation for the new values to take effect. Once Auto-Negotiation has completed, software may examine this register along with the LP Base Page ability register to determine the highest common denominator technology.

The Base Page value is transferred to mr_adv_ability when register 7.514 is written. Therefore, if used, registers 7.515 and 7.516 should be written before 7.514.

Table 45-XX2 BASE-T1 AN advertisement register bit definitions

Bit(s)	Name	Description	R/W
7.514.15	Next Page	See 98.2.1.2.9	R/W
7.514.14	Acknowledge	Value always 0, writes ignored	RO
7.514.13	Remote fault	See 98.2.1.2.7	R/W
7.514.12:5	D12:D5	See 98.2.1.2	R/W
7.514.4:0	Selector field	See Annex 98A	R/W
7.515.15:0	D31:D16	See 98.2.1.2	R/W
7.516.15:0	D47:D32	See 98.2.1.2	R/W

45.2.7.18 BASE-T1 AN LP Base Page ability register (7.517, 7.518, and 7.519)

All of the bits in the BASE-T1 AN LP Base Page ability register are read only. A write to the BASE-T1 AN LP Base Page ability register shall have no effect.

The value of the registers 7.20 and 7.21 is latched when register 7.19 is read and reads of registers 7.20 and 7.21 return the latched value rather than the current value.

Table 45-XX3 AN LP Base Page ability register bit definitions

Bit(s)	Name	Description	RO
7.517.15:0	D15:D0	See 98.2.1.2	RO
7.518.15:0	D31:D16	See 98.2.1.2	RO
7.519.15:0	D47:D32	See 98.2.1.2	RO

45.2.7.19 BASE-T1 AN NEXT PAGE transmit register (7.520, 7.521, and 7.522)

The register contains the BASE-T1 AN LD Next Page link codeword as defined in 98.2.4.3.

On power-up or AN reset, this register shall contain the default value, which represents a Message Page with the message code set to Null Message. This value may be replaced by any valid Extended Next Page message code that the device intends to transmit.

A write to register 7.521 or 7.522 does not set mr_next_page_loaded. Only a write to register 7.520 sets mr_next_page_loaded true as described in 98.5.1. Therefore registers 7.521 and 7.522 register should be written before register 7.520.

Table 45-XX4 BASE-T1 AN NEXT PAGE transmit register bit definitions

Bit(s)	Name	Description	R/W
7.520.15	Next Page	See 98.2.4.3	R/W
7.520.14	Reserved	Value always 0	RO
7.520.13	Message Page	See 98.2.4.3	R/W
7.520.12	Acknowledge 2	See 98.2.4.3	R/W
7.520.11	Toggle	See 98.2.4.3	RO
7.520.10:0	Message/Unformatted Code Field	See 98.2.4.3	R/W
7.521.15:0	Unformatted Code Field 1	See 98.2.4.3	R/W
7.522.15:0	Unformatted Code Field 2	See 98.2.4.3	R/W

45.2.7.20 BASE-T1 AN LP NEXT PAGE ability register (7.523, 7.524, and 7.525)

BASE-T1 AN LP NEXT PAGE ability register (registers 7.523, 7.524, and 7.525) store BASE-T1 link partner Extended Next Pages as shown in Table 45–XX5. All of the bits in the BASE-T1 AN LP NEXT PAGE ability register are read only. A write to the BASE-T1 AN LP NEXT PAGE ability register shall have no effect.

The value of registers 7.524 and 7.525 is latched when register 7.523 is read and reads of registers 7.524 and 7.525 return the latched value rather than the current value.

NOTE—If this register is used to store multiple link partner Extended Next Pages, the previous value of this register is assumed to be stored by a management entity that needs the information overwritten by subsequent link partner Extended Next Pages.

Table 45-XX5 AN LP NEXT PAGE ability register bit definitions

Bit(s)	Name	Description	R/W
7.523.15	Next Page	See 98.2.4.3	RO
7.523.14	Acknowledge	See 98.2.4.3	RO
7.523.13	Message Page	See 98.2.4.3	RO
7.523.12	Acknowledge 2	See 98.2.4.3	RO
7.523.11	Toggle	See 98.2.4.3	RO
7.523.10:0	Message/Unformatted Code Field	See 98.2.4.3	RO
7.524.15:0	Unformatted Code Field 1	See 98.2.4.3	RO
7.525.15:0	Unformatted Code Field 2	See 98.2.4.3	RO

98 Physical Layer Link Signaling for Auto-Negotiation on Single Twisted Pair

Editor to make changes in clause 98 to be consistent with the register changes are as follows:
7.0 ➔ 7.512
7.1 ➔ 7.513
7.16 ➔ 7.514
7.17 ➔ 7.515
7.18 ➔ 7.516
7.19 ➔ 7.517
7.20 ➔ 7.518
7.21 ➔ 7.519
7.22 ➔ 7.520
7.23 ➔ 7.521
7.24 ➔ 7.522
7.25 ➔ 7.523
7.26 ➔ 7.522
7.27 ➔ 7.524
AN advertisement register ➔ BASE-T1 AN advertisement register
AN LP Base Page ability register ➔ BASE-T1 AN LP Base Page ability register
AN NEXT PAGE transmit register ➔ BASE-T1 AN NEXT PAGE transmit register
AN LP NEXT PAGE ability register ➔ BASE-T1 AN LP NEXT PAGE ability register