97. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, Physical Medium Dependent (PMD) sublayer, and baseband medium, type 1000BASE-T1

97.1 Overview

This clause defines the type 1000BASE-T1 Physical Coding Sublayer (PCS), type 1000BASE-T1 Physical Medium Attachment (PMA) sublayer, and type 1000BASE-T1 Physical Medium Dependent (PMD). Together, the PCS, PMA, and PMD sublayers comprise a 1000BASE-T1 Physical Layer (PHY). Provided in this clause are fully functional and electrical specifications for the type 1000BASE-T1 PCS, PMA, and PMD. This clause also specifies the critical parameters of the baseband medium used with 1000BASE-T1 PHY.

The 1000BASE-T1 PHY is one of the Gigabit Ethernet family of high-speed full-duplex network specifications, capable of operating at 1000 Mb/s and intended to be operated over a single pair of balanced copper cabling, referred to as an automotive link segment (Type A) or additional link segment (Type B), defined in 97.5.6. The cabling supporting the operation of the 1000BASE-T1 PHY is defined in terms of performance requirements between the attachment points (Medium Dependent Interface (MDI)), allowing implementers to provide their own cabling to operate the 1000BASE-T1 PHY as long as the normative requirements included in this Clause are met.

This clause also specifies 1000BASE-T1 Low Power Idle (LPI) as part of Energy-Efficient Ethernet (EEE). This allows the PHY to enter a low power mode of operation during periods of low link utilization as described in Clause 78.

97.1.1 Relationship of 1000BASE-T1 to other standards

Relations between the 1000BASE-T1 PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 CSMA/CD LAN Model are shown in Figure 97–1. The PHY sublayers (shown shaded) in Figure 97–1 connect one Clause 4 Media Access Control (MAC) layer to the medium. Auto-Negotiation for 1000BASE-T1 is defined in Clause 98. GMII is defined is Clause 35.

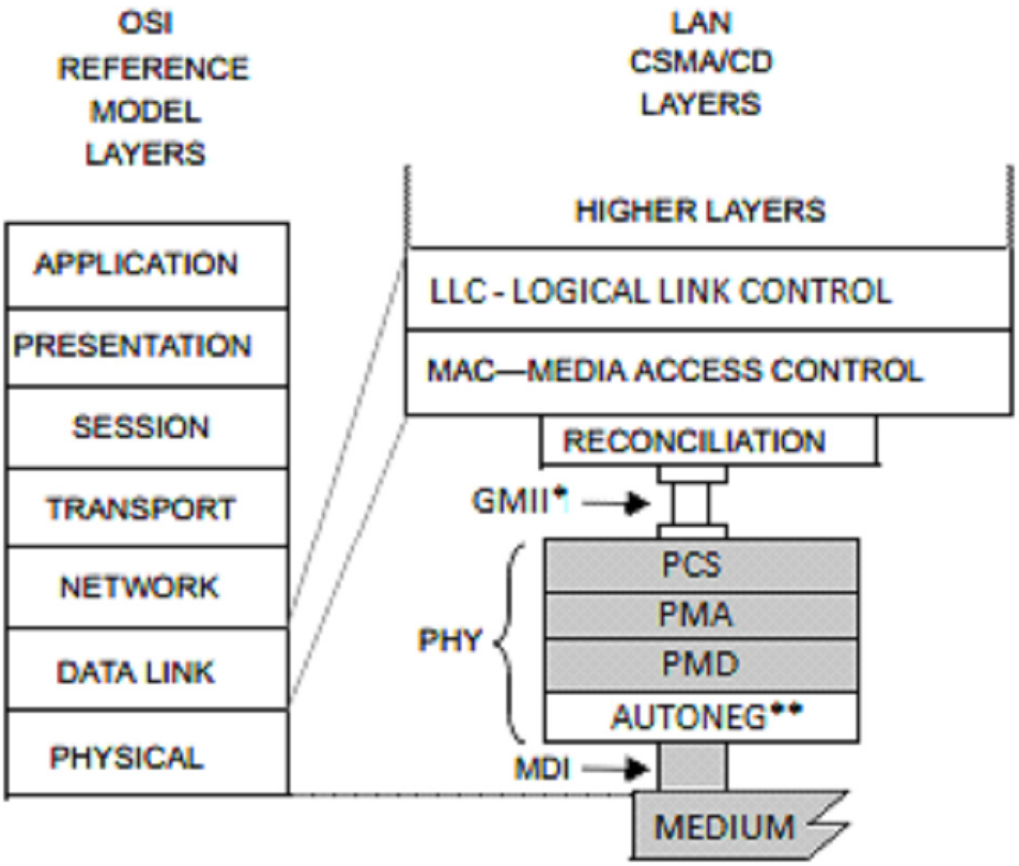


Figure 97–1—Relationship of 1000BASE-T1 PHY to the ISO/IEC OSI reference model and the IEEE 802.3 CSMA/CD LAN Model

MDI = MEDIUM DEPENDENT INTERFACE

GMII = GIGABIT MEDIA INDEPENDENT INTERFACE

AUTONEG = AUTO-NEGOTIATION

PCS = PHYSICAL CODING SUBLAYER

PMA = PHYSICAL MEDIUM ATTACHMENT

PHY = PHYSICAL LAYER DEVICE

PMD = PHYSICAL MEDIUM DEPENDENT

* GMII is optional

** AUTONEG is optional

97.1.2 Operation of 1000BASE-T1

The 1000BASE-T1 PHY operates using full-duplex communications (using echo cancellation) over a single pair of balanced copper cabling with an effective rate of 1 Gb/s in each direction simultaneously while meeting the requirements (EMC, temperature, etc.) of automotive and industrial environments. The PHY supports operation on two types of link segments:

a) An automotive link segment supporting up to four inline connectors using unshielded balanced copper cabling for at least 15 meters (referred to as link segment type A).
b) An additional link segment supporting up to four inline connectors using balanced copper cabling for at least 40 meters to support applications requiring additional physical reach, such as industrial and automation controls and transportation (aircraft, railway, bus and heavy trucks). This link segment is referred to as link segment type B.

The 1000BASE-T1 PHY utilizes 3 level Pulse Amplitude Modulation (PAM3) transmitted at a 750 MHz rate. A 15-bit scrambler is used to improve the EMC performance. GMII TX_D, TX_EN, and TX_ER are encoded together in using 81B encoding where 10 cycles of GMII data and control are encoded together in 81 bits to reduce the overhead. To maintain a bit error ratio (BER) of less than or equal to 10^{-10}, the 1000BASE-T1 PHY adds a 396 bit Reed Solomon Forward Error Correction (RS FEC) code to each group of forty-five 81B blocks (containing 450 octets of GMII data). The PAM3 mapping, scrambler, RS FEC, and 81B encoder/decoder are all contained in the PCS (see 97.3).

Auto-Negotiation (Clause 98) may optionally be used by 1000BASE-T1 devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for joint operation. Auto-Negotiation is performed upon link startup through the use of half-duplex differential Manchester encoding.

A 1000BASE-T1 PHY can be configured either as a MASTER PHY or as a SLAVE PHY. A MASTER PHY uses a local clock to determine the timing of transmitter operations. A SLAVE PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations. When Auto-Negotiation is used, The MASTER-SLAVE relationship between two stations sharing a link segment is established during Auto-Negotiation (see Clause 98). If Auto-Negotiation is not used, MASTER-SLAVE relationship is established by management or hardware configuration of the PHY, and the MASTER and SLAVE are synchronized by a PHY Link Synchronization function in the PHY (see 97.6).

A 1000BASE-T1 PHY may optionally support Energy Efficient Ethernet (see Clause 78) and advertise the EEE capability as described in 78.3. The EEE capability is a mechanism by which 1000BASE-T1 PHYs are able to reduce power consumption during periods of low link utilization.

The 1000BASE-T1 PMA couples messages from the PCS to the MDI and provides clock recovery, link management and PHY Control functions. The PMA provides full duplex communications at 750 MBd over the single pair of balanced copper cabling. PMA functionality is described in 97.4. The PMD is described in 97.5. The MDI is specified in 97.8.

97.1.2.1 Physical Coding Sublayer (PCS)

The 1000BASE-T1 PCS couples a Gigabit Media Independent Interface (GMII), as described in Clause 35, to a Physical Medium Attachment (PMA) sublayer, described in 97.4, which supports communication over a single pair of balanced copper cabling.

The PCS comprises the PCS Reset function, PCS Transmit, and PCS Receive. The Transmit and Receive functions start immediately after completion of the Reset function and run simultaneously and asynchronously with relation to each other.

In Data Mode, the PCS Transmit function data path starts with the GMII interface, where TXD, TX_EN, and TX_ER input data to the PCS every 8 ns (as clocked by GTX_CLK). Data and control from ten GTX_CLK cycles are encoded into an 81 bit "81B block" that encodes every possible combination of data and control (control signals include error propagation, assert low power idle, and inter-frame signaling). Each set of forty-five 81B blocks along with 9 bits of OAM data (see 97.7) processed by a Reed Solomon FEC encoder (RS FEC). The RS encoder adds 396 bits of FEC data and the 4050 bits (forty-five 81B blocks = 3645 bits, 9 bits of OAM, and 396 bits of FEC data) are scrambled using a 15-bit side-stream scrambler. Each 3 bits of the scrambled data is converted to 2 ternary PAM3 symbols by the 3B2T mapper (the 4050 bits in the RS frame become 2700 PAM3 symbols) and passed to the PMA. PCS transmit functions are described in 97.3.2.2.

In Data Mode, the PCS Receive function data path operates in the opposite order as the transmit path. The incoming PAM3 symbols are synchronized to frame boundaries. Within each frame, each two PAM3 symbols are de-mapped to 3 bits by the 3B2T demapper (the 2700 PAM3 symbols are converted to 4050 bits). The data is then descrambled and passed to the RS FEC decoder for data validation and correction. Finally, each of the forty-five 81B blocks is decoded into GMII data or control. PCS data mode receive is described in 97.3.2.3.

In Training Mode (see 97.4.2.5), the PCS transmits and receives data sequences to synchronize the RS FEC blocks, learn the Data Mode scrambler seed, and exchange EEE and OAM capabilities. The training mode uses PAM2 encoding.

97.1.2.2 Physical Medium Attachment (PMA) sublayer

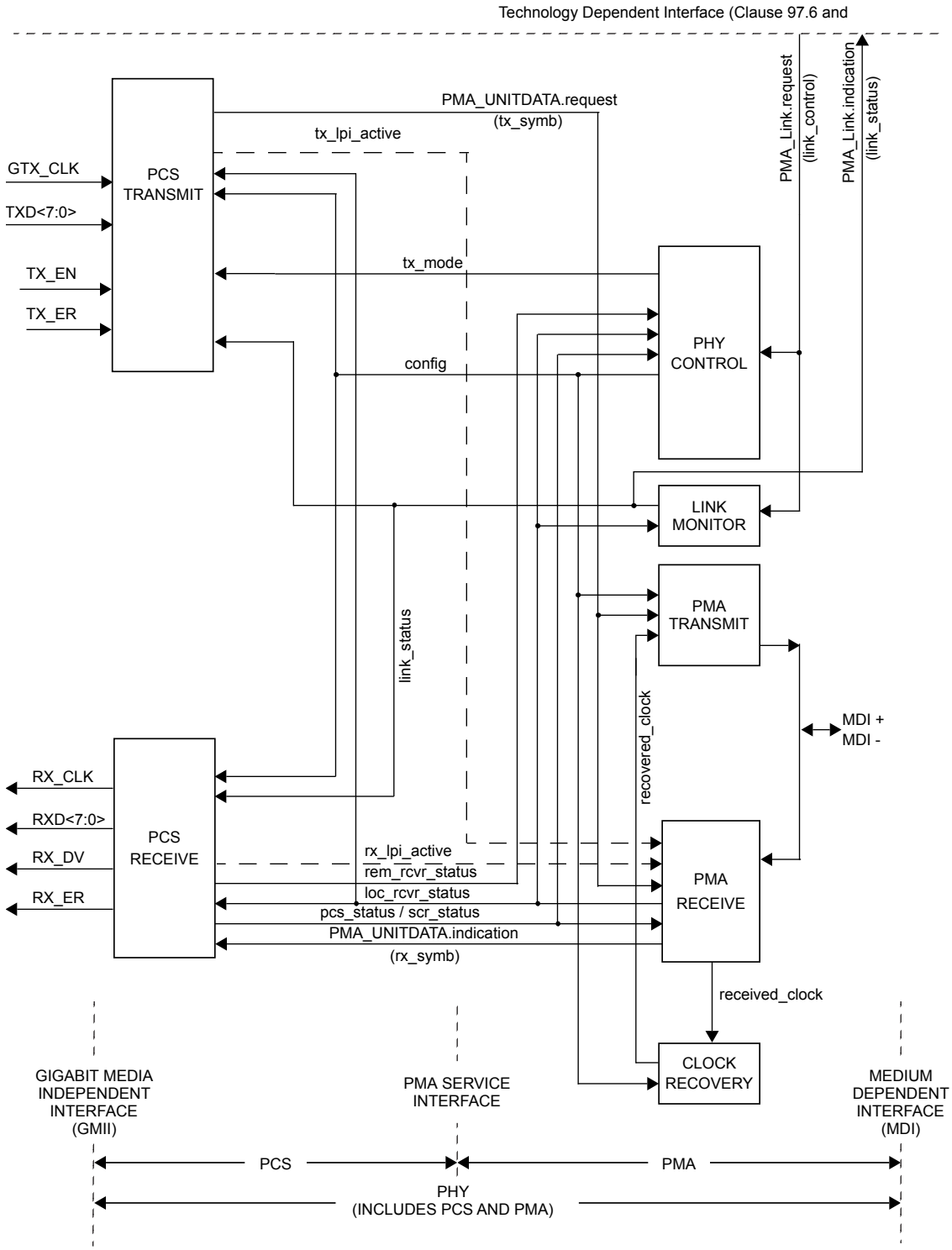
The 1000BASE-T1 PMA transmits/receives symbol streams to/from the PCS onto the single balanced twisted pair and provides the clock recovery, link monitor and the 1000BASE-T1 PHY Control function. The PMA provides full duplex communications at 750 MBd.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control is enabled following the completion of Auto-Negotiation or PHY Link Synchronization and provides the start-up functions required for successful 1000BASE-T1 operation. It determines whether the PHY operates in a disabled state, a training state, or a data state where MAC frames can be exchanged between the link partners.

The Link Monitor determines the status of the underlying link channel and communicates this status to other functional blocks. A failure of the receive channel causes data mode operation to stop and Auto-Negotiation or Link Synchronization to restart.

97.1.2.3 Physical Medium Dependent (PMD) sublayer

The1000BASE-T1 PMD (see 97.5) defines the transmit and receive electrical characteristics. The PMD also specifies the minimum link segment characteristics, EMC requirements, and test modes.



NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing

NOTE—Signals and functions shown with dashed lines are optional.

Figure 97–2—Functional block diagram

97.1.2.4 EEE capability

A 1000BASE-T1 PHY may optionally support the EEE capability, as described in 78.3. The EEE capability is a mechanism by which 1000BASE-T1 PHYs are able to reduce power consumption during periods of low link utilization. PHYs can enter this mode of operation after completing training. Each direction of the full duplex link is able to enter and exit the LPI mode independently, supporting symmetric and asymmetric LPI operation. This allows power savings when only one side of the full duplex link is in a period of low utilization. The transition to or from LPI mode shall cause no data frames be lost or corrupted.

In the transmit direction the transition to the LPI transmit mode begins when the PCS transmit function detects an "Assert Low Power Idle" condition on the GMII in the last 80B/81B block of a frame. At the next RS frame the PCS transmits a sleep signal composed of an entire RS frame containing only LP_IDLE. The sleep signal indicates to the link partner that the transmit function of the PHY is entering the LPI transmit mode. Immediately after the transmission of the sleep frame, the transmit function of the local PHY enters the LPI transmit mode. While the transmit function is in the LPI mode the PHY may disable data path and control logic to save additional power. Periodically the transmit function of the local PHY transmits refresh frames that may be used by the link partner to update adaptive filters and timing circuits in order to maintain link integrity. LPI mode may begin with quiet signaling, a full refresh period, or a wake frame. The quiet-refresh cycle continues until the PCS function detects a condition that is not Assert Low Power Idle on the GMII. This condition signals to the PHY that the LPI transmit mode should end. At the next RS frame the PCS transmits a wake frame composed of an entire RS frame containing only Idle. On the next RS frame normal power mode shall resume.

Support for EEE capability is advertised during Training. See 97.4.2.5.5 for details. Transitions to and from the LPI transmit mode are controlled via GMII signaling. Transitions to and from the LPI receive mode are controlled by the link partner using sleep and wake signaling.

The PCS 80B/81B Transmit state diagram in Figure 97–14 includes additional states for EEE. The PCS 80B/81B Receive state diagram in Figure 97–15 includes additional states for EEE.

97.1.2.5 Link Synchronization

The Link Synchronization function is used when Auto-Negotiation is disabled to synchronize between the MASTER PHY and SLAVE PHY before training starts. Link Synchronization provides a fast and reliable mechanism for the link partner to detect the presence of the other, validate link, and start the timers used by the link monitor. Link Synchronization operates in a half-duplex fashion. Based on timers, the MASTER PHY sends a synchronization sequence for 1 us. If there is no response from the slave, the MASTER repeats by sending a synchronization sequence every 5 us. If the slave detects the sequence, it responds by responding with a synchronization sequence for 1 us (after the MASTER has stopped transmitting). If no other detection happens after the slave response for 4 us then Link Synchronization is successfully complete, link monitor timers are started, and the PHY Control state machine starts Training. Link synchronization is defined in 97.6.

97.1.3 Signaling

1000BASE-T1 signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over the single pair of balanced copper cabling. The signaling scheme achieves a number of objectives including:

a) Algorithmic mapping from TXD<7:0> to PAM3 symbols in the transmit path.
b) Algorithmic mapping from PAM3 symbols to TXD<7:0> in the receive path
c) Adding FEC coded data to transmit and validating data using FEC on receive
d) Uncorrelated symbols in the transmitted symbol stream.

e) No correlation between symbol streams traveling both directions.
f) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
g) Optionally, ability to signal to the remote PHY that transmit in entering the LPI mode or exiting the LPI mode and returning to normal operation.

The PHY may operate in three basic modes, normal mode, training mode, or an optional LPI mode.

In the normal mode, PCS generates code-groups that represent data, control, or idles for transmission by the PMA.

In the training mode, the PCS is directed to generate only a PAM2 pattern with periodic embedded data which enables the receiver at the other end to train and synchronize timing, scrambler seeds, and capabilities. The LPI mode is enabled separately in each direction (see LPI signaling in 97.3.5). When transmitting in LPI mode, the PCS is directed to generate zero symbols and periodically send a REFRESH pattern to keep the two PHYs synchronized (see 97.3.2.2.16).

97.1.4 Interfaces

All 1000BASE-T1 PHY implementations are compatible at the MDI and at a physically exposed GMII, if made available. Physical implementation of the GMII is optional. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and GMII (if the GMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the GMII is implemented or not.

97.1.5 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5.

The values of all components in test circuits shall be accurate to within ±1% unless otherwise stated.

Default initializations, unless specifically specified, are left to the implementer.

97.2 1000BASE-T1 Service Primitives and Interfaces

1000BASE-T1 transfers data and control information across the following four service interfaces:

a) Gigabit Media Independent Interface (GMII)
b) Technology Dependent Interface
c) PMA service interface
d) Medium dependent interface (MDI)

The GMII is specified in Clause 35; the Technology Dependent Interface is specified in 97.6 and Clause 98. The PMA service interface is defined in 97.2.2 and the MDI is defined in 97.8.

97.2.1 Technology Dependent Interface

1000BASE-T1 uses the following service primitives to exchange status indications and control signals across the Technology Dependent Interface as specified in 97.6 or Clause 98:

PMA_LINK.request (link_control)

PMA_LINK.indication (link_status)

97.2.1.1 PMA_LINK.request

This primitive allows the Auto-Negotiation or the PHY Link Synchronization algorithm to enable and disable operation of the PMA, as specified in 98.4.2 or 97.6, respectively.

97.2.1.1.1 Semantics of the primitive

PMA_LINK.request (link_control)

The link_control parameter can take on one of two values: DISABLE, or ENABLE.

DISABLE	Used by the Auto-Negotiation or PHY Link Synchronization process to disable the PHY.
ENABLE	Used by the Auto-Negotiation or PHY Link Synchronization process to enable the PHY.

97.2.1.1.2 When generated

Auto-Negotiation or PHY Link Synchronization generates this primitive to indicate a change in link_control as described in 97.6 or Clause 98.

97.2.1.1.3 Effect of receipt

This primitive affects the operation of the PMA Link Monitor function as defined in 97.4.2.6 and the PMA PHY Control function as defined in 97.4.2.5.

97.2.1.2 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 98.4.1. This primitive informs the PCS, PMA PHY Control function, and the Auto-Negotiation or PHY Link Synchronization process about the status of the underlying link.

97.2.1.2.1 Semantics of the primitive

PMA_LINK.indication (link_status)

The link_status parameter can take on one of two values: FAIL or OK.

FAIL	No valid link established.
OK	The Link Monitor function indicates that a valid 1000BASE-T1 link is established. Reliable reception of signals transmitted from the remote PHY is possible.

97.2.1.2.2 When generated

The PMA generates this primitive to indicate a change in link_status in compliance with the state diagram given in Figure 97–21.

97.2.1.2.3 Effect of receipt

The effect of receipt of this primitive is specified in 98.4.1.

97.2.2 PMA service interface

1000BASE-T1 uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indication (tx_mode)
PMA_CONFIG.indication (config)
PMA_UNITDATA.request (tx_symb)
PMA_UNITDATA.indication (rx_symb)
PMA_SCRSTATUS.request (scr_status)
PMA_PCSSTATUS.request (pcs_status)
PMA_RXSTATUS.indication (loc_rcvr_status)
PMA_DATAREADY.indication (loc_data_ready)
PMA_REMRXSTATUS.request (rem_rcvr_status)
PMA_REMDATAREADY.request (rem_data_ready)
PMA_RESET.indication()

The use of these primitives is illustrated in Figure 97–3. Connections from the management interface (signals MDC and MDIO) to the sublayers are pervasive and are not shown in Figure 97–3.

EEE-capable PHYs additionally support the following service primitives:

PMA_PCS_RX_LPI_STATUS.request (rx_lpi_active)
PMA_PCS_TX_LPI_STATUS.request (tx_lpi_active)

97.2.2.1 PMA_TXMODE.indication

The transmitter in a 1000BASE-T1 link normally sends over the MDI symbols that represent a GMII data stream with framing, scrambling and encoding of data, control information, or idles.

97.2.2.1.1 Semantics of the primitive

PMA_TXMODE.indication (tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of code-groups the PCS should be transmitting. The parameter tx_mode can take on one of the following four values of the form:

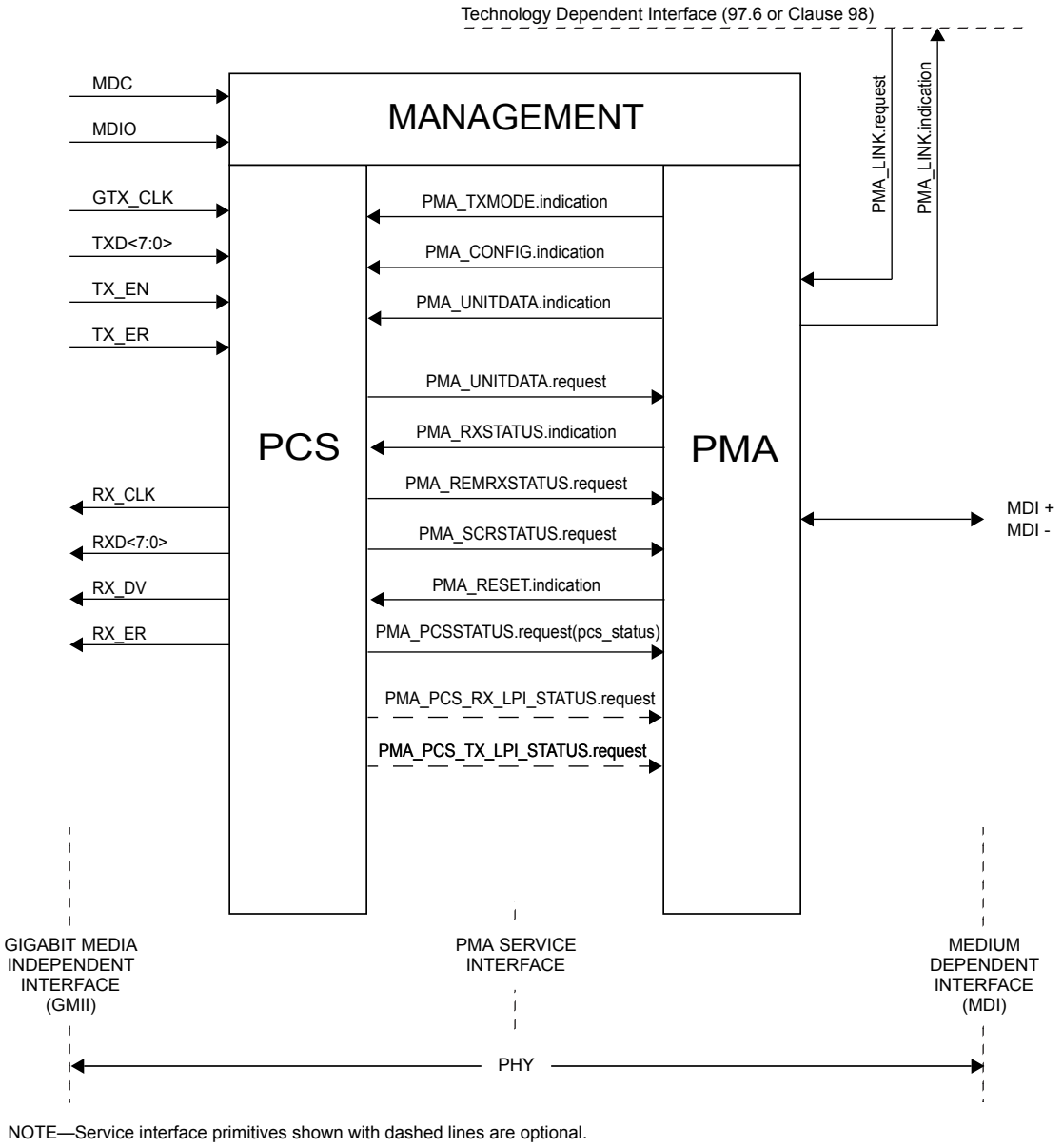
SEND_N	This value is continuously asserted during transmission of sequences of symbols representing a GMII data stream in data mode.
SEND_I	This value is continuously asserted when transmission of sequences of idle symbols is to take place.
SEND_T	This value is continuously asserted in case transmission of sequences of code-groups representing the training mode is to take place.
SEND_Z	This value is continuously asserted in case transmission of zeros is required.

97.2.2.1.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

97.2.2.1.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 97.3.2.2.



NOTE—Service interface primitives shown with dashed lines are optional.

Figure 97–3—1000BASE-T service interfaces

97.2.2.2 PMA_CONFIG.indication

Each PHY in a 1000BASE-T1 link is capable of operating as a MASTER PHY and as a SLAVE PHY. If the Auto-Negotiation process is enabled, PMA_CONFIG MASTER-SLAVE configuration is determined during Auto-Negotiation (Clause 98) and the result is provided to the PMA. If the Auto-Negotiation process is not enabled, PMA_CONFIG MASTER-SLAVE configuration is pre-determined to be Master or Slave via management control during initialization or via default hardware set-up.

97.2.2.2.1 Semantics of the primitive

PMA_CONFIG.indication (config)

PMA_CONFIG.indication specifies to PCS and PMA Transmit via the parameter config whether the PHY operates as a MASTER PHY or as a SLAVE PHY. The parameter config can take on one of the following two values of the form:

MASTER	This value is continuously asserted when the PHY operates as a MASTER PHY.
SLAVE	This value is continuously asserted when the PHY operates as a SLAVE PHY.

97.2.2.2.2 When generated

PMA generates PMA_CONFIG.indication messages to indicate a change in config.

97.2.2.2.3 Effect of receipt

PCS and PMA Clock Recovery perform their functions in MASTER or SLAVE configuration according to the value assumed by the parameter config.

97.2.2.3 PMA_UNITDATA.request

This primitive defines the transfer of code-groups in the form of the tx_symb parameter from the PCS to the PMA. The code-groups are obtained in the PCS Transmit function using the encoding rules defined in 97.3.2.2 to represent GMII data and control streams or other sequences.

97.2.2.3.1 Semantics of the primitive

PMA_UNITDATA.request (tx_symb)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb the value of the symbols to be sent over the MDI. The tx_symb may take on one of the values in the set { –1, 0, 1 }

97.2.2.3.2 When generated

The PCS generates PMA_UNITDATA.request (tx_symb) synchronously with every transmit clock cycle.

97.2.2.3.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols after processing with optional transmit filtering and other specified PMA Transmit processing. The parameter tx_symb is also used by the PMA Receive function to process the signals received on the MDI for cancelling the echo.

97.2.2.4 PMA_UNITDATA.indication

This primitive defines the transfer of code-groups in the form of the rx_symb parameter from the PMA to the PCS.

97.2.2.4.1 Semantics of the primitive

PMA_UNITDATA.indication (rx_symb)

During reception the PMA_UNITDATA.indication conveys to the PCS via the parameter rx_symb the value of symbols detected on the MDI during each cycle of the recovered clock.

97.2.2.4.2 When generated

The PMA generates PMA_UNITDATA.indication (rx_symb) messages synchronously for every symbol received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive is 750 MHz, as governed by the recovered clock.

97.2.2.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

97.2.2.5 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the training mode descrambler has achieved synchronization.

97.2.2.5.1 Semantics of the primitive

PMA_SCRSTATUS.request (scr_status)

The scr_status parameter can take on one of two values of the form:

OK	The training mode descrambler has achieved synchronization.
NOT_OK	The training mode descrambler is not synchronized.

97.2.2.5.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

97.2.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 97.4.2.4 and 97.4.2.5.

97.2.2.6 PMA_PCSSTATUS.request

This primitive is generated by PCS Receive to indicate the fully operational state of the PCS for the local PHY. The parameter pcs_status conveys to the PMA Receive function the information that the PCS is operating reliably in data mode.

97.2.2.6.1 Semantics of the primitive

PMA_PCSSTATUS.request (pcs_status)

The pcs_status parameter can take on one of two values of the form:

OK	The PCS is operating reliably in data mode.
NOT_OK	The PCS is not operating reliably in data mode.

97.2.2.6.2 When generated

PCS Receive generates PMA_PCSSTATUS.request messages to indicate a change in pcs_status.

97.2.2.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 97.4.2.5.9 and 97.4.5.

97.2.2.7 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criterion for setting the parameter loc_rcvr_status is left to the implementor. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol stream.

97.2.2.7.1 Semantics of the primitive

PMA_RXSTATUS.indication (loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the form:

OK	This value is asserted and remains true during reliable operation of the receive link for the local PHY.
NOT_OK	This value is asserted whenever operation of the link for the local PHY is unreliable.

97.2.2.7.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages to indicate a change in loc_rcvr_status on the basis of signals received at the MDI.

97.2.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 97–22, 97.3.2.3, 97.4.2.5, and 97.4.5.

97.2.2.8 PMA_DATAREADY.indication

This primitive is generated by PMA Receive to indicate the local PHY is ready or not ready to receive data. The parameter loc_data_ready is conveyed to the link partner by the PCS as defined in Table 97-1.

97.2.2.8.1 Semantics of the primitive

PMA_DATAREADY.indication (loc_data_ready)

The loc_data_ready parameter can take on one of two values of the form:

OK	The local PHY is ready to receive data.
NOT_OK	The local PHY is not ready to receive data.

97.2.2.8.2 When generated

PMA Receive generates PMA_DATAREADY.indication messages to indicate a change in loc_data_ready based on loc_rcvr_status and pcs_status values.

97.2.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 97–22 and Figure 97-23.

97.2.2.9 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The parameter rem_rcvr_status is set to the value received in the loc_rcvr_status bit in the InfoField from the remote PHY. The rem_rcvr_status is set to NOT_OK if the PCS has not decoded a valid InfoField from the remote PHY.

97.2.2.9.1 Semantics of the primitive

PMA_REMRXSTATUS.request (rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK	The receive link for the remote PHY is operating reliably.
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected.

97.2.2.9.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages to indicate a change in rem_rcvr_status based on the PCS decoding the loc_rcvs_status bit in InfoField messages received from the remote PHY during training.

97.2.2.9.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 97–22.

97.2.2.10 PMA_REMDATAREADY.request

This primitive is generated by PCS Receive to indicate whether the remote PHY is ready or not ready to receive data. Its value is received from the link partner by the PCS as defined in Table 97-1.

97.2.2.10.1 Semantics of the primitive

PMA_REMDATAREADY.request (rem_data_ready)

The rem_data_ready parameter can take on one of two values of the form:

OK	The remote PHY is ready to receive data.
NOT_OK	The remote PHY is not ready to receive data.

97.2.2.10.2 When generated

The PCS generates PMA_REMDATAREADY.request messages to indicate a change in rem_data_ready based on the PCS decoding the control words in Table 97-1 received from the remote PHY.

97.2.2.10.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 97–22.

97.2.2.11 PMA_RESET.indication

This primitive is used to pass the PMA Reset function to the PCS (pcs_reset=ON) when reset is enabled.

The PMA_RESET.indication primitive can take on one of two values:

TRUE Reset is enabled.
FALSE Reset is not enabled.

97.2.2.11.1 When generated

The PMA Reset function is executed as described in 97.4.2.1.

97.2.2.11.2 Effect of receipt

The effect of receipt of this primitive is specified in 97.4.2.1.

97.2.2.12 PMA_PCS_RX_LPI_STATUS.request

When the PHY supports the EEE capability this primitive is generated by the PCS receive function to indicate the status of the receive link at the local PHY. The parameter PMA_PCS_RX_LPI_STATUS.request conveys to the PCS transmit and PMA receive functions information regarding whether the receive function is in the LPI receive mode.

97.2.2.12.1 Semantics of the primitive

PMA_PCS_RX_LPI_STATUS.request (rx_lpi_active)

The rx_lpi_active parameter can take on one of two values of the form:

TRUE	The receive function is in the LPI receive mode.
FALSE	The receive function is not in the LPI receive mode.

97.2.2.12.2 When generated

The PCS generates PMA_PCS_RX_LPI_STATUS.request messages to indicate a change in the rx_lpi_active variable as described in 97.3.2.3 and 97.3.6.2.2.

97.2.2.12.3 Effect of receipt

The effect of receipt of this primitive is specified in 97.3.6.4.

97.2.2.13 PMA_PCS_TX_LPI_STATUS.request

When the PHY supports the EEE capability this primitive is generated by the PCS transmit function to indicate the status of the transmit link at the local PHY. The parameter PMA_PCS_TX_LPI_STATUS.request conveys to the PCS transmit and PMA receive functions information regarding whether the transmit function is in the LPI transmit mode.

97.2.2.13.1 Semantics of the primitive

PMA_PCS_TX_LPI_STATUS.request (tx_lpi_active)

The tx_lpi_active parameter can take on one of two values of the form:

TRUE	The transmit function is in the LPI transmit mode.
FALSE	The transmit function is not in the LPI transmit mode.

97.2.2.13.2 When generated

The PCS generates PMA_PCS_TX_LPI_STATUS.request messages to indicate a change in the tx_lpi_active variable as described in 97.3.5 and 97.3.6.2.2.

97.2.2.13.3 Effect of receipt

The effect of receipt of this primitive is specified in 97.3.6.4.

97.3 Physical Coding Sublayer (PCS)

Editor's Note: Text written in italics are not approved baseline and are included only for placeholder information. The text will be change to match approved baseline when selected.

97.3.1 PCS service interface (GMII)

The PCS service interface allows the 1000BASE-T1 PCS to transfer information to and from a PCS client. The PCS Interface is precisely defined as the Gigabit Media Independent Interface (GMII) in Clause 35.

97.3.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions. The PCS operating functions are: PCS Transmit and PCS Receive. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram, Figure 97–4, shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 97–4.

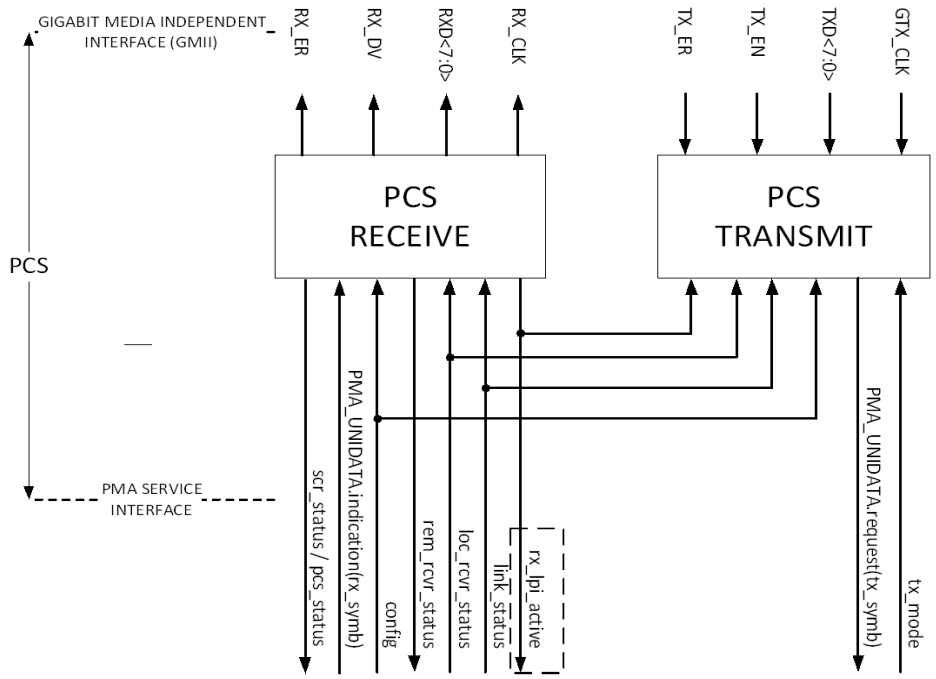


Figure 97–4—PCS reference diagram

97.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on.
b) The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset=ON while any of the above reset conditions hold true (see 97.3.6.2.2). All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

97.3.2.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS 80B/81B Transmit state diagram in Figure 97–14 and the PCS Transmit bit ordering in Figure 97–5 and Figure 97–7.

When communicating with the GMII, the PCS uses an octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. Alignment to 80B/81B blocks is performed in the PCS. The PMA sublayer operates independently of block and packet boundaries. The PCS provides the functions necessary to map packets between the GMII format and the PMA service interface format.

When the transmit channel is in data mode, the PCS Transmit process continuously generates 81B blocks based upon the TXD <7:0>, TX_EN and TX_ER signals on the GMII. The subsequent functions of the PCS Transmit process then pack the resulting blocks plus one OAM symbol, both of which are then processed by a Reed-Solomon (RS) encoder and subsequently 3B2T mapped into a transmit RS frame of PAM3 symbols.

Transmit data-units are sent to the PMA service interface via the PMA_UNITDATA.request primitive. A symbol period, T, is 4/3 ns.

If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit generates sequences of codes defined in 97.3.4.2 to the PMA via the PMA_UNITDATA.request primitive. These codes are used for training mode and only transmit the values {–1, +1}.

During training mode an InfoField is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner. (See 97.4.2.5.)

In the data mode of operation, the PMA_TXMODE.indication message has the value SEND_N, and the PCS Transmit function uses an 81B-RS coding technique to generate at each symbol period code-groups that represent data or control. During transmission, 45 81B blocks shall be aggregated, encoded by a RS frame encoder, and then scrambled by a PCS scrambler. During data encoding PCS Transmit frames shall be encoded into a sequence of PAM3 symbols and transferred to the PMA.

Dashed rectangles in Figure 97–14 indicate states and state transitions in the transmit process state diagram that shall be supported by PHYs with the EEE capability. PHYs without the EEE capability do not support these transitions.

After reaching the data mode of operation, EEE-capable PHYs may enter the LPI transmit mode under the control of the MAC via the GMII. The EEE Transmit state diagram is contained within the PCS Transmit function. The EEE capability is described in 97.3.2.2.16.

97.3.2.2.1 Use of blocks

The PCS maps GMII signals into 81-bit blocks inserted into an RS frame, and vice versa, using an 81B-RS coding scheme. The *PAM2* PMA training frame synchronization allows establishment of RS frame and 81B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 97.3.2.2.2.

97.3.2.2.2 81B-RS transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters. The encoding defined by the transmission code ensures that sufficient information is present in the PHY bit stream to make clock recovery possible at the receiver. The encoding also preserves the likelihood of detecting any RS frame errors that may occur during transmission and reception of information. In addition, the code enables the receiver to achieve PCS synchronization alignment on the incoming PHY bit stream.

The relationship of block bit positions to GMII, PMA, and other PCS constructs is illustrated in Figure 97–5 for transmit and Figure 97–6 for receive. These figures illustrate the processing of a multiplicity of blocks containing 10 data octets. See 97.3.2.2.5 for information on how blocks containing control characters are mapped.

97.3.2.2.3 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

80B/81B encodes 10 data octets or control characters into an 81B block.

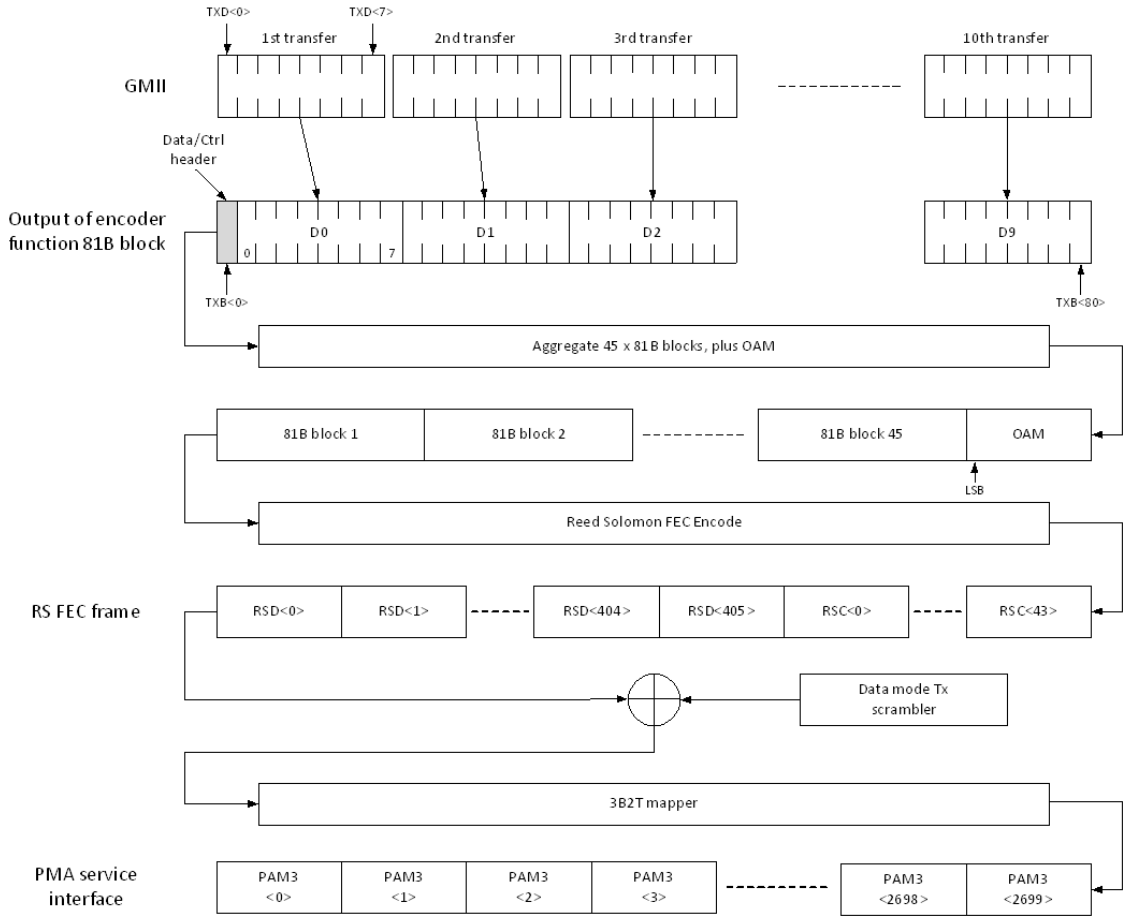


Figure 97–5—PCS Transmit bit ordering

97.3.2.2.4 Transmission order

The PCS Transmit bit ordering shall conform to Figure 97–5 and Figure 97–7. Note that these figures show the mapping from GMII to 80B/81B block for a block containing ten data characters. The LSB of the OAM symbol is transmitted first.

97.3.2.2.5 Block structure

Blocks consist of 81 bits. The first bit of a block is the data/ctrl header. Blocks are either data blocks or control blocks. The data/ctrl header is 0 for data blocks and 1 for control blocks. The remainder of the block contains the payload.

Data blocks contain ten data octets. Control blocks begin with a 5-bit pointer field that indicates the location of the first control code within the block. Bit 0 to 3 of pointer points to next octet that is a control symbol. Bit 4 of pointer indicates whether the next control symbol is the final control symbol of the block: 0 = final, 1 = more control symbols. If the first octet in the block is a control character, the pointer field is followed by a 3-bit control code. Otherwise the pointer field is followed by one or more data octets until the position of the first control code. Then the 3-bit control code indicates type of control character. The control code is followed by a 5-bit pointer field to the next control character if the prior pointer field value was greater than 15 (i.e. bit 4 = 1). The pointer field may be followed by a data octet or control code depending on the value of

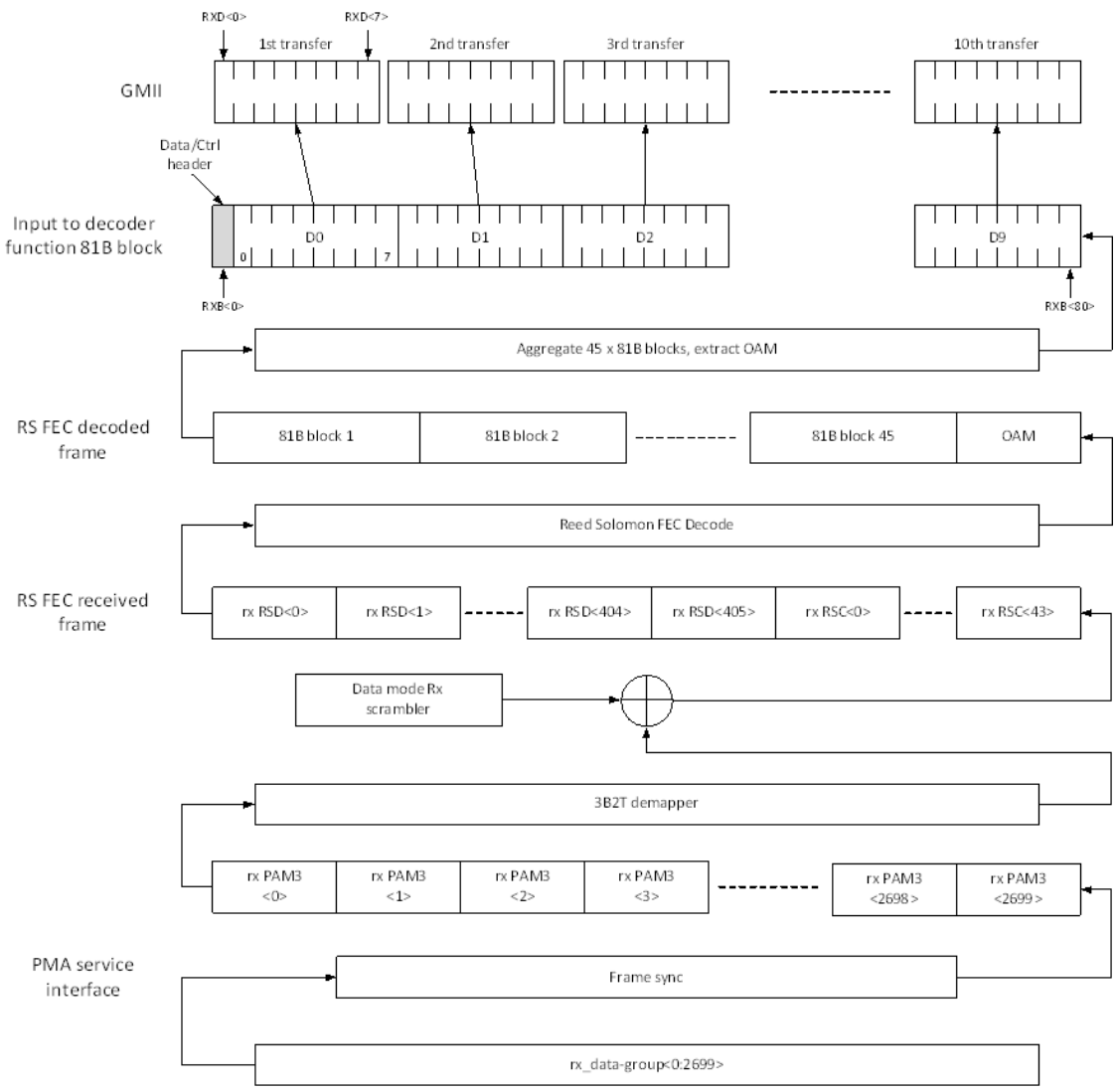


Figure 97–6—PCS Receive bit ordering

the pointer field. In this way any combination of ten data octets and control characters may be encapsulated within an 81B block.

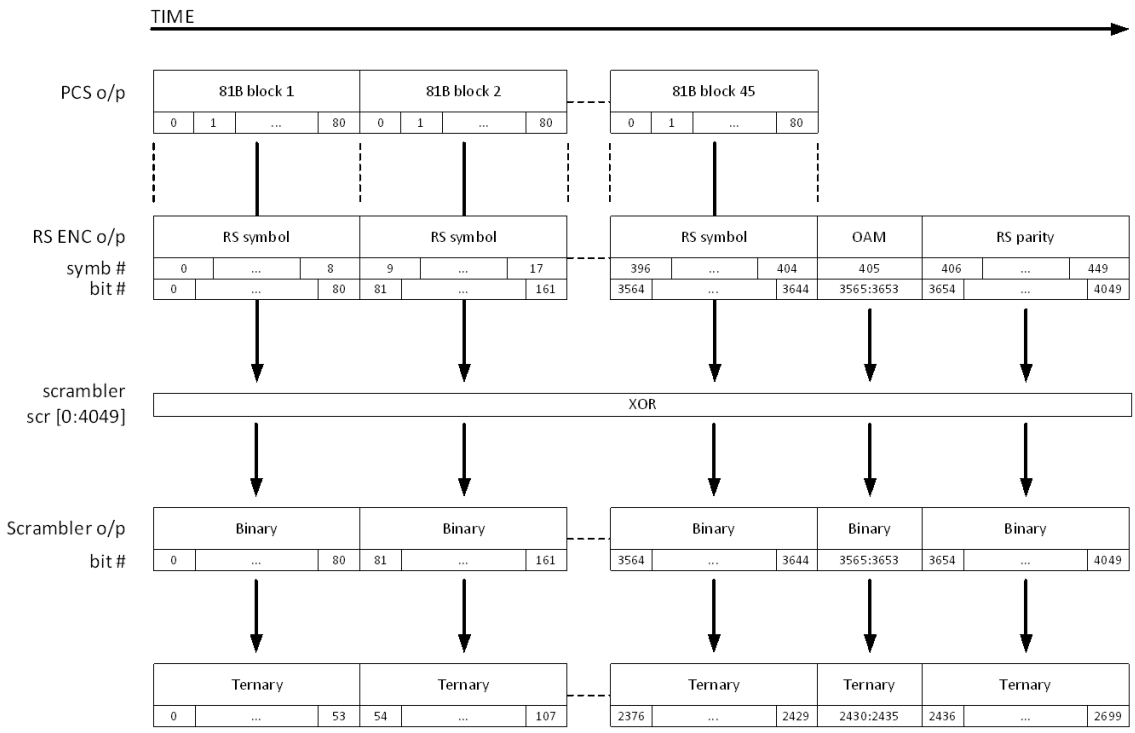


Figure 97–7—PCS detailed transmit bit ordering

The 81B block encoding is defined by the following equations where N = 10.

N = number of GMII octets encoded into block
octets numbered n = 0, 1, 2, …, N-1. octet 0 is the first one presented on GMII.
TC[n] = 0 if octet n is data octet on GMII, 1 if octet n is control octet on GMII
TC[-1] = 1 by definition
TD[n][0:7] = GMII octet n TXD[0:7] if TC[n] = 0
TD[n][5:7] = 000 or 010 – IPG, 101 – LPI, 001 – TX Error if TC[n] = 1. TD[n][0:4] is undefined.
B[0:8N] is the 8N+1 block. Bit 0 transmitted first.
OR(n) = Bitwise OR of TC[n:N-1]
NEXT(n)[0:3] = bit position of lowest bit in TC[n:N-1] that is a 1. Bit 3 is MSB.
NEXT(n)[4] = 0 if Bitwise SUM of TC[n:N-1] = 1, else 1

B[0] = OR(0)

B[8n+1:8n+4] = TD[n][0:3] – if OR(n) = 0
NEXT(n)[0:3] – if OR(n) = 1 AND TC[n-1] = 1
TD[n-1][3:6] – if OR(n) = 1 AND TC[n-1] = 0

B[8n+5] = TD[n][4] – if OR(n) = 0
NEXT(n)[4] – if OR(n) = 1 AND TC[n-1] = 1
TD[n-1][7] – if OR(n) = 1 AND TC[n-1] = 0

B[8n+6:8n+8] = TD[n][5:7] – if OR(n) = 0
TD[n][5:7] – if OR(n) = 1 AND TC[n] = 1
TD[n][0:2] – if OR(n) = 1 AND TC[n] = 0

97.3.2.2.6 Control codes

A subset of control characters defined at the GMII are supported by the 1000BASE-T1 PCS. When TX_ER and TX_EN are both asserted, the 1000BASE-T1 PCS conveys an Error symbol in the 80B81B block code. When TX_EN is not asserted and no other supported control code is present at the GMII, the 1000BASE-T1 PCS will convey and Idle symbol in the 80B81B block code.

The control characters and their mappings to 1000BASE-T1 control code and GMII control code are specified in Table 97–1. All GMII and 1000BASE-T1 control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received.

Table 97–1—GMII Control Code Mapping

Control Code[0:2]	GMII Transmit	GMII Receive
000	Normal Inter-Frame with loc_data_ready=NOT_OK	Normal Inter-Frame with rem_-data_ready=NOT_OK
001	Transmit Error Propagation	Data Reception Error
010	Normal Inter-Frame with loc_data_ready=OK	Normal Inter-Frame with rem_data_ready=OK
101	Assert Low Power Idle	Assert Low Power Idle
other	Reserved	Reserved

The Carrier Extend and Carrier Extend Error, and Reserved transactions, if any occurred, are assigned to ~~the Control Code<0:2> of 010,~~ Normal inter-frame~~,~~ in the PCS 80B/81B Encoder.

97.3.2.2.7 Valid and invalid blocks

A block is invalid if any of the following conditions exists:

a) The block contains an invalid pointer.
b) Any control character contains a value not in Table 97–1.
c) The RS frame containing this 80B/81B block is uncorrectable.

97.3.2.2.8 Idle

Idle (Normal Inter-frame) control characters are transmitted when TX_EN is not asserted and no other supported control code is present at the GMII. Idle characters may be added or deleted by the PCS to adapt between clock rates.

97.3.2.2.9 LP_IDLE

The low power idle control characters (LP_IDLEs) are transmitted when TX_EN is not asserted, TX_ER is asserted, and TXD<7:0> = 0x1. A continuous stream of LPI control characters is used to maintain a link in the LPI transmit mode. Idle control characters are used to transition from the LPI transmit mode to the normal mode. EEE compliant PHYs respond to the Assert Low Power Idle condition on the GMII using the procedure outlined in 97.1.2.4.

If EEE is not supported, then LP_IDLE shall be converted to IDLE.

97.3.2.2.10 Error

The Error control code is sent when TX_ER and TX_EN are both asserted. It is also sent when invalid blocks are received. Error allows physical sublayers such as the PCS to propagate received errors.

97.3.2.2.11 Transmit process

The transmit process generates blocks based upon the TXD<7:0>, TX_EN and TX_ER signals received from the GMII. Ten GMII data transfers are encoded into each block. It takes 2700 PMA_UNITDATA transfers to send an RS frame of data. Where the GMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process needs to insert idles, or delete idles to adapt between the rates.

The transmit process generates blocks as specified in the transmit process state diagram. The contents of each block are contained in a vector tx_coded<80:0>, which is aggregated with 45 81B blocks and OAM, then passed to the Reed Solomon FEC Encoder and then finally passed to the scrambler. tx_coded<0> contains the data/ctrl header and the remainder of the bits contain the block payload.

97.3.2.2.12 RS encoder

The 1000BASE-T1 PCS shall encode the transmitted data stream using Reed-Solomon code (450,406). The RS encoder shall follow the notation described in 97.3.2.2.3 where the LSB is the first bit into the RS encoder and the first transmitted bit.

The FEC code used for 1000BASE-T1 links is a shortened Reed-Solomon (450,406) code over the Galois Field of GF(2^9)—a code operating on 9 bit symbols, as shown in Figure 97–8. The code encodes 406 information symbols and adds 44 parity symbols. The code is systematic, meaning that the information symbols are not disturbed in any way in the encoder and the parity symbols are added separately to each block.

The code is based on the generating polynomial shown in Equation (97–1).

$$G(Z) = \prod_{i=0}^{43} (Z - \alpha^i) = A_{44}Z^{44} + A_{43}Z^{43} + \ldots + A_0Z^0 \quad (97\text{–}1)$$

where

α is a root of the binary primitive polynomial $x^9 + x^4 + 1$ and is represented as 0x002
A is a series representing the resulting polynomial coefficients of $G(Z)$, (A_{44} is equal to 0x001)
Z corresponds to an 9 bit GF(2^9) symbol
x corresponds to a bit position in a GF(2^9) symbol

The parity calculation shall produce the same result as the shift register implementation shown in Figure 97–8. Before calculation begins, the shift register shall be initialized to zero. The contents of the shift register are transmitted without inversion.

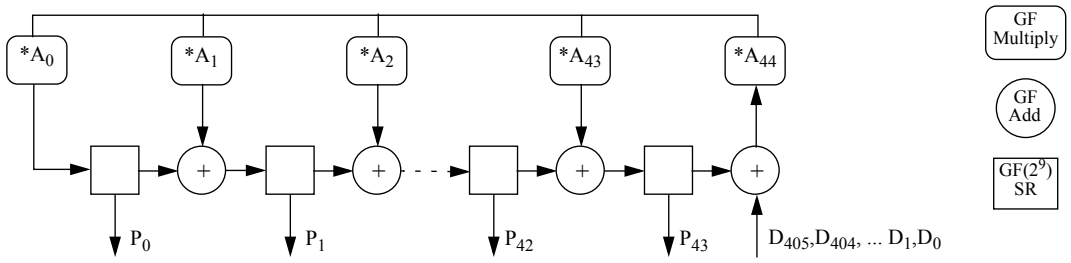


Figure 97–8—Circuit for generating FEC parity vector

A FEC parity vector is represented by Equation (97–2).

$$P(Z) = D(Z) \bmod G(Z) \quad (97\text{–}2)$$

where

$D(Z)$ is the data vector $D(Z) = D_{405}Z^{449} + D_{404}Z^{448} + \ldots + D_0Z^{44}$. D_{405} is the first 9-bit data symbol and D_0 is the last.

$P(Z)$ is the parity vector $P(Z) = P_{43}Z^{43} + P_{42}Z^{42} \ldots + P_0Z^0$. P_{43} is the first 9-bit parity symbol and P_0 is the last.

A data symbol $(d_8, d_7, \ldots, d_1, d_0)$ is identified with the element: $d_8\alpha^8 + d_7\alpha^7 + \ldots + d_1\alpha^1 + d_0$ in GF(2^9), the finite field with 2^9 elements. The code has a correction capability of up to twenty-two symbols.

The d_0 is identified as the LSB and d_8 is identified as the MSB for all symbols.

The resulting payload of scrambled 45 81B blocks, followed by the OAM symbol results in a total payload of 3654 bits. The resulting RS block size is 450 9-bit symbols, a total of 4050 bits. Figure 97–9 shows the bit mapping between PCS and FEC.

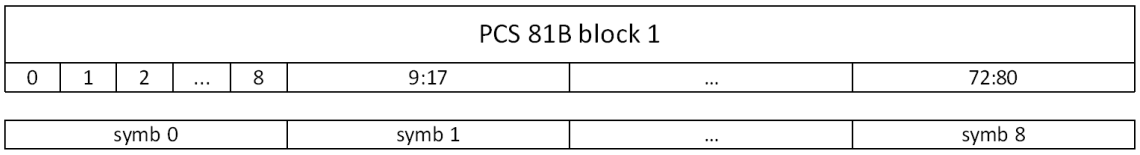


Figure 97–9—PCS to FEC bit mapping

97.3.2.2.13 PCS scrambler

The PCS Transmit function employs side-stream scrambling. The scrambler for the MASTER shall produce the same result as the implementation shown in Figure 97–10. This implements the scrambler polynomial:[1]

$$G(x) = 1 + x^4 + x^{15} \tag{97–3}$$

The scrambler for the SLAVE shall produce the same result as the implementation shown in Figure 97–10. This implements the scrambler polynomial:

$$G(x) = 1 + x^{11} + x^{15} \tag{97–4}$$

The initial seed values for the MASTER and SLAVE scramblers are left to the implementor. The seed values shall be non-zero and shall be transmitted during the InfoField exchange. (See 97.4.2.5.5). The scrambler is run continuously on all RS frame output bits.

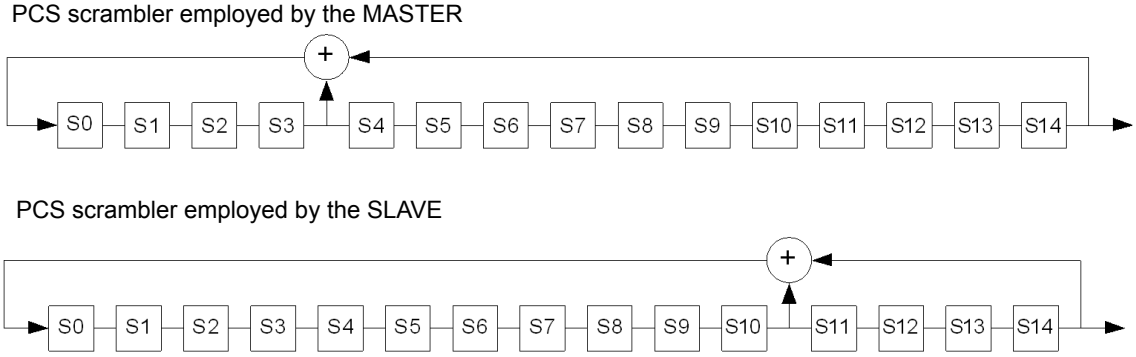


Figure 97–10—MASTER and SLAVE PCS scramblers

97.3.2.2.14 3B2T to PAM3

The 3B2T mapper generates 2700 PAM3 symbols per RS frame that are sent to the PMA via PMA_UNITDATA.request. Every 9-bit symbol is divided into three 3-bit groups with the LSB bits as the first group. Each 3-bit group is then mapped by the 3B2T into 2 PAM3 symbols. The mapping of 3B2T to PAM3 is illustrated in Table 97–2. B[0] is the LSB and T[0] is the first PAM3 symbol transmitted.

[1]The convention here, which considers the most recent bit into the scrambler to be the lowest order term, is consistent with most references and with other scramblers shown in this standard. Some references consider the most recent bit into the scrambler to be the highest order term and would therefore identify this as the inverse of the polynomial in Equation (97–3). In case of doubt, note that the conformance requirement is based on the representation of the scrambler in the figure rather than the polynomial equation.

Table 97–2—3B2T Mapping to PAM3

B[2], B[1], B[0]	T[1], T[0]
000	-1,-1
001	0,-1
010	-1,0
011	-1,+1
100	+1,0
101	+1,-1
110	+1,+1
111	0,+1

97.3.2.2.15 81B-RS framer

The 81B-RS framer adapts between the 81-bit width of the 81B blocks and the PAM3 input to the PMA. When the transmit channel is operating in data mode, the 81B-RS sends one PAM3 symbol of transmit data at a time via PMA_UNITDATA.request primitives. The PMA_UNITDATA.request primitives are fully packed with bits.

97.3.2.2.16 EEE capability

The optional 1000BASE-T1 EEE capability allows compliant PHYs to transition to an LPI mode of operation when link utilization is low. EEE compliant PHYs shall implement the transmit state diagram including the EEE portion, noted by dotted lines in Figure 97–14, within the PCS.

When there is an Assert Low Power Idle while in the SEND_DATA state the PHY transmits the sleep signal to indicate to the link partner that it is transitioning to the SEND_LPI state. The sleep signal is one RS frame composed entirely of LP_IDLE characters. If the LP_IDLE character occurs in the last 80B/81B block then the sleep signal is the next RS frame. The PHY shall transmit no RS frames partially filled with LP_IDLES.

Following the transmission of the sleep signal, quiet-refresh signaling begins, as described in 97.3.5.

While the PMA asserts SEND_N, the lpi_tx_mode variable shall control the transmit signal through the PMA_UNITDATA.request primitive described as follows:

> When the PMA_TXMODE.indication message does not have the value of SEND_N, the lpi_tx_-mode variable is ignored.
>
> When the lpi_tx_mode variable takes the value NORMAL the PCS passes coded data to the PMA via the PMA_UNITDATA.request primitive.
>
> When the lpi_tx_mode variable takes the value QUIET the PCS passes zeros to the PMA through the PMA_UNITDATA.request primitive.
>
> When the lpi_tx_mode variable takes the value REFRESH, the PCS passes zero data encoded through PCS data path to the PMA via the PMA_UNITDATA.request primitive.

The quiet-refresh cycle is repeated until Assert Low Power Idle is not detected at the GMII. This indicates that the local system is requesting a transition back to the normal power mode. At the next RS frame the PCS transmits a wake frame composed of an entire RS frame containing only Idle. The wake frame shall be sent only during alternating RS frame counts.

Due to the wake signal constrained to occur at the beginning of every second RS frame boundary the PHY wake time may range from 3.6 µs to 10.8 µs (lpi_wake_timer=T_{w_phy} as defined by Clause 78).

97.3.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 80B/81B receive state diagram in Figure 97–15 and the PCS Receive bit ordering in Figure 97–6 including compliance with the associated state variables as specified in 97.3.6.

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the PMA training alignment to correctly align the 81B-RS frames. The received 81B-RS frames are decoded with error correction; the framing is checked; and the 80B/81B ordered sets are converted to 10 data octets to obtain the signals RXD<7:0>, RX_DV and RX_ER for transmission to the GMII.

During PMA training mode, PCS Receive checks the received PAM2 framing and signals the reliable acquisition of the descrambler state by setting the parameter scr_status to OK.

When the PCS Synchronization process has obtained synchronization, the RS frame error rate (RFER) monitor process monitors the signal quality asserting hi_rfer if excessive RS frame errors are detected (RS parity error). If 40 consecutive RS frame errors are detected, the block_lock flag is de-asserted. When block_lock is asserted and hi_rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD<7:0>, RX_DV and RX_ER for transmission to the GMII.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication (loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.request primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training sequence includes 1 bit pattern every 180 PAM2 symbols, which is aligned with the PCS Partial RS frame boundary, as well as an InfoField which is inserted in the 15th PCS Partial RS frame. When the PCS Synchronization process is synchronized to the RS frame boundary using this pattern, block_lock is asserted.

PHYs with the EEE capability support transition to the LPI mode when the PHY has successfully completed training. Transitions to and from the LPI mode are allowed to occur independently in the transmit and receive functions. The PCS receive function is responsible for detecting transitions to and from the LPI receive mode and indicating these transitions using signals defined in 97.3.6.

The link partner signals a transition to the LPI mode of operation by transmitting one frame composed entirely of 80B/81B blocks of LP_IDLES. When blocks of LP_IDLES are detected at the output of the 80B/81B decoder, rx_lpi_active is asserted by the PCS receive function and the LPI character is continuously asserted at the receive GMII. After the sleep frame the link partner begins transmitting zeros, and it is recommended that the receiver power down receive circuits to reduce power consumption. The receive function uses RS frame counters to maintain synchronization with the remote PHY and receives periodic refresh signals that are used to update coefficients, so that the integrity of adaptive filters and timing loops in the PMA is maintained. LPI signaling is defined in 97.3.5. The quiet-refresh cycle continues until the PHY detects the wake frame. The PHY receive function sends Idles to the GMII for the remainder of the wake frame and then resumes normal power mode operation.

97.3.2.3.1 Frame and block synchronization

When the receive channel is operating in data mode, the frame and block synchronization function receives data via PAM3 PMA_UNITDATA.indication primitive. It shall form a PAM3 stream from the primitive by concatenating requests in order from rx_data<0> to rx_data<2699> (see Figure 97–6). It obtains block lock to the RS frames during the PAM2 training pattern using synchronization bits provided in the training sequence.

97.3.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. The PHY shall descramble the data stream and return the proper sequence of code-groups to the decoding process for generation of RXD<7:0> to the GMII. For side-stream descrambling, the MASTER PHY shall employ the receiver descrambler generator polynomial per Equation (97–4) and the SLAVE PHY shall employ the receiver descrambler generator polynomial per Equation (97–3).

97.3.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, the channel and remote receiver. When the transmit PCS is operating in test-pattern mode it shall transmit continuously as illustrated in Figure 97–5, with the input to the scrambler set to zero and the initial condition of the scrambler set to any non-zero value. When the receiver PCS is operating in test-pattern mode it shall receive continuously as illustrated in Figure 97–6. The output of the received descrambled values should be zero. Any nonzero values correspond to receiver bit errors. This mode is further described as test mode 7 in 97.5.2.

97.3.4 PMA training side-stream scrambler polynomials

The PCS Transmit function employs side-stream scrambling. If the parameter config provided to the PCS by the PMA PHY Control function via the PMA_CONFIG.indication message assumes the value MASTER, PCS Transmit shall employ Equation (97–5).

$$g_M(x) = 1 + x^{13} + x^{33} \tag{97–5}$$

as transmitter side-stream scrambler generator polynomial. If the PMA_CONFIG.indication message assumes the value of SLAVE, PCS Transmit shall employ Equation (97–6).

$$g_S(x) = 1 + x^{20} + x^{33} \tag{97–6}$$

as transmitter side-stream scrambler generator polynomial. An implementation of master and slave PHY side-stream scramblers by linear-feedback shift registers is shown in Figure 97–10. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit

vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros.

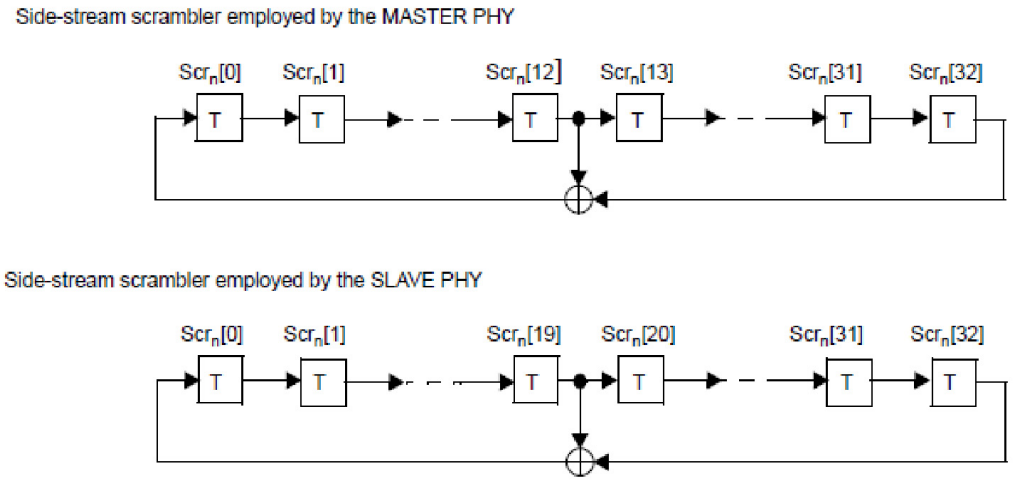


Figure 97–11—A realization of side-stream scramblers by linear feedback shift registers

97.3.4.1 Generation of S_n

During PMA training, the training pattern is embedded with indicators to establish alignment to the RS FEC block and the 15 partial frames that comprise the block. The last partial frame is embedded with an information field used to exchange messages between link partners. PMA training signal encoding is based on the generation, at time n, of the bit S_n. The first bit is inverted in the first 14 partial frames of each RS FEC block. The first 96 bits of the 15th partial frame is XOR'd with the contents of the Infofield.

$$S_n = \begin{cases} Scr_n[0] \oplus 1 Infofield_{(nmod180)} & 2519 < (nmod2700) < 2616 \\ Scr_n[0] \oplus 1 & (nmod180) = 0 \\ Scr_n[0] & otherwise \end{cases} \quad (97–7)$$

97.3.4.2 Generation of symbol T_n

The bit S_n is mapped to the transmit symbol T_n as follows: if $S_n = 0$ then $T_n = +1$, if $S_n = 1$ then $T_n = -1$.

97.3.4.3 PMA training mode descrambler polynomials

The PHY shall acquire descrambler state synchronization to the PAM2 training sequence and report success through scr_status. For side-stream descrambling, the MASTER PHY shall employ the receiver descrambler generator polynomial same as Equation (97–6) and the SLAVE PHY shall employ the receiver descrambler generator polynomial same as Equation (97–5).

97.3.5 LPI signaling

PHYs with EEE capability have transmit and receive functions that can enter and leave the LPI mode independently. The PHY can transition to the LPI mode when the PHY has successfully completed training. The transmit function of the PHY initiates a transition to the LPI transmit mode when it generates a sleep signal composed of 80B/81B blocks containing only LPI control characters, as described in 97.3.2.2.16.

When the transmitter begins to send the sleep signal, it asserts tx_lpi_active and the transmit function enters the LPI transmit mode.

Within the LPI mode PHYs use a repeating quiet-refresh cycle (see Figure 97–12). The first part of this cycle is known as the quiet period and lasts for a time lpi_quiet_time equal to 354 partial RS frame periods. The quiet period is defined in 97.3.5.2. The second part of this cycle is known as the refresh period and lasts for a time lpi_refresh_time equal to 6 partial RS frame periods. The refresh period is defined in 97.3.5.3. A cycle composed of one quiet period and one refresh period is known as an LPI cycle and lasts for an lpi_qr_time equal to 24*15 = 360 partial RS frame periods.

lpi_offset, lpi_quiet_time, lpi_refresh_time, and lpi_qr_time are timing parameters that are integer multiples of the partial RS frame period. lpi_offset is a fixed value equal to lpi_qr_time/2 + 15. It is used to ensure refresh signals and wake start times are appropriately offset by the link partners.

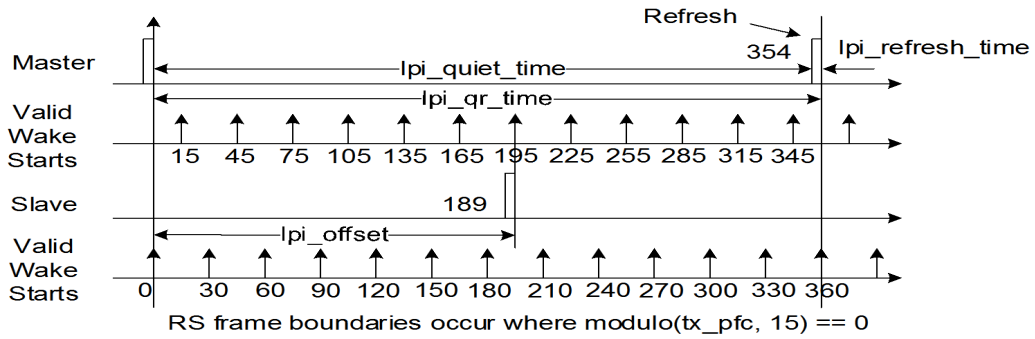


Figure 97–12—LPI signal timing

PHYs begin the transition from the LPI receive mode when they detect the wake frame.

97.3.5.1 LPI Synchronization

To maximize power savings, maintain link integrity, and ensure interoperability, EEE-capable PHYs must synchronize refresh intervals during the LPI mode. The quiet-refresh cycle is established from the Master Partial Frame Count (PFC24) during PMA Training. At the master, partial frame zero and all multiples of 360 partial frames thereafter denote the start of the cycle.

An EEE-capable PHY in slave mode is responsible for synchronizing its partial frame count to the master's partial frame count during link up. The slave shall ensure that its partial frame count is synchronized to the master's partial frames within 1 partial frame. The start of the slave quiet-refresh cycle is delayed from the master by 13 frames (195 partial frames). This offset ensures that the master and slave wake/sense windows are offset from each other and that the refresh periods are nearly a half cycle offset.

Following the transition to PAM3, the PCS continues to count transmitted partial RS frames (tx_pfc), and uses the counter to generate refresh and wake control signals for the transmit functions.

Wake frames may be sent at the beginning of every second RS frame boundary starting at the beginning of the refresh RS frame. This sets wake_period to 30 partial RS frames. The master and slave allowable wake positions do not overlap. The wake frame may start in the same RS frame as a planned refresh and obviate this refresh.

The master and slave shall derive the refresh_active and wake_start signals from the transmitted partial RS frames (tx_pfc) as shown in Table 97-3 and Table 97-4.

Table 97–3—Synchronization logic derived from slave signal partial RS frame count

Slave-side Variable	u = tx_pfc
tx_refresh_active=true	lpi_offset – lpi_refresh_time ≤ mod(u, lpi_qr_time) < lpi_offset
tx_wake_start=true	mod(u, wake_period) = 0

Table 97–4—Synchronization logic derived from master signal partial RS frame count

Master-side variable	v = tx_pfc
tx_refresh_active=true	mod(v, lpi_qr_time) ≥ lpi_quiet_time
tx_wake_start=true	mod(v, wake_period) = wake_period/2

97.3.5.2 Quiet period signaling

During the quiet period the transmitter shall put zeros on to the MDI. During the quiet period the transmitter and may be turned off to save power.

97.3.5.3 Refresh period signaling

During the LPI mode 1000BASE-T1 PHYs use staggered, out-of-phase refresh signaling to maximize power savings. PAM3 refresh symbols are generated from the output of the data mode PCS side-stream scrambler polynomials described in 97.3.2.2.13 with PCS transmit data masked to zero. The scramblers run continuously regardless of the transmit mode. The refresh occupies the last 6 partial RS frames of where the RS frame would occur if it were transmitted.

The OAM symbol and its associated parity symbols are XOR'ed with the scrambler stream at the same relative position to the RS boundaries as they occupy during normal power mode. The parity is generated using Equation (97–2) with D_{405} ... $D_1 = 0$ and D_0 = OAM.

97.3.6 Detailed functions and state diagrams

97.3.6.1 State diagram conventions

The body of this subclause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 21.5. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

97.3.6.2 State diagram parameters

97.3.6.2.1 Constants

EBLOCK_R<99:0>
TYPE: bit vector
100-bit vector to be sent to the GMII containing symbol errors in all 10 character locations.

IBLOCK_R<99:0>
TYPE: bit vector
100-bit vector to be sent to the GMII containing idles in all 10 character locations.

IBLOCK_T<99:0>
TYPE: bit vector
100-bit vector to be sent to the encoder containing idles in all 10 character locations.

LPBLOCK_R<99:0>
TYPE: bit vector
100-bit vector to be sent to the GMII containing LP_IDLEs in all 10 character locations.

LPBLOCK_T<99:0>
TYPE: bit vector
100-bit vector to be sent to the encoder containing LP_IDLEs in all 10 character locations.

RFER_CNT_LIMIT
TYPE: TBD
Number of Reed Solomon frames with uncorrectable errors.

RFRX_CNT_LIMIT
TYPE: TBD
Number of Reed Solomon frames received over bit error rate interval.

97.3.6.2.2 Variables

RFER_test_lf
Boolean variable that is set true when a new RS frame is available for testing and false when RFER_TEST_LF state is entered. A new RS frame is available for testing when the Block Sync process has accumulated enough symbols from the PMA to evaluate the next RS frame.

block_lock
Boolean variable that is set true when receiver acquires block delineation.

hi_rfer
Boolean variable which is asserted true when the rfer_cnt exceeds RFER_CNT_LIMIT indicating a bit error ratio > 4×10^{-4}.

pcs_reset
Boolean variable that controls the resetting of the PCS. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

rx_coded<81:0>
Vector containing the input to the 80B/81B decoder including a block valid flag. The format for

rx_coded<80:0> is shown in Figure 97–6. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<80>. rx_coded<81> (not shown in the figure) is set to 1 if all parity checks of the Reed Solomon frame are satisfied, otherwise it is set to 0.

rf_valid

Boolean indication that is set true if received Reed Solomon frame is valid. The frame is valid if all parity checks of the coded bits are satisfied.

rx_lpi_active

This variable is set TRUE upon detection of LP_IDLE. Set FALSE upon wake_detection.

rx_raw<99:0>

Vector containing 10 successive GMII output transfers. Each transfer is numbered from 0 to 9 with the first transfer numbered as the 0th transfer. The nth GMII transfer is labeled as RX_DV[n], RX_ER[n], RXD[n][7:0].
For n = 0 to 9, rx_raw<8n> = RX_DV[n], rx_raw<8n+1> = RX_ER[n], rx_raw<8n+9:8n+2> = RXD[n][7:0]

rx_wake_frame_complete

This variable is set TRUE at end of WAKE RS frame, otherwise FALSE.

tx_coded<80:0>

Vector containing the output from the 80B/81B encoder. The format for this vector is shown in Figure 97–14. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<80>.

tx_data_mode

Set true when tx_mode = SEND_N, otherwise false.

tx_lpi_active

This variable is set FALSE at next wake frame if non- LP_IDLE is detected on GMII in any block.
This variable is set TRUE on next RS frame if LP_IDLE detected on GMII in the last 80/81 block.

tx_raw<99:0>

Vector containing 10 successive GMII transfers. Each transfer is numbered from 0 to 9 with the first transfer numbered as the 0th transfer. The nth GMII transfer is labeled as TX_EN[n], TX_ER[n], TXD[n][7:0].
For n = 0 to 9, tx_raw<8n> = TX_EN[n], tx_raw<8n+1> = TX_ER[n], tx_raw<8n+9:8n+2> = TXD[n][7:0]

tx_wake_frame_complete

This variable is set TRUE at the end of the RS WAKE frame, otherwise FALSE.

lpi_tx_mode

A variable indicating the signaling to be used from the PCS to the PMA across the PMA_UNITDATA.request (tx_symb) interface.
lpi_tx_mode controls tx_symb only when tx_mode is set to SEND_N.
The variable is set to NORMAL when !tx_lpi_active, indicating that the PCS is in the normal power mode of operation.
The variable is set to REFRESH when (tx_lpi_active * tx_refresh active).
The variable is set to QUIET when (tx_lpi_active * !tx_refresh active).

97.3.6.2.3 Timers

State diagram timers follow the conventions described in 14.2.3.2.

97.3.6.2.4 Functions

DECODE(rx_coded<81:0>)

In the PCS Receive process, this function takes as its argument 82-bit rx_coded<81:0> from the Reed Solomon decoder and descrambler. If rx_coded<81> = 1 then the decoder decodes the 81B-Reed Solomon bit vector rx_coded<80:0> returning a vector rx_raw<99:0>, which is sent to the GMII. The DECODE function shall decode the block based on code specified in 97.3.2.2.2. If rx_coded<81> = 0 then the decoder returns EBLOCK_R.

ENCODE(tx_raw<99:0>)

Encodes the 100-bit vector received from the GMII, returning 81-bit vector tx_coded. The ENCODE function shall encode the block as specified in 97.3.2.2.2. The ENCODE function shall only encode LPI_IDLE while in the SEND_LPI state. Otherwise LPI_IDLE is converted to Idle in the ENCODE function.

97.3.6.2.5 Counters

rfer_cnt

Count up to a maximum of RFER_CNT_LIMIT of the number of invalid Reed Solomon frames within the current RFRX_CNT_LIMIT Reed Solomon frame period.

rfrx_cnt

Count number Reed Solomon frames received during current period.

97.3.6.3 Messages

PMA_UNITDATA.indication (rx_symb)

A signal sent by PMA Receive indicating that a PAM3 symbol is available in rx_symb.

PMA_UNITDATA.request (tx_symb)

A signal sent to PMA Transmit indicating that a PAM3 symbol is available in tx_symb.

PCS_status

Indicates whether the PCS is in a fully operational state. (See 97.3.7.1.)

RX_AGGREGATE

A signal sent to PCS Receive indicating that 9 aligned 9-bit Reed Solomon symbols are aggregated in rx_coded<80:0>.

TX_AGGREGATE

A signal sent to PCS Transmit indicating that 10 GMII transfers are aggregated in tx_raw<99:0>.

RX_FRAME

A signal sent to PCS Receive indicating that a full Reed Solomon frame has been decoded and the variable rf_valid is updated.

TX_FRAME

A signal sent to PCS Transmit indicating that a full Reed Solomon frame has been transmitted.

97.3.6.4 State diagrams

The RFER Monitor state diagram shown in Figure 97–13 monitors the received signal for high RS frame error ratio.

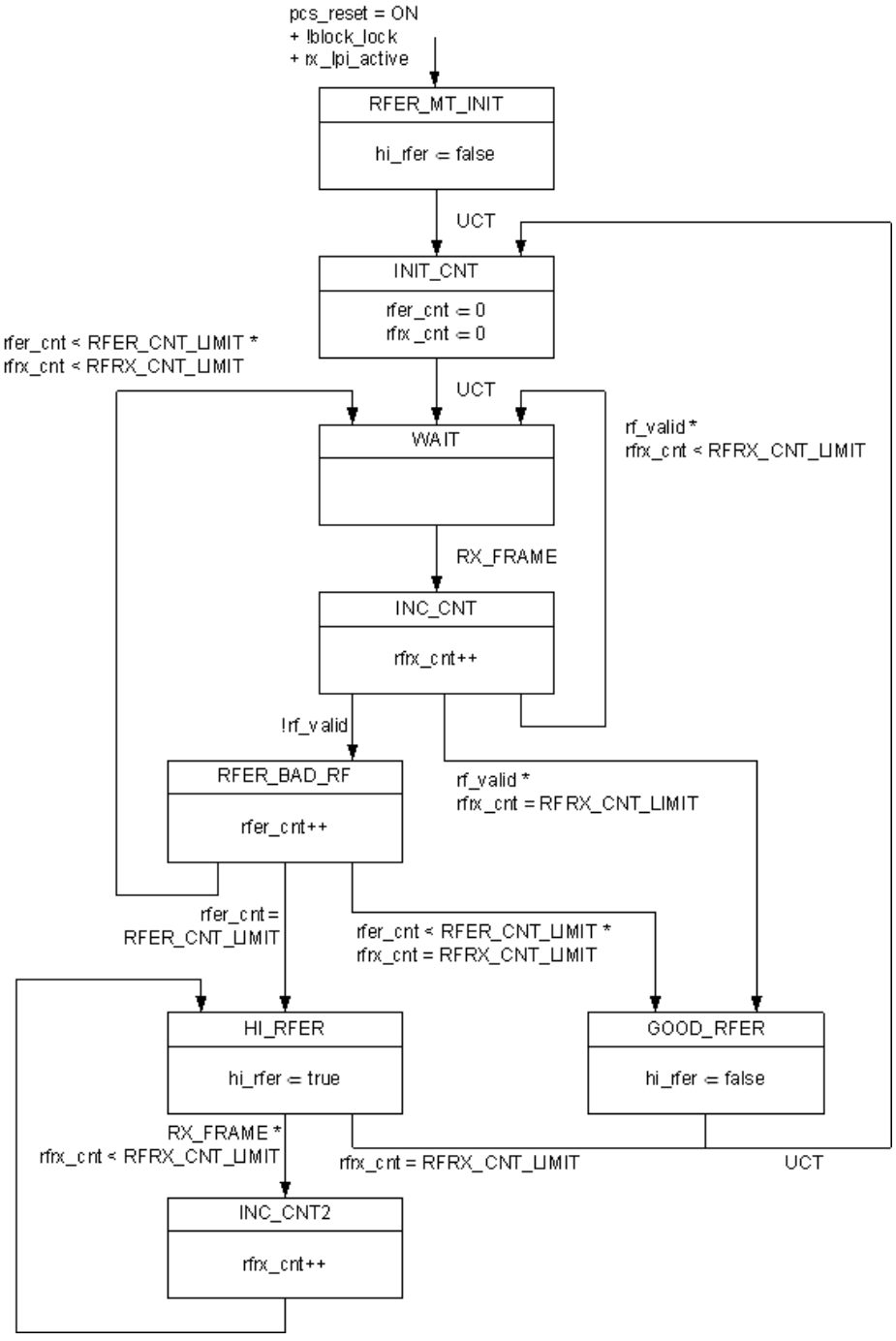


Figure 97–13—RFER monitor state diagram

The 80B/81B Transmit state diagram shown in Figure 97–14 controls the encoding of 81B transmitted blocks. It makes exactly one transition for each 81B transmit block processed. The 80B/81B Receive state diagram shown in Figure 97–15 controls the decoding of 81B received blocks. It makes exactly one transi-

tion for each receive block processed. The PCS shall perform the functions of RFER Monitor, Transmit, and Receive as specified in these state diagrams.

97.3.7 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

97.3.7.1 Status

PCS_status:
Indicates whether the PCS is in a fully operational state. It is only true if block_lock is true and hi_rfer is false. This status is reflected in MDIO register 3.32.12. A latch low view of this status is reflected in MDIO register 3.1.2 and a latch high of the inverse of this status, Receive fault, is reflected in MDIO register 3.8.10.

block_lock:
Indicates the state of the block_lock variable. This status is reflected in MDIO register 3.32.0. A latch low view of this status is reflected in MDIO register 3.33.15.

hi_rfer:
Indicates the state of the hi_rfer variable. This status is reflected in MDIO register 3.32.1. A latch high view of this status is reflected in MDIO register 3.33.14.

Rx LPI indication:
For EEE capability, this variable indicates the current state of the receive LPI function. This flag is set to TRUE (register bit set to one) when the PCS Transmit Receive state diagram (Figure 97–15) is in the RECEIVE_LPI or RECEIVE_WAKE states. This status is reflected in MDIO register 3.1.8. A latch high view of this status is reflected in MDIO register 3.1.10 (Rx LPI received).

Tx LPI indication:
For EEE capability, this variable indicates the current state of the transmit LPI function. This flag is set to TRUE (register bit set to one) when the PCS Transmit state diagram (Figure 97–14) is in the SEND_LPI or SEND_WAKE states. This status is reflected in MDIO register 3.1.9. A latch high view of this status is reflected in MDIO register 3.1.11 (Tx LPI received).

97.3.7.2 Counters

The following counters are reset to zero upon read and upon reset of the PCS. When they reach all ones, they stop counting. Their purpose is to help monitor the quality of the link.

RFER_count:
6-bit counter that counts each time RFER_BAD_RF state is entered. This counter is reflected in MDIO register bits 3.33.13:8. The counter is reset when register 3.33 is read by management. Note that this counter counts a maximum of RFER_CNT_LIMIT counts per RFRX_CNT_LIMIT period since the RFER_BAD_RF can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

97.3.7.3 Loopback

The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14 is set to a one. In this mode, the PCS shall accept data on the transmit path from the GMII and return it on the receive path to the GMII. In addition, the PCS shall transmit a continuous stream of GMII to 81B-RS encoded PAM3 symbols to the PMA sublayer, and shall ignore all data presented to it by the PMA sublayer.

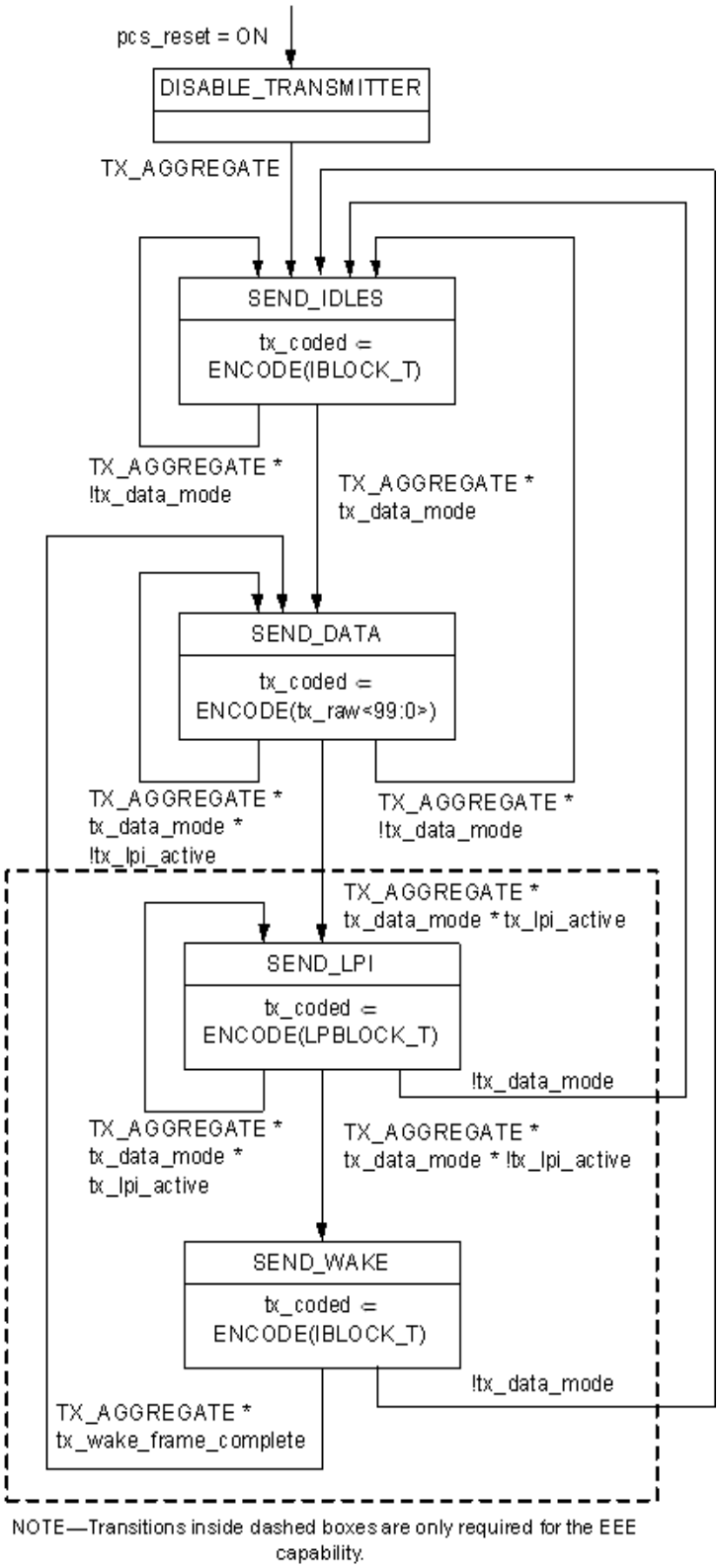


Figure 97–14—PCS Transmit state diagram

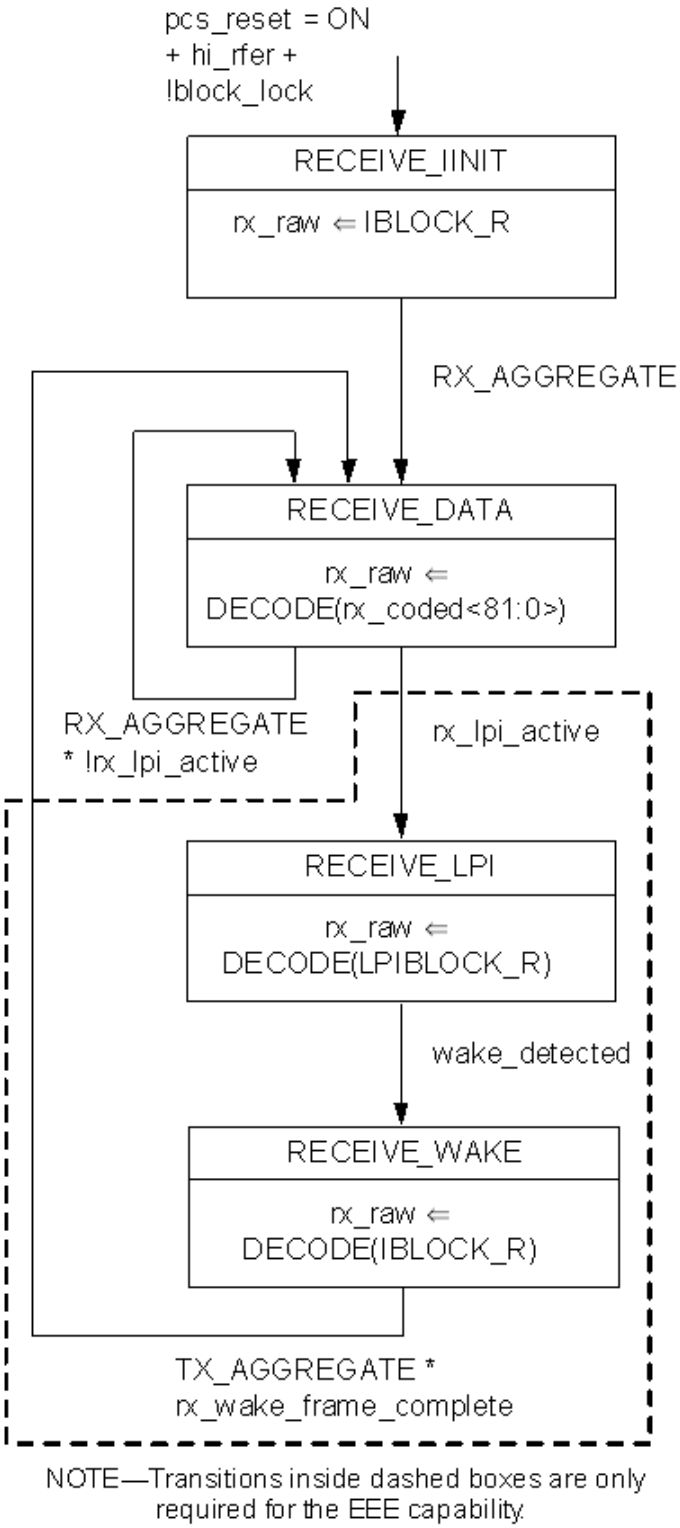


Figure 97–15—PCS Receive state diagram

97.4 Physical Medium Attachment (PMA) sublayer

97.4.1 PMA functional specifications

The PMA couples messages from a PMA service interface specified in 97.2.2 to the 1000BASE-T1 baseband medium, specified in 97.5.

The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 97.8.

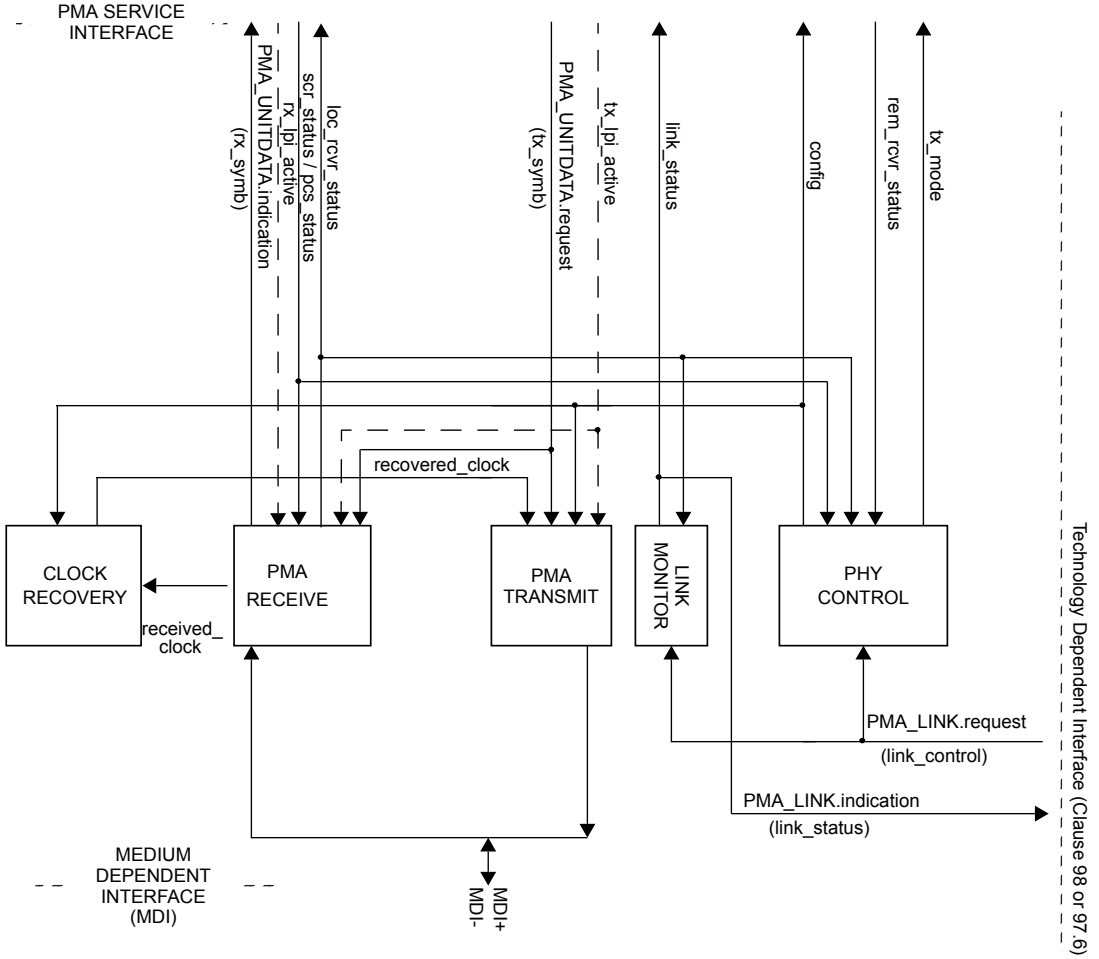


Figure 97–16—PMA reference diagram

NOTE—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

97.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure 97–16, shows how the operating functions relate to the messages of the PMA Service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 97–16.

97.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power on (see 98.5.1)
b) The receipt of a request for reset from the management entity

All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

97.4.2.2 PMA Transmit function

The PMA Transmit function comprises a transmitter to generate a 3 level modulated signals on the single twisted pair. PMA Transmit shall continuously transmit onto the MDI pulses modulated by the symbols given by tx_symb after processing with optional transmit filtering, digital to analog conversion (DAC) and subsequent analog filtering. The signals generated by PMA Transmit shall comply with the electrical specifications given in 97.5.

When the PMA_CONFIG.indication parameter config is MASTER, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 97.5.3.3. The MASTER-SLAVE relationship shall include loop timing. If the PMA_CONFIG.indication parameter config is SLAVE, the PMA Transmit function shall source TX_TCLK from the recovered clock of 97.4.2.8 while meeting the jitter requirements of 97.5.3.3.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

97.4.2.3 PMA transmit disable function

97.4.2.3.1 Global PMA transmit disable function

When the Global_PMA_transmit_disable variable is set to TRUE, this function shall turn off the transmitter so that the transmitter Average Launch Power of the Transmitter is less than –53 dBm.

97.4.2.3.2 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 97–5. Mapping of MDIO status variables to PMA status variables is shown in Table 97–6.

Table 97–5—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	Control register 1	1.0.15	PMA_reset
Global transmit disable	Transmit disable register	1.9.0	Global_PMA_transmit_disable

Table 97–6—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Fault	Status register 1	1.1.7	PMA_fault
Transmit fault	Status register 2	1.8.11	PMA_transmit_fault
Receive fault	Status register 2	1.8.10	PMA_receive_fault

97.4.2.4 PMA Receive function

The PMA Receive function comprises a receiver for PAM3 signals on the twisted pair. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI over receive pair and to present these sequences to the PCS Receive function. The PMA translates the signals received on the twisted pair into the PMA_UNITDATA.indication parameter rx_symb. The quality of these symbols shall allow RFER of less than 3.6×10^{-7} after RS decoding, over a channel meeting the requirements of 97.5.6.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization and echo cancellation. The sequence of symbols assigned to tx_symb is needed to perform echo cancellation.

The PMA Receive function uses the scr_status parameter and the state of the equalization, cancellation, and estimation functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The loc_rcvr_status variable is expected to become NOT_OK when the link partner's tx_mode changes to SEND_Z from any other values (see PHY Control state diagram in Figure 97-22). The precise algorithm for generation of loc_rcvr_status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for pair polarity swaps.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5.

97.4.2.5 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram description given in Figure 97–22.

During PMA training (TRAINING and COUNTDOWN states in Figure 97–22), PHY Control information is exchanged between link partners with a 12 octet InfoField, which is XOR'ed with the first 96 bits of the 15th partial RS FEC frame (bits 2520 to 2615) of the RS FEC frame. The InfoField is also denoted IF. The link partner is not required to decode every IF transmitted but is required to decode IFs at a rate that enables the correct actions prior to the PAM2 to PAM3 transition.

The 12 octet InfoField shall include the fields in 97.4.2.5.2 through 97.4.2.5.8, also shown in the overview Figure 97–17, and the more detailed Figure 97–18 and Figure 97–20. Each message shall be transmitted at least 256 times to ensure detection at link partner.

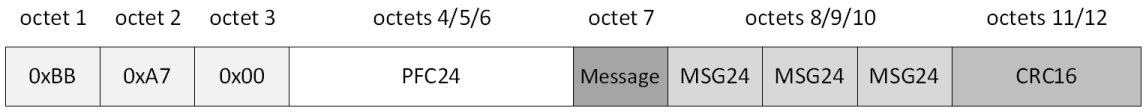


Figure 97–17—InfoField format

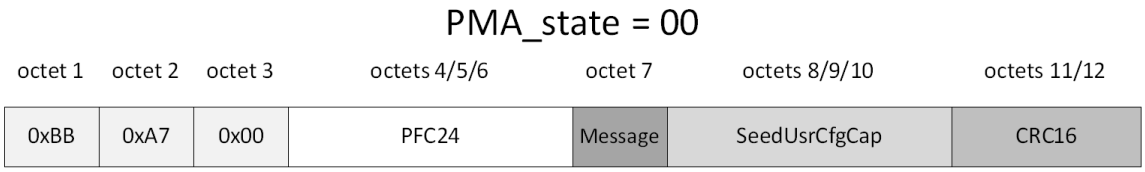


Figure 97–18—InfoField TRAINING format

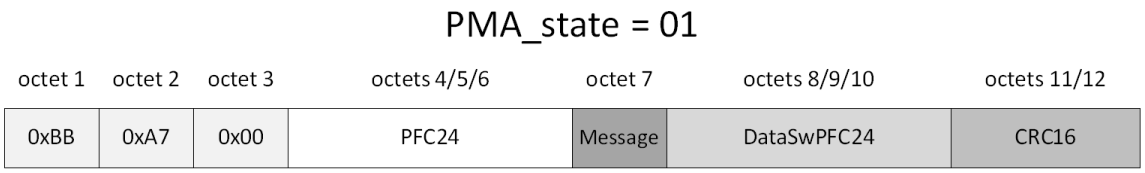


Figure 97–19—InfoField COUNTDOWN format

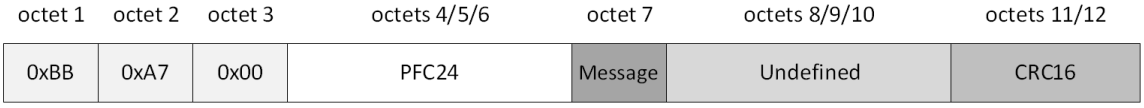


Figure 97–20—InfoField message exchange format

97.4.2.5.1 Infofield notation

For all the InfoField notation below, Reserved<bit location> represents any unused values and shall be set to zero and ignored by the link partner. The InfoField is transmitted following the notation described in 97.3.2.2.3 where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Oct1 is sent first).

97.4.2.5.2 Start of Frame Delimiter

The start of Frame Delimiter consists of 3 octets [Oct1<7:0>, Oct2<7:0>, Oct3<7:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Oct1<7:0> and so forth.

97.4.2.5.3 Partial Frame Count (PFC24)

The start of Partial Frame Count consists of 3 octets [Oct4<7:0>, Oct5<7:0>, Oct6<7:0>] and indicates the running count of partial RS FEC frames sent LSB first. There are 15 partial frames per RS FEC frame and the Infofield is embedded within the 15th partial frame. The first partial frame is zero, thus the first partial frame count field after a reset is 14.

97.4.2.5.4 Message Field

Message Field (1 octet). For the MASTER, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, en_slave_tx<4>, reserved<3:0>}. For the SLAVE, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, timing_lock_OK<4>, reserved<3:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6>=00 indicates TRAINING, and PMA_state<7:6>=01 indicates COUNTDOWN.

All possible Message Field settings are listed in Table 97–7 for the MASTER and Table 97–8 for the SLAVE. Any other value shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA frame shall be the first row of Table 97–7 for the MASTER and the first or second row of Table 97–8 for the SLAVE. Moreover, for a given Message Field setting, the following Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status=OK the InfoField variable is set to loc_rcvr_status<5>=1 and set to 0 otherwise.

Table 97–7—InfoField message field valid MASTER settings

PMA_state<7:6>	loc_rcvr_status	en_slave_tx	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

Table 97–8—InfoField message field valid SLAVE settings

PMA_state<7:6>	loc_rcvr_status	timing_lock_OK	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

97.4.2.5.5 PHY Capability Bits, User Configurable Register, and Data Mode Scrambler Seed

When PMA_state<7:6>=00, [0ct8<7:0>, 0ct9<7:0>, 0ct10<7:0>] contains the two PHY capability bits (Cap), the user configurable register bits, and the 15-bit data mode scrambler seed (Seed). Each octet is sent LSB first.

The format of PHY capability bits is Oct9<7>=EEEen and Oct10<0>=OAMen, indicating EEE and OAM capability enable respectively. The PHY shall indicate the support of optional capabilities by setting the corresponding capability bits to 1. Otherwise it shall set the capability bit to 0 to indicate no support for the optional capability.

The data mode scrambler seed contains bits S14 (sent first) to S0 (sent last) to indicate the initial state of data mode transmit scrambler of the local device upon reaching the data switch partial frame count. The state of the scrambler in Figure 97–10 shall be S14:S0 at the first bit of the first RS FEC frame when the partial frame counter equals to the DataSwPFC24 value, see 97.4.2.5.6. The format of Seed is Oct8<7:0> = S<7:14> and Oct9<6:0> = S<0:6>. Seed S<14:0> shall not be all zeros.

The remaining 7-bit Oct10<7:1> shall be user configurable register. See 97.4.2.5.10 for details.

97.4.2.5.6 Data Switch Partial Frame Count

When PMA_state<7:6>=01, [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the data switch partial frame count (DataSwPFC24) sent LSB first. DataSwPFC24 indicates the partial frame count when the transmitter switches from PAM2 to PAM3 which occurs at the start of a RS FEC block. The last value of PFC24 prior to the transition is DataSwPFC24 - 1.

97.4.2.5.7 Reserved Fields

When PMA_state<7:6> is greater than 01, [Oct8<1:0>, Oct9<1:0>, Oct10<7:0>] contains a reserved field. All InfoField fields denoted Reserved are reserved for future use.

97.4.2.5.8 CRC16

CRC16 (2 octets) shall implement the CRC16 polynomial $(x+1)(x^{15}+x+1)$ of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 97–21. In Figure 97–21 the 16 delay elements S0,..., S15, shall be initialized to zero. Afterwards Oct4 through Oct10 are used to compute the CRC16 with the switch connected, which is setting CRCgen in Figure 97–21. After all the 7 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

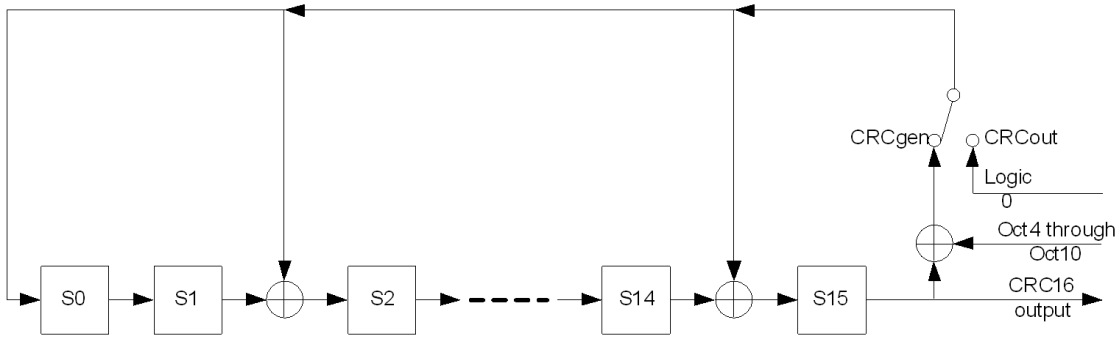


Figure 97–21—CRC16

97.4.2.5.9 Startup sequence

The startup sequence shall comply with the state diagram description given in Figure 97–22. If mr_autoneg_en = FALSE, PMA_CONFIG is pre-determined to be Master or Slave via management control during initialization or via default hardware set-up.

The Auto-Negotiation function is optional for 1000BASE-T1 PHYs. If the Auto-Negotiation function is used, during the Auto-Negotiation process PHY Control is in the DISABLE_TRANSMITTER state and the transmitter is disabled. If the Auto-Negotiation function is not used, PHY Control is in the DISABLE_TRANSMITTER state and the transmitter is controlled by the PHY Link Synchronization state machine.

When the Auto-Negotiation process asserts link_control=ENABLE or when the PHY Link Synchronization process asserts link_control=ENABLE, PHY Control enters the INIT_MAXWAIT_TIMER state. Upon entering the INIT_MAXWAIT_TIMER state, the maxwait_timer is started.

PHY Control then transition to the SILENT state. Upon entering this state the minwait_timer is started and the PHY transmits zeros (tx_mode=SEND_Z).

In MASTER mode PHY Control immediately transitions to the TRAINING state.

Upon entering the TRAINING state, the minwait_timer is started and the PHY Control forces transmission into the training mode by asserting tx_mode=SEND_T, which includes the transmission of InfoFields. The PHY Control also sets PMA_state = 00 and sends the PHY capability bits, the user configurable register bits, and the Seed value used by the local device for data mode scrambler initialization, see 97.4.2.5.5.

The optional EEE capability shall be enabled only if both PHYs set the capability bit EEEen=1. The optional OAM capability shall be enabled only if both PHYs set the capability bit OAMen=1.

Initially the MASTER is not ready for the SLAVE to respond and sets en_slave_tx=0, which is communicated to the link partner via the InfoField. After the MASTER has sufficiently converged the necessary circuitry, the MASTER must set en_slave_tx=1 to allow the SLAVE to transition to TRAINING.

In SLAVE mode PHY Control transitions to the TRAINING state only after the SLAVE PHY acquires timing, converges its equalizers, acquires its descrambler state and sets loc_SNR_margin=OK. The SLAVE shall align its transmit 81B-RS frame to within +0/-1 partial frames of the MASTER as seen at the SLAVE MDI. The SLAVE InfoField Partial Frame Count shall match the MASTER InfoField Partial Frame Count for the aligned frame.

Upon entering TRAINING state the SLAVE initially sets timing_lock_OK = 0 until it has acquired timing lock at which point the SLAVE sets timing_lock_OK = 1.

After the PHY completes successful training and establishes proper receiver operations, PCS Transmit conveys this information to the link partner via transmission of the parameter InfoField value loc_rcvr_status. The link partner's value for loc_rcvr_status is stored in the local device parameter rem_rcvr status. Upon expiration of the minwait_timer and when the condition loc_rcvr_status=OK and rem_rcvr_status=OK is satisfied, PHY control transitions to the COUNTDOWN state.

Upon entering the COUNTDOWN state, PHY Control sets PMA_state = 01, set_data_sw_pfc = 1 and DataSwPFC24 to the value of the partial frame count when the transmitter will switch from PAM2 to PAM3.

Upon reaching DataSwPFC24 partial frame count PHY Control transitions to the SEND_IDLE1 state and forces transmission into the idle mode by asserting tx_mode=SEND_I.

Once the link partner has transitioned from PAM2 to PAM3, PHY Control transitions to the SEND_IDLE2 state and starts the minwait_timer.

Upon expiration of the minwait_timer and when the condition ~~loc_rcvr_status~~loc_data_ready=OK and ~~PCS_status~~rem_data_ready=OK is satisfied, PHY control transitions to the SEND_DATA state.

Upon entering the SEND_DATA state, PHY Control stops the maxwait_timer, starts the minwait_timer and enables frame transmission to the link partner by asserting tx_mode=SEND_N.

The operation of the maxwait_timer requires that the PHY complete the startup sequence from state INIT_-MAXWAIT_TIMER to SEND_DATA in the PHY Control state diagram state diagram (Figure 97–23) in less than 97.5 ms to avoid link_status being changed to FAIL by the Link Monitor state diagram (Figure 97–23).

97.4.2.5.10 PHY Control Registers

The PHY control registers are shown in Table 97–9.

Table 97–9—PHY Control Registers

Variable	Name	Register mapping
force_config (see 97.6.1.1)	Master/Slave	1.2304.4
force_PHY_type (see 97.6.1.1)	PHY Type	1.2304.3:0
	OAM Ability	1.2305.11
	EEE Ability	1.2305.10
PMA_state<7:6> = 00, Oct10<7:1>	User Field	1.2306.10:4
PMA_state<7:6> = 00, Oct10<0>	OAM Advertisement	1.2306.1
PMA_state<7:6> = 00, Oct9<7>	EEE Advertisement	1.2306.0
LP PMA_state<7:6> = 00, Oct10<7:1>	Link Partner User Field	1.2307.10:4
LP PMA_state<7:6> = 00, Oct10<0>	Link Partner OAM Advertisement	1.2307.1
LP PMA_state<7:6> = 00, Oct9<7>	Link Partner EEE Advertisement	1.2307.0

97.4.2.6 Link Monitor function

Link Monitor determines the status of the underlying receive channel and communicates it via the variable link_status. Failure of the underlying receive channel causes the PMA to set link_status to FAIL, which in turn causes the PMA's clients to stop exchanging frames and restart the auto-negotiation (if enabled) or synchronization (if auto-negotiation is not enabled) process.

The Link Monitor function shall comply with the state diagram of Figure 97–23.

Upon power on, reset, or release from power down, the Auto-Negotiation or PHY Link Synchronization algorithms set link_control=DISABLE. If the presence of a remote station is sensed through reception of DME data, the Auto-Negotiation process exchanges Auto-Negotiation information with the remote station. During this period, link_status=FAIL is asserted. When the Auto-Negotiation function establishes the presence of a remote 1000BASE-T1 PHY or when the PHY Link Synchronization finishes the synchronization function, link_control is set to ENABLE, and the Link Monitor state machines begins monitoring the PCS and receiver lock status. As soon as reliable transmission is achieved, the variable link_status=OK is asserted, upon which further PHY operations can take place.

97.4.2.7 Refresh Monitor function

A 1000BASE-T1 PHY supporting the EEE capability shall implement the Refresh monitor function. The Refresh monitor operates when the PHY is in the LPI receive mode. ~~The receiver shall force a retrain if Refresh is unreliably detected within a moving window of 50 Q/R cycles (4.32 ms).~~If Refresh is not reliably detected within a moving window of 50 Q/R cycles (4.32 ms), the refresh monitor shall set PMA_refresh_status to FAIL, which sets link_status to FAIL. Subsequently the PHY restarts auto-negotiation (if auto-negotiation is enabled) or synchronization (if auto-negotiation is disabled). PMA_refresh_status shall be set to OK when the Link Monitor state diagram (Figure 97-23) enters the LINK_UP state.

97.4.2.8 Clock Recovery function

The Clock Recovery function shall provide a clock suitable for signal sampling so that the RS FER indicated in 97.4.2.4 is achieved. The received clock signal should be stable and ready for use when training has been completed (loc_rcvr_status=OK). The received clock signal is supplied to the PMA Transmit function by received_clock.

97.4.3 MDI

Communication through the MDI is summarized in 97.4.3.1 and 97.4.3.2.

97.4.3.1 MDI signals transmitted by the PHY

The symbols to be transmitted by the PMA are denoted by tx_symb. The modulation scheme used over each pair is PAM3. PMA Transmit generates a pulse-amplitude modulated signal on each pair in the following form:

$$s(t) = \sum_{n=0}^{\infty} a_n h_T(t - nT) \qquad (97–8)$$

In Equation (97–8), a_n is the PAM3 modulation symbol from the set {–1, 0, 1} to be transmitted at time nT, and $h_T(t)$ denotes the system symbol response at the MDI. This symbol response shall comply with the electrical specifications given in 97.5.

97.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed for each pair as pulse-amplitude modulated signals that are corrupted by noise as follows:

$$r(t) = \sum_{n=0}^{\infty} a_n h_R(t - nT) + w(t) \qquad (97–9)$$

In Equation (97–9) $h_R(t)$ denotes the symbol response of the overall channel impulse response between the transmit symbol source and the receive MDI and w(t) represents the contribution of various noise sources including uncancelled echo. The receive signal is processed within the PMA Receive function to yield the received symbols rx_symb.

97.4.4 State variables

97.4.4.1 State diagram variables

config

The PMA shall generate this variable continuously and pass it to the PCS via the PMA_CONFIG.indication primitive.

Values:

MASTER

SLAVE

en_slave_tx

The en_slave_tx variable in the InfoField received by the slave.

Values:

0: Master is not ready for the slave to transmit.

1: Master is ready for the slave to transmit.

link_control

When the Auto-Negotiation function is used, this variable is set as defined in Clause 98.

When the Auto-Negotiation function is not used, this variable is set as defined in 97.6.

link_status

The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.

Values:

OK

FAIL

loc_data_ready

This variable is set by the PMA Receive function to indicate the local PHY is ready or not ready to receive data. The value of loc_data_ready is equal to OK only if loc_rcvr_status = OK and pcs_status = OK. Otherwise its value is NOT_OK. This variable is conveyed to the link partner by the PCS as defined in Table 97-1.

Values:

OK: The local PHY is ready to receive data.

NOT_OK: The local PHY is not ready to receive data.

loc_rcvr_status

Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive link for the local PHY. This variable is transmitted in the loc_rcvr_status bit of the InfoField by the local PHY.

Values:

OK: The receive link for the local PHY is operating reliably.

NOT_OK: Operation of the receive link for the local PHY is unreliable.

loc_SNR_margin

This variable reports whether the local device has sufficient SNR margin to continue to the next state. The criterion for setting the parameter loc_SNR_margin is left to the implementer.

Values:

OK: The local device has sufficient SNR margin.

NOT_OK: The local device does not have sufficient SNR margin.

PMA_refresh_status

This variable indicates the status of the Refresh Monitor as described in 97.4.2.7.

Values:

OK: Refresh is detected reliably.

FAIL: Refresh is not detected reliably.

pma_reset

Allows reset of all PMA functions. It is set by PMA Reset.

Values:

ON
OFF

PMA_state
Variable for the value transmitted in the PMA_state<7:6> of the InfoField by the local PHY.
Values:
00: TRAINING state.
01: COUNTDOWN state.

PMA_watchdog_status
Variable indicating the status of the PAM3 monitor.
Values:
OK: The local device has received sufficient PAM3 transitions.
NOT_OK: The local device has not received sufficient PAM3 transitions.

rem_data_ready
This variable is set by the PCS Receive function to indicate whether the remote PHY is ready or not ready to receive data. This variable is received from the link partner by the PCS as defined in Table 97-1.
Values:
OK: The remote PHY is ready to receive data.
NOT_OK: The remote PHY is not ready to receive data.

rem_rcvr_status
Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not. This variable is received in the loc_rcvr_status bit in the InfoField from the remote PHY. This variable is set to NOT_OK if the PCS has not decoded a valid InfoField from the remote PHY.
Values:
OK: The receive link for the remote PHY is operating reliably.
NOT_OK: Reliable operation of the receive link for the remote PHY is not detected.

tx_mode
PCS Transmit sends code-groups according to the value assumed by this variable.
Values:
SEND_N: This value is continuously asserted when transmission of sequences of code-groups representing a GMII data stream take place.
SEND_I: This value is continuously asserted when transmission of sequences of code-groups representing a idle stream take place.
SEND_T: This value is continuously asserted when transmission of sequences of code-groups representing the training sequences of code-groups is to take place.
SEND_Z: This value is asserted when transmission of zero code-groups is to take place.

97.4.4.2 Timers

All timers operate in the manner described in 14.2.3.2.

maxwait_timer
A timer used to limit the amount of time during which a receiver dwells in the SILENT and TRAINING states. The timer shall expire 97.5 ms ± 0.5 ms after being started.
This timer is used jointly in the PHY Control and Link Monitor state diagrams. The maxwait_timer is tested by the Link Monitor to force link_status to be set to FAIL if the timer expires and loc_rcvr_status, PCS_state or PMA_watchdog_status is NOT_OK.
See Figure 97–22 and Figure 97–23.

minwait_timer

A timer used to determine the minimum amount of time the PHY Control stays in the SILENT, TRAINING, SEND IDLE1 and SEND IDLE2 states. The timer shall expire 975 us ± 50 us after being started.

97.4.5 State diagrams

97.4.5.1 PHY Control state diagram

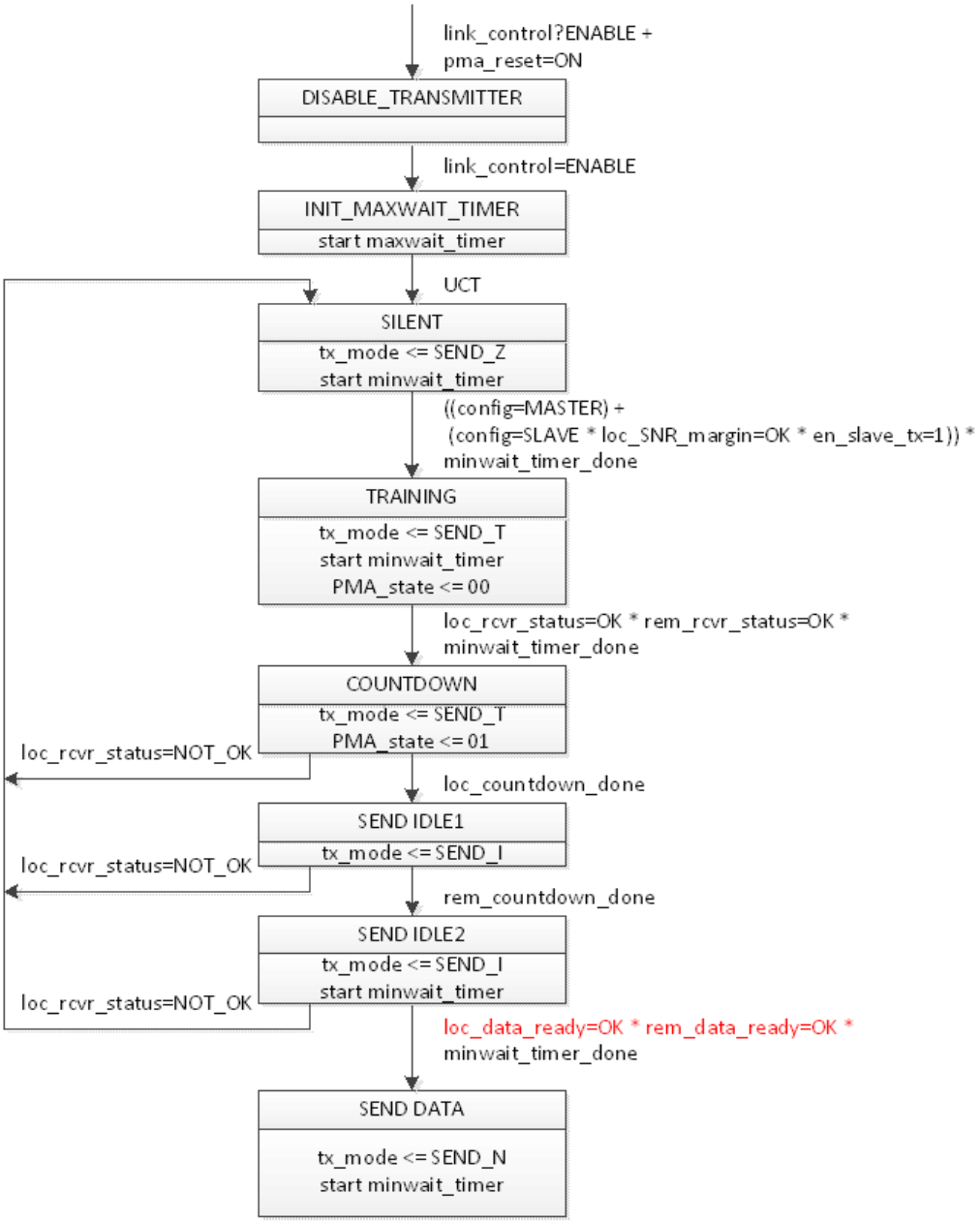
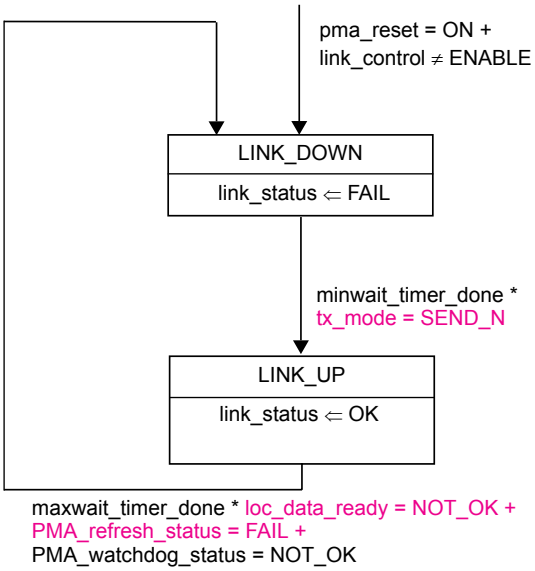


Figure 97–22—PHY Control state diagram

97.4.5.2 Link Monitor state diagram



NOTE 1—maxwait_timer is started in PHY Control state diagram (see Figure 97–22).
NOTE 2—The variables link_control and link_status are designated as link_control_1GigT1 and link_status_1GigT1, respectively, by the Auto-Negotiation Arbitration state diagram (Figure 98–14) if the optional Auto-Negotiation function is implemented.

Figure 97–23—Link Monitor state diagram

97.5 Physical Medium Dependent (PMD) sublayer

97.5.1 EMC Requirements

A system integrating the 1000BASE-T1 PHY shall comply with applicable local and national codes, or as agreed between customer and supplier, for the limitation of electromagnetic interference.

Direct Power Injection (DPI) and 150 Ohms emission tests for noise immunity and emission as per 97.5.1.1 and 97.5.2.2 shall be used to establish a baseline for PHY EMC performance. These tests provide a high degree of repeatability and a good correlation to immunity and emission measurements. Additional tests may be needed to verify EMC performance in various configurations, applications and conditions.

97.5.1.1 Immunity - DPI test

Radio frequency Common Mode (CM) noise at the PHY is the result of electromagnetic interference coupling to the cabling system. The sensitivity of the PMA receiver to radio frequency noise shall be tested according to DPI method of IEC 62132-4 with the test circuit and limits agreed between customer and supplier.

97.5.1.2 Emission - 150 Ohm conducted emission test

Radio frequency emission may result from conducted CM signal at MDI. The conducted CM emission of the PMA transmitter to its electrical environment shall be tested according to the 150 Ohms direct coupling method of IEC 61967-4 with the test circuit and limits agreed between customer and supplier.