Sine Wave Interference Tolerance of RTPGE vs. TX launch Voltage

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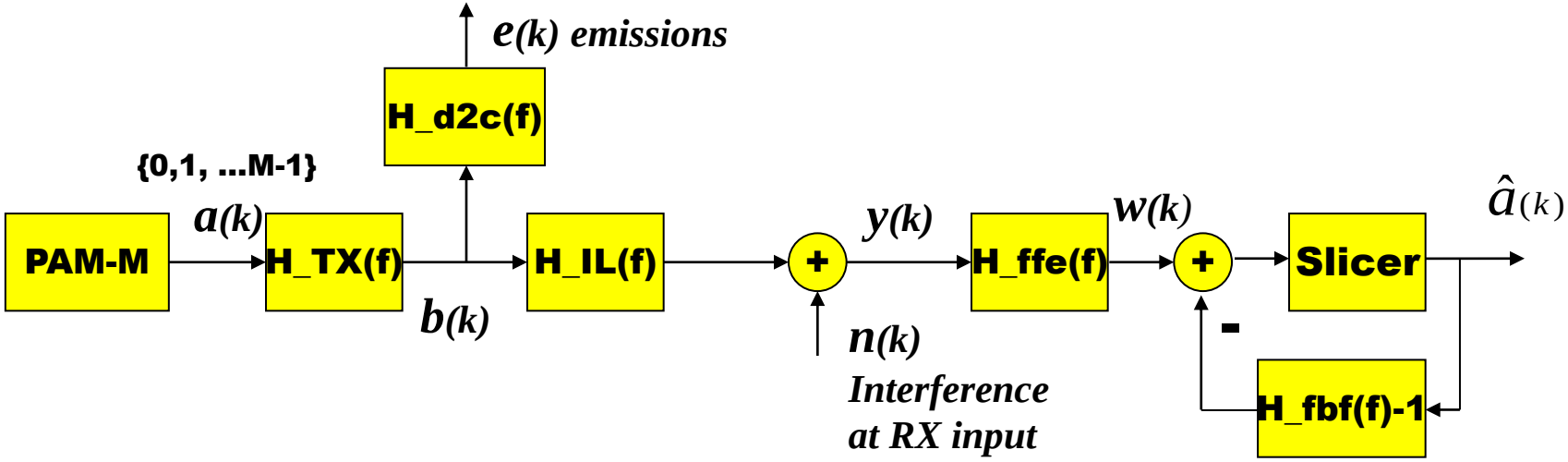
Overview

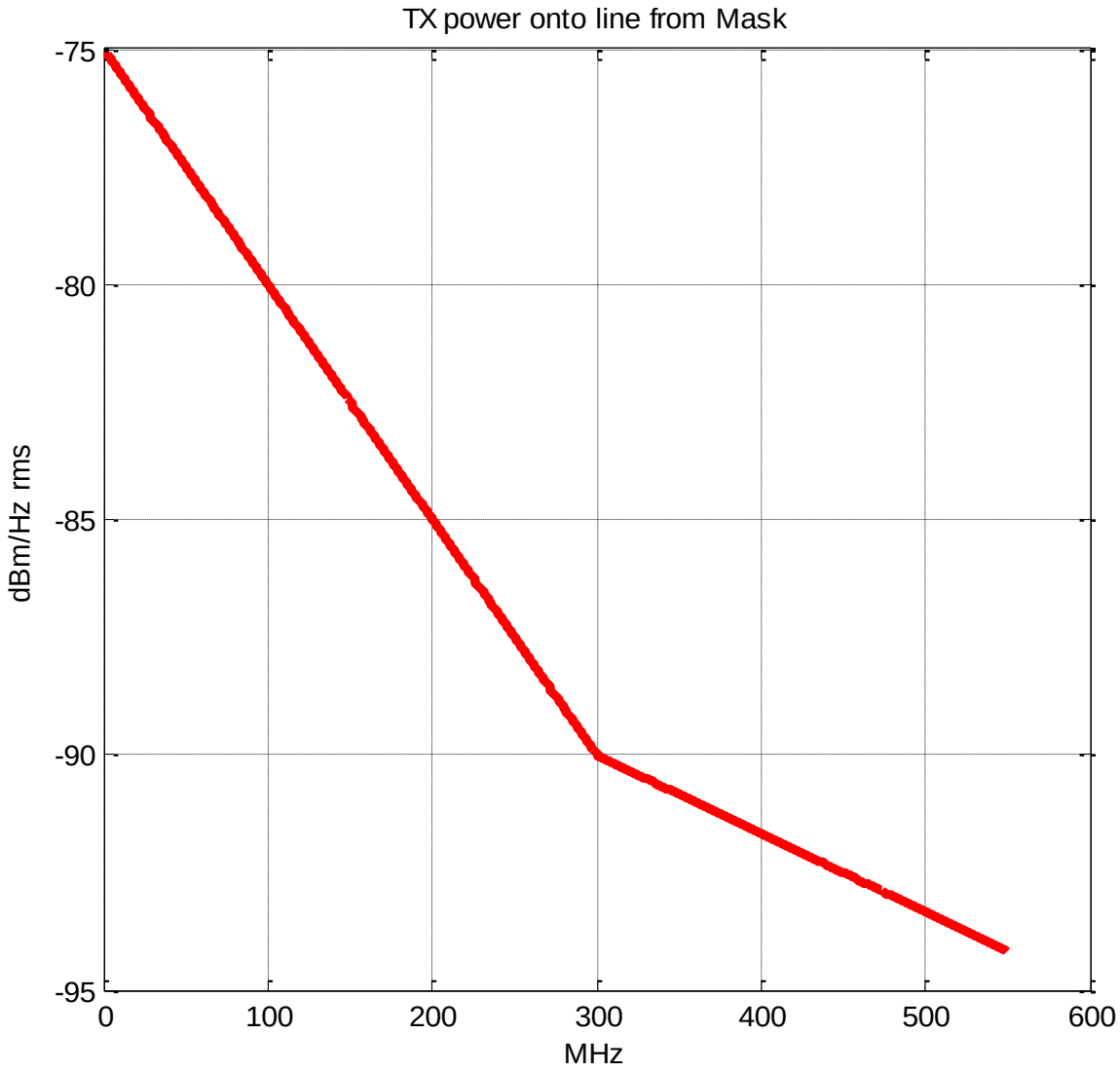
- Evaluate the tolerance to sine wave interference at the RX input
- Assume PAM-2 modulation
- Assume 10% overhead for coding (transcoding and FEC)
- Use the latest proposed TX PSD mask
- Use the latest four connector cable IL limit line model
- Assume all filters and DFE RX with unlimited taps
- Consider using lower TX launch Voltage and calculate the reduction in sine wave tolerance
- Apply a simple RX power model to create ‘power cost’ vs. ‘sine wave tolerance’ tradeoff
- Recommended target tolerance

EMC model for RTPGE w/ PAM & DFE



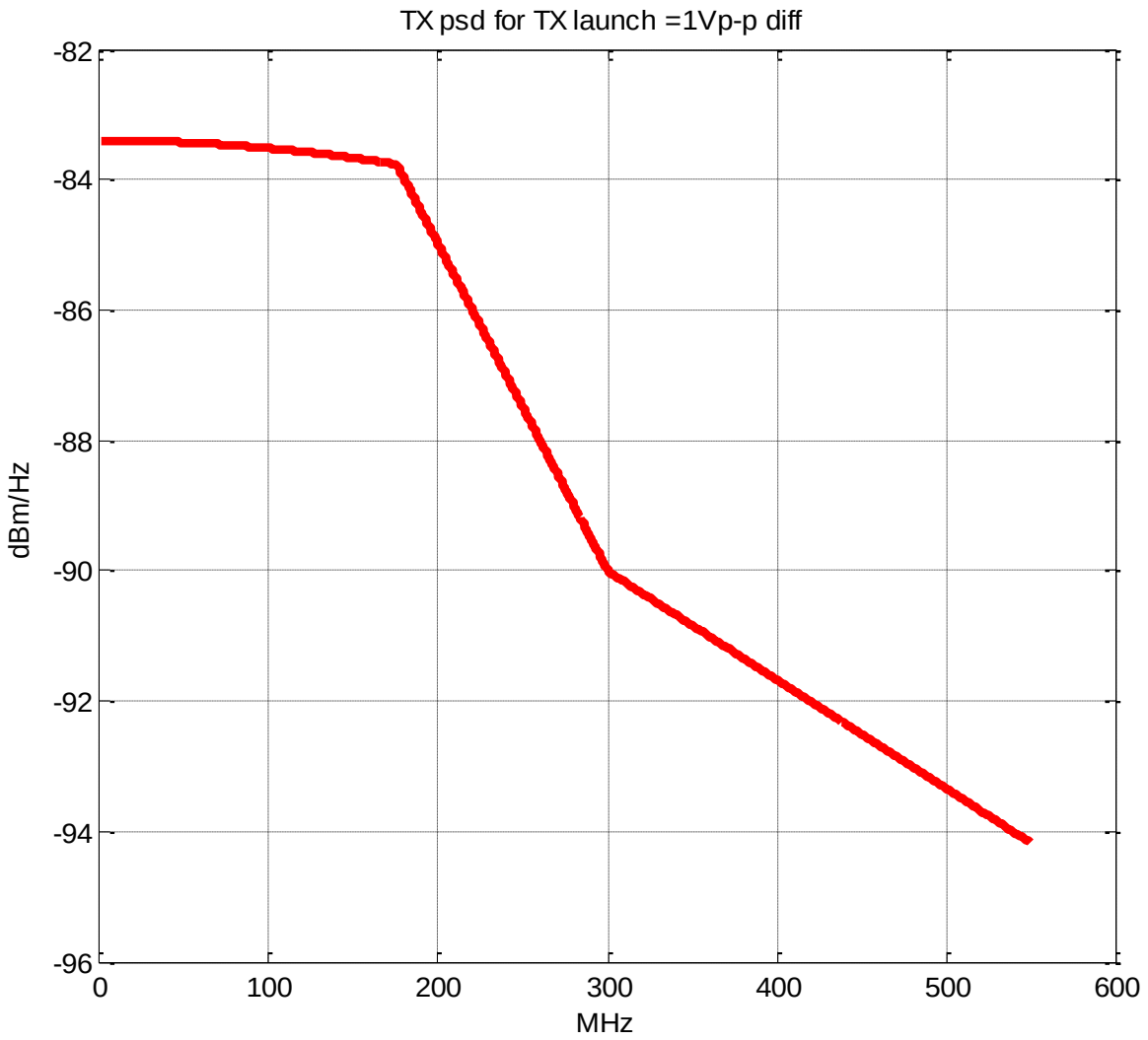
- The transmitter must be limited by LPF H_TX(f) such that the emissions *e(k)* meet the criteria set by the industry and regulation. In other words, the signal at *b(k)* must meet the TX PSD mask
- Further, we consider here cases where the maximum peak to peak Voltage at b(k) is limited by necessity or choice of TX design
- The transmit signal is further low passed by the Insertion Loss of the cabling and connectors, H_IL(f)
- Assuming *n(k)* is 'white' and the SNR(f) is nowhere low, H_ffe(f) will be all-pass, creating a minimum phase signal at *w(k)*
- Solve for the minimum amplitude sine wave at *n(k)* that creates slicer errors (with no other noises or non-idealities)

Updated TX PSD Mask



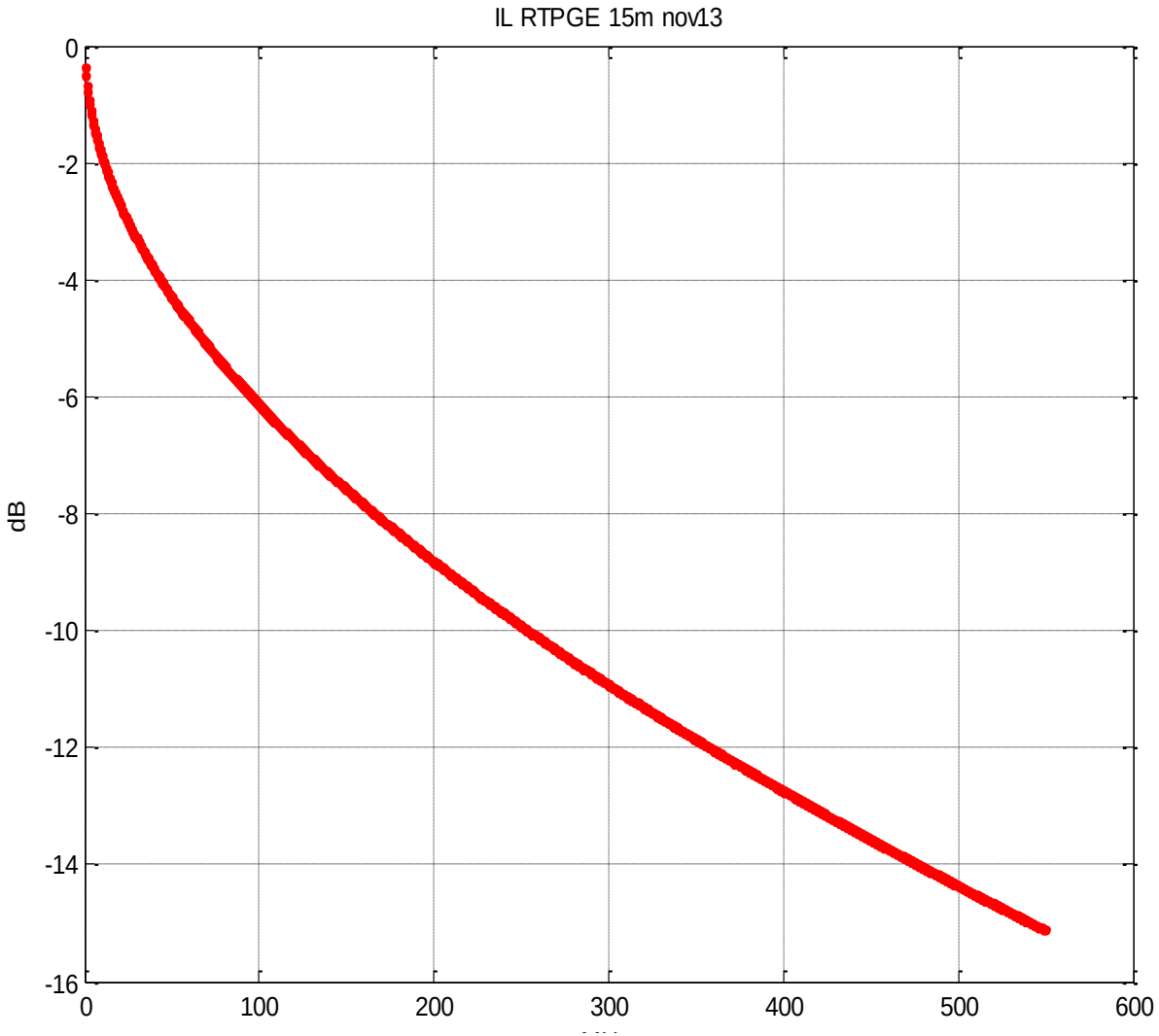
- From [Tazebay_3bp_01_062613]
- Here shown out to the Nyquist frequency for PAM-2 with 10% overhead, = 550MHz

Modified TX PSD Mask, e.g. 1Vp-p



- Modified TX PSDs meets both the original TX PSD mask AND meets a maximum peak Voltage launched onto the line,
- The example shown is for limiting the TX to 1Volt peak to peak differential launched onto the line
- The peak voltage max limits the PSD below 180 MHz
- The assumption of Baud rate signaling creates the sin(f)/f shape at low frequencies
- For this 1Vpp example, the dynamic range is reduced from 19dB to 10dB

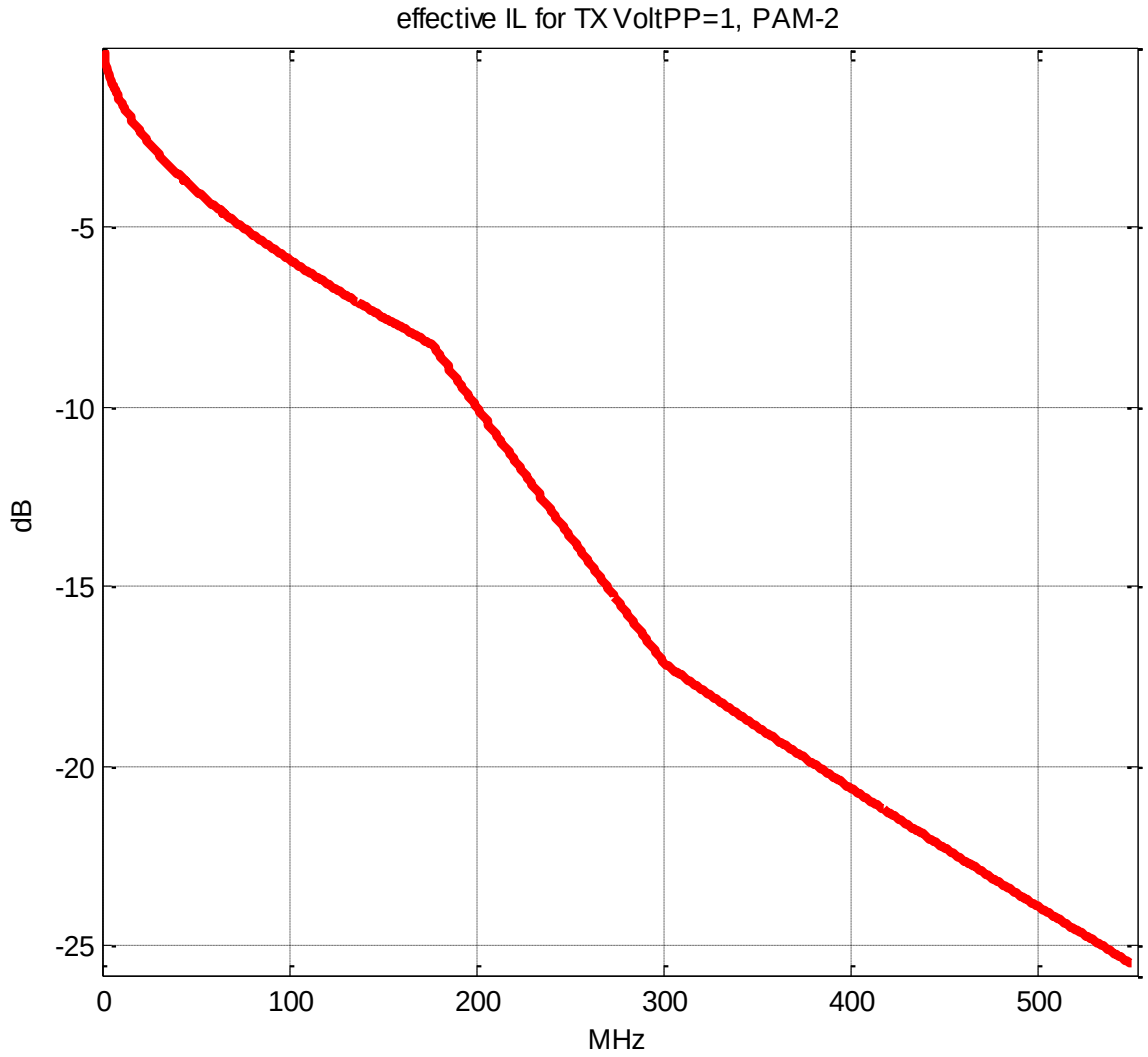
Insertion Loss



- Taken from 802.3bp Link Segment Baseline-0.2.pdf
- 15m
- 4 connector
- ~15dB IL @ Nyquist for PAM-2

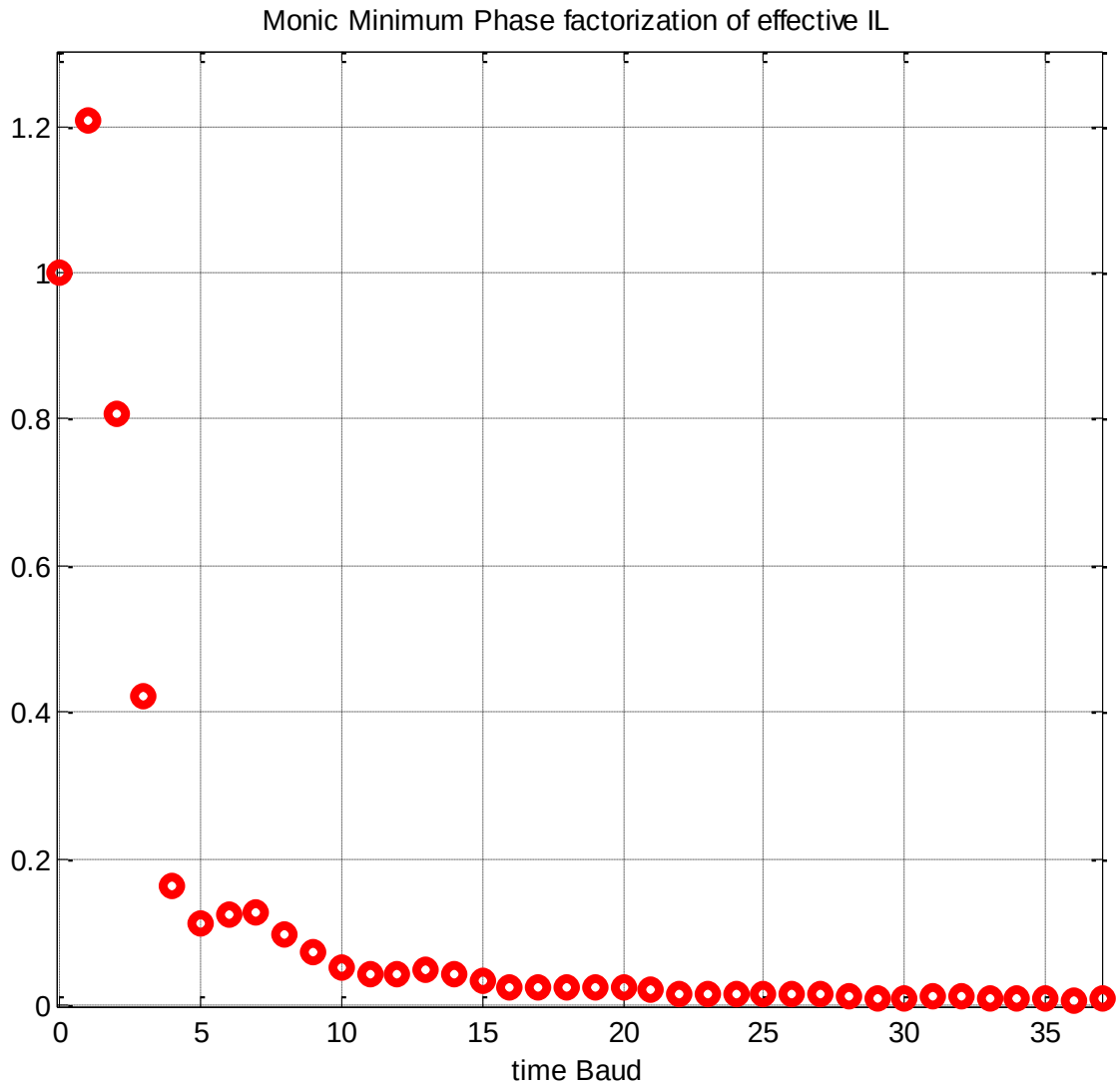
$$IL = .4927\sqrt{f} + 0.0023f + (0.0639 / \sqrt{f}) + 0.08\sqrt{f} + 0.018\sqrt{f}$$

‘Effective IL’, e.g. 1Vpp



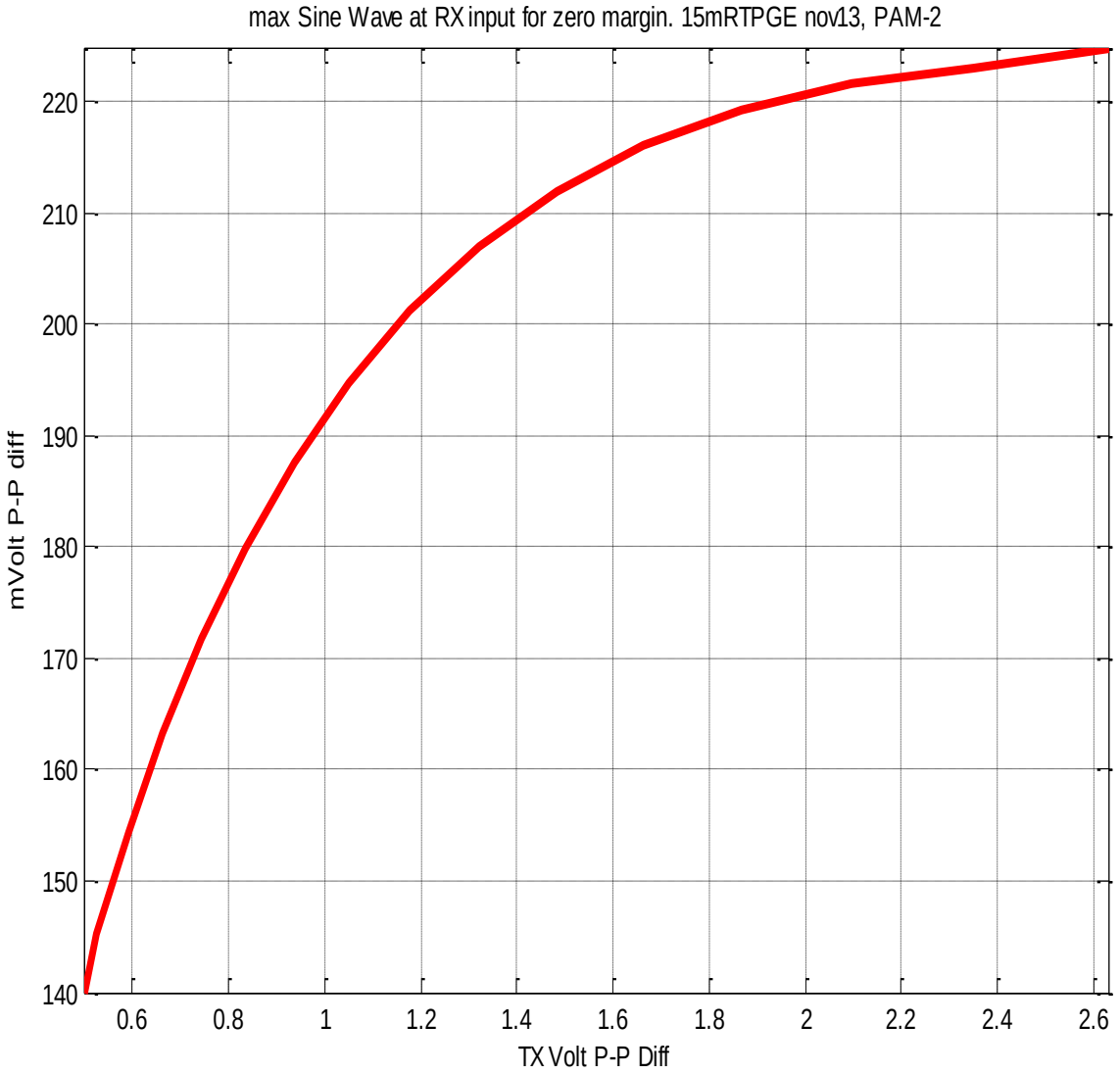
- The constraint of 1Vpp TX launch voltage reduces the dynamic range of the ‘effective IL’ seen by the RX from 34dB to 25dB
- This reduces the implementation power of the TX, and we’ll look at the reduction in RX implementation power as well

DFE Response for 1Vpp



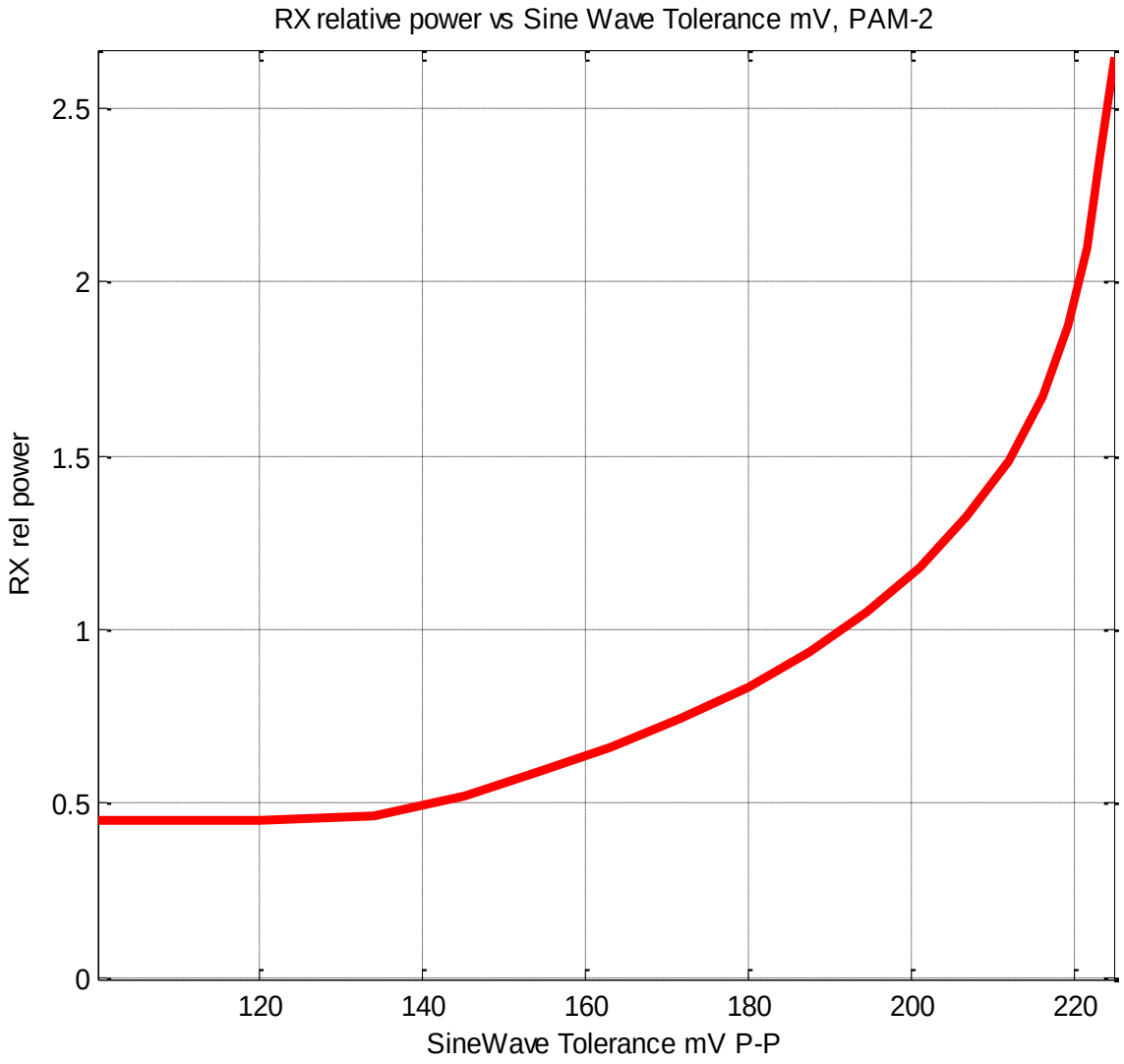
- DFE designed for white noise at the RX input with moderately high SNR(f)
- Example shown for 1Vpp max TX launch voltage
- The monic term *h(0)=1* is dropped from the actual feedback circuit
- This response is consistent with that of channels with ~25dB IL

Sine Wave Tolerance vs. TX Vpp



- The slope of the sine wave amplitude tolerated vs. the max TX Voltage Peak to Peak is low at the maximum of ~2.6 Volts
- E.g., only reduces from 225 to 192 mV going from 2.6 to 1 Volt P-P

RX relative power vs. Sine wave tolerance



- A simple model of the relative RX power cost is;
- Every 6dB of added dynamic range doubles the power
- Taken from standard ADC design Figure of Merit
- At low tolerance levels the TX PSD mask has been replaced by sinc(f), so no power reductions
- E.g., probably want to be not much more than double the ‘minimum’, so around 190mV from 1Vpp TX,

Budget for 'other Noises'

- So far we've included no other noises and /or mis-equalizations, etc.
- A practical budget must include these items
- Consider a 'base design' that just meets the BER target (w/o FEC) w/o any Sine Wave interference
- Claimed here (w/o demonstration here) that Alien cross talk is low enough to ignore in the following;
- If we lower the RX noise floor by 6dB, we will now tolerate Sine Wave interference exactly one-half of the 'bound values' previously plotted
  - So e.g., for 1Vpp, the 192mV bound is made to a real 96mVpp tolerance
  - This takes another doubling of 'relative RX power'
- E.g., another 6dB reduction in implementation noises (at another doubling of power) would achieve three-fourths of the sine wave tolerance plotted
  - So e.g., for 1Vpp, the 192mV bound is made to a real 144mVpp
- This author expects that ~100mV pp sine wave tolerance is probably near the maximum tolerance that the market will deign to 'purchase'
- Is 100mV pp enough tolerance?

Conclusions and Future Work

- The latest IL limit line and TX PSD mask limitations were used
- A range of TXs with limited max peak to peak drive Voltage was considered for possible cost reduction, and sine wave tolerance was solved for these
- There is relatively small ~15% loss in sine wave tolerance from dropping the TX drive from 2.6Vpp down to 1Vpp
- A 'relative RX power' model was introduced, and showed a 62% reduction in power from the 15% reduction in tolerance
- Practical design parameters can achieve 100mVpp sine wave tolerance
- Group needs to decide 'how much tolerance is enough', and 'how much power cost' that protection is worth.
- If going ahead with this PAM-2 technique, need a TX PSD 'window' with upper and lower limit lines

Thank you