PCS Options for the RTPGE PHY

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Overview

- Motivation
- PCS Codings in 802.3
- Recommendation

Motivation

- PHY modulation and FEC proposals will evaluate SNR and margin based on a carried bit rate
  - Carried bit rate is NOT the 1Gbps data rate
  - Ethernet control characters require additions to the information rate
  - IEEE 802.3 has used several options
    - Some relevant ones are described here
- Desire to converge PHY proposals to ease comparative analysis and progress work

PCS Codings in 802.3 (1)

- Control symbols coded as short blocks in data stream
  - Allows for FEC to protect control symbols along with data
  - General approach, used widely in 802.3
    - Original motivations for DC balance and adjacent bit error protection not relevant to RTPGE
    - Variations based on overhead tolerance and presence of FEC
  - Various code options:
    - 8B/10B: 25% overhead, short blocks, low latency, used in BASE-X interfaces
    - 64B/66B: 3.125% overhead, longer blocks, used in BASE-R interfaces, protects control characters against adjacent bit errors
    - 64B/65B: 1.015625% overhead, used in 10GBASE-T, recognizing that the PHY's FEC already protects all bits, including adjacent bit errors.

PCS Codings in 802.3 (2)

- Control symbols as unique points in the PHY constellation
  - Used in 1000BASE-T
  - Lowest overhead, and allows increased distance for control characters
  - Intimately tied into modulation and FEC design
    - Most complex for PHY analysis, most case-specific
    - Increased distance may be a liability if impulse (erasure) protection is decreased

Recommendation

- Tentatively pick 64/65B coding for PHY design
  - Assumes all PHY proposals will use some FEC to protect data and control characters
  - Minimizes overhead among choices
  - Perform PHY analysis on a carried bit rate of at least 1.015625 Gb/s
    - Additional bits may be added to ease clock generation, add overhead, etc, as specific PHY proposals may need