40GBASE-T
Channel modeling ad hoc

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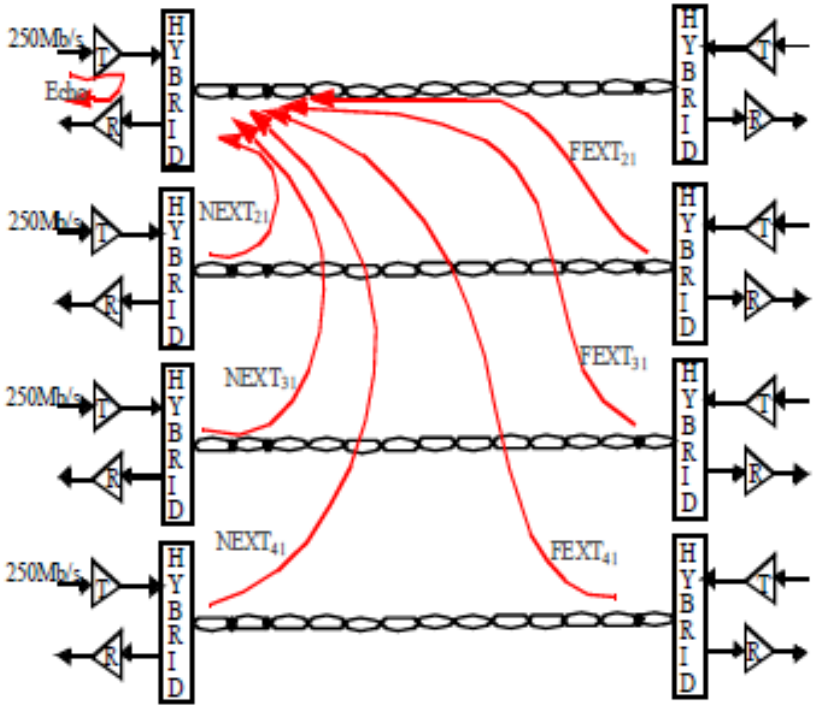
Discussion

- **Overview of 802.3 copper modeling**
- **40GBASE-T PHY-Channel**

1000BASE-T cabling channels

1000BASE-T Channel Models

- **Worst Case NEXT - 3 disturbers - Cat 5**
  - 27.1-16.8log10(f/100) dB
- **FEXT - 3 disturbers**
  - 17 - 20log10 (f/100) dB
  - 19.5 - 20log10 (f/100) dB
  - 23 - 20log10(f/100) dB
- **PSELFEXT loss>14.4-20log10(f/100) dB**
- **Return loss (2 models)**
  - 15 dB (1-20 MHz)
  - 15-10log10(f/20) (20-100 MHz)
- **Insertion Loss (cat 5)**
  - Insertion_Loss(f) < 2.1 f ^0.529 + 0.4/f (dB)



Source: http://www.ieee802.org/3/10GBT/public/jan03/index.html
10GBASE-T Physical Layer Specifications
diminico_1_0103.pdf

Matlab code 3 dB margin

3 dB Design Point -Summary Assumptions

D/ A: 17 levels at 125MHZ
Launch Level: 2V ptp
Analog Transmit Filter: Single pole RC
Analog Receive Filter: BW2@ 100MHz
A/ D: 5.5bits ideal at 125MHz
Baseline Wander Correction: Digital
FFE - #taps: 12 taps at 125MHz
DFE - #taps: 10 taps at 125MHz
NEXT Cancellers - #taps: 12 taps at 125MHz
Echo Canceller - #taps: 50 taps at 125MHz
Viterbi Decoder: 12- stage
Total worst- case latency: 31BT < 40BT
Uniform Jitter Tolerance for 0dB margin: 1.3ns ptp [> 10ns ptp Gaussian]
Worst- Case Total Noise Budget: 140mV ptp
Est. Gate Count/ Power Consumption: 130K/ 2.2W
Margin without FEXT: 3.6dB (relative external noise margin)
Margin with Worst- Case FEXT: 2.6dB (relative external noise margin)

10GBASE-T

Slide Source: Sailesh K. Rao

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10GBASE-T Physical Layer Specifications
diminico_1_0103.pdf

Matlab code 10 dB margin

10 dB Design Point -Summary Assumptions

D/A: 17 levels at 125MHZ
Launch Level: 2V ptp
Analog Transmit Filter: Single pole RC
Analog Receive Filter: BW2@ 100MHz
A/ D: 6.5bits ideal at 125MHz
Baseline Wander Correction: Digital
FFE - #taps: 16 taps at 125MHz
DFE - #taps: 12 taps at 125MHz
NEXT Cancellers - #taps: 72 taps at 125MHz
Echo Canceller - #taps: 120 taps at 125MHz
Viterbi Decoder: 12- stage
Total worst- case latency: 31BT < 40BT
Uniform Jitter Tolerance for 0dB margin: 1.5ns ptp [> 10ns ptp Gaussian]
Worst- Case Total Noise Budget: 140mV ptp
Est. Gate Count/ Power Consumption: 330K/ 4W
Margin without FEXT: 10.5dB (relative external noise margin residual noise)
Margin with Worst- Case FEXT: 7.0dB (relative external noise margin residual no

10GBASE-T

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diminico_1_0103.pdf

10GBASE-T model assumptions

Capacity and Margin vs. Cabling length

- **Model Assumptions:**
  - Cabling AdHoc 4-connector models
    - IL and ELFEXT scaled for length
  - No ANEXT mitigation assumed
    - -150 dBm/Hz background noise
    - 55 dB RL Cancellation
    - 40 dB NEXT, 25 dB FEXT cancellation
    - Flat TX spectrum across bandwidth

IEEE P802.3™
Sept 2003

Source: http://www.ieee802.org/3/10GBT/public/sep03/diminico_1_0903.pdf
10GBASE-T Objectives
diminico_1_0903.pdf

10GBASE-T supporting presentations

Capacity and Margin vs. Cabling length

- Capacity 18-20 Gbps used as metric for feasibility (roth_1_0503)
- Implementation metric:
  - PAM-10 DFE margin with example code (jones_2_0103 slide 14)
  - Detailed time-domain simulations shown for this case, including cancellation to levels shown
- Matlab code available for use with models from cabling adhoc

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Source: http://www.ieee802.org/3/10GBT/public/sep03/diminico_1_0903.pdf
10GBASE-T Objectives
diminico_1_0903.pdf

10GBASE-T power consumption and complexity

Power Consumption & Complexity

- Based on an existing detailed design, we estimate:
  - 1.5 TOPs computation (1.5X Quad 1000BASE-T)
  - 6M Gates DSP
  - PAM-10 computation
  - Cancellation per simulations
  - Analog components & A/D converters in CMOS
- TSMC's roadmap puts 90nm mature & 65nm technology as commercial in 2006
- Based on silicon in the lab today:
  - we estimate power for 10GBASE-T in 2006 to be <7W with 90nm technology

IEEE P802.3™
Sept 2003

Source: http://www.ieee802.org/3/10GBT/public/sep03/diminico_1_0903.pdf
10GBASE-T Objectives
diminico_1_0903.pdf

Channel Operating Margin – 100GBASE-CR4

•The channel operating margin (COM) for the channel between TP0 and TP5, computed using the procedure in 93A and the parameters in Table 93–9, is recommended to be greater than or equal to 3 dB.

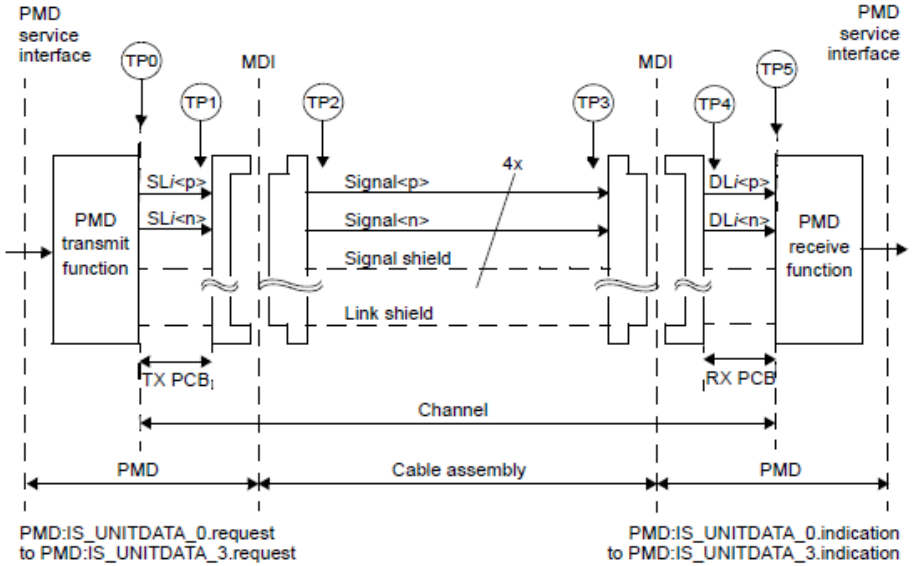


Figure 92–2—100GBASE-CR4 link (one direction is illustrated)

Test points	Description
TP0 to TP5	The 100GBASE-CR4 channel including the transmitter and receiver differential controlled impedance printed circuit board insertion loss and the cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are to be made between TP1 and TP4 as illustrated in Figure 92–2. The cable assembly test fixture of Figure 92–14 or its equivalent, is required for measuring the cable assembly specifications in 92.10 at TP1 and TP4.
TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 92.8.3 and 92.8.4. The maximum insertion loss from TP0 to TP2 or TP3 to TP5 including the test fixture is specified in 92.8.3.5.
TP2	Unless specified otherwise, all transmitter measurements defined in Table 92–5 are made at TP2 utilizing the test fixture specified in 92.11.1.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 92.8.4 are made at TP3 utilizing the test fixture specified in 92.11.1.

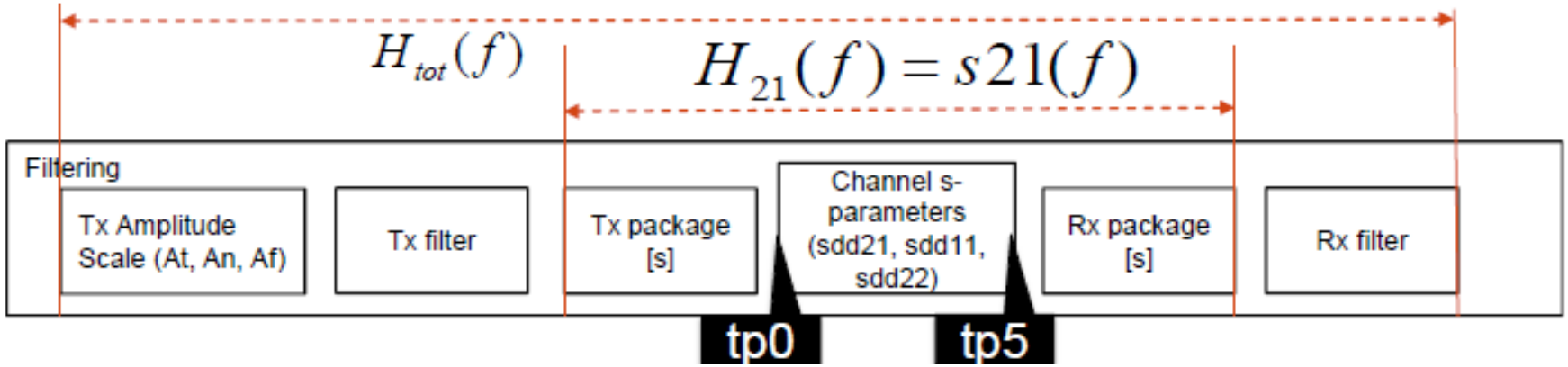
Channel Operating Margin

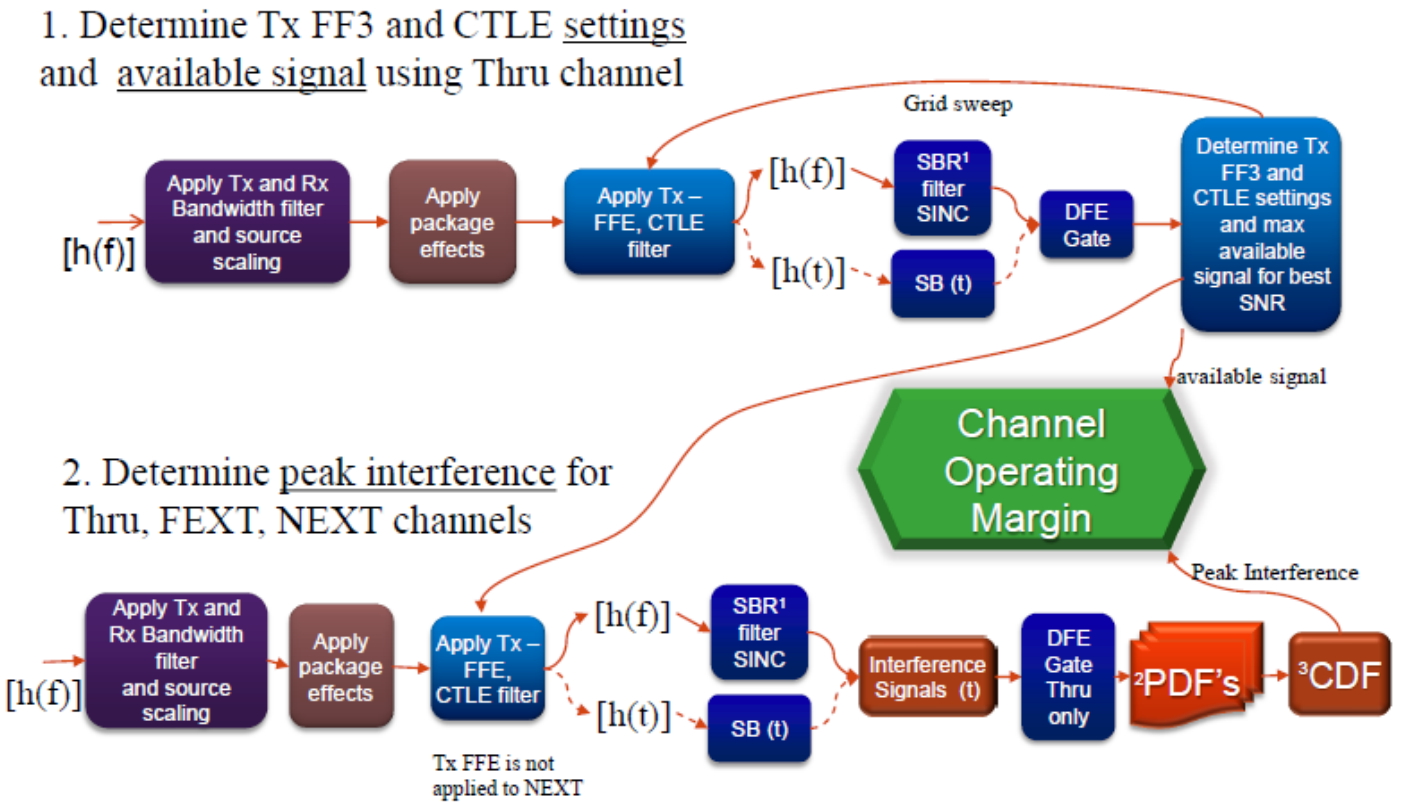
•The channel operating margin (COM) is a figure of merit for a channel utilizing reference transmitter/receiver performance characteristics. The reference transmitter/receiver block represents a minimum expected capability.

•This method is complemented by appropriate TX and RX compliance tests.

•A channel with positive COM is considered likely to operate with a minimally compliant transmitter and receiver.

Channel Operating Margin





Channel Operating Margin Parameters – WGB D2.0

Table 93–9—Channel operating margin parameters

Parameter	Symbol	Value	Units
Signaling rate	f_b	25.78125	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device package model Single-ended device capacitance Transmission line length Single-ended package capacitance	 C_d z_p C_p	 2.5×10^{-4} 12 1.8×10^{-4}	 nF mm nF
Single-ended reference resistance	R_0	50	Ω
Single-ended termination resistance	R_d	55	Ω
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_f A_n	 0.4 0.4 0.6	 V V V
Receiver 3 dB bandwidth	f_r	$0.75 \times f_b$	GHz
Transmitter equalizer, pre-cursor coefficient Minimum value Maximum value Step size	$c(-1)$	 –0.18 0 0.02	 — — —
Transmitter equalizer, post-cursor coefficient Minimum value Maximum value Step size	$c(1)$	 –0.38 0 0.02	 — — —
Continuous time filter, DC gain Minimum value Maximum value Step size	g_{DC}	 –12 0 1	 dB dB dB
Number of signal levels	L	2	—
Number of samples per unit interval	M	32	—
Decision feedback equalizer (DFE) length	N_b	14	UI
Normalized DFE coefficient magnitude limit	b_{max}	1	—
Random jitter, RMS	σ_{RJ}	0.01	UI
Dual-Dirac jitter, peak	A_{DD}	0.07	UI
Receiver additive Gaussian noise, RMS	σ_r	1	mV
Target detector error ratio	DER_0	10^{-5}	—

Cable assembly COMS

•Revisions to working group ballot D2.0

•Normative requirements for Insertion Loss Deviation, Integrated Crosstalk Noise, and fitted insertion loss coefficients replaced with a COM specification for the cable assembly.

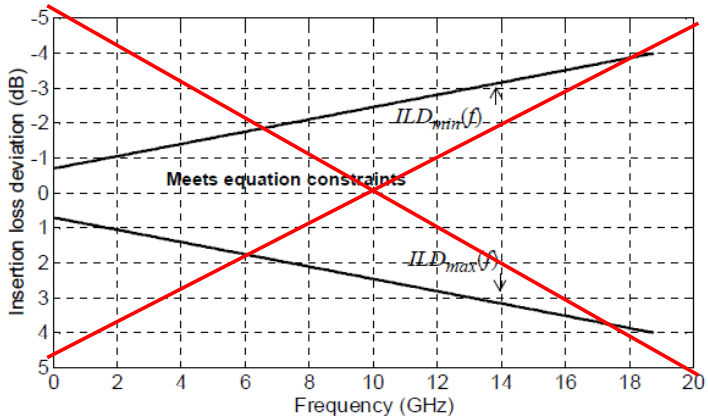


Figure 92–11—Maximum cable assembly insertion loss deviation

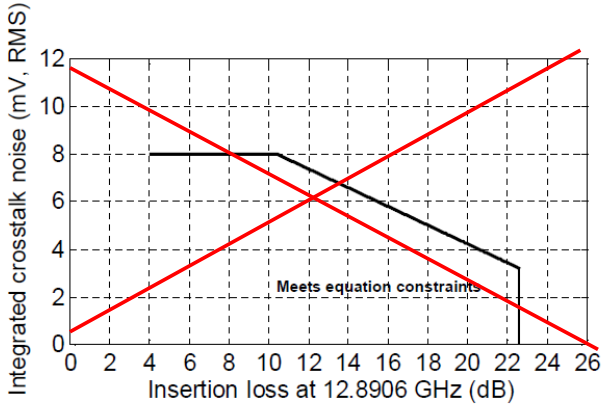


Figure 92–13—Integrated crosstalk noise limits

Table 92–12—Maximum and minimum cable assembly insertion loss characteristics

Description	Value	Unit
Maximum insertion loss at 12.8906 GHz	22.48[a]	dB
~~Maximum fitted insertion loss coefficient a_1~~	~~4.28~~	~~dB/√GHz~~
~~Maximum fitted insertion loss coefficient a_2~~	~~0.7~~	~~dB/GHz~~
~~Maximum fitted insertion loss coefficient a_4~~	~~0.02~~	~~dB/GHz^2~~
Minimum insertion loss at 12.8906 GHz	8	dB

[a]The limit on the maximum insertion loss at 12.8906 GHz precludes the coefficients a_1, a_2, and a_4 from simultaneous maximum values.

Channel Operating Margin – cable assembly

•92.10.8 Channel operating margin
The performance of the cable assembly is evaluated using the channel operating margin (COM) procedure in 93A and the parameters in Table 93-9 plus the additional PCB loss parameters. The cable assembly (COM) is derived from the cable assembly scattering parameter measurements of the insertion loss of a receive lane and the four individual pair to-pair differential NEXT losses and three individual pair-to-pair differential FEXT losses that can couple into a receive lane.

•The channel insertion loss between TP0 and TP5 for the cable assembly (COM) consists of the cable assembly insertion loss measurement and an insertion loss allocation of 6.26 dB for TPO to MDI and 6.26 dB for TP5 to MDI to account for the transmitter and receiver PCB insertion losses and the additional MDI insertion loss.

•The cable assembly (COM) shall be greater than or equal to 4 dB.

Host PCB loss allocation

PCB losses

Attenuation* (dB/in) at:	1 GHz	6.5 GHz	7 GHz	12.89 GHz	14 GHz
Meg6_LowSR – Wide	0.0951	0.4159	0.4433	0.7562	0.8127
Meg6_LowSR – Narrow	0.1466	0.5849	0.6205	1.0152	1.0847
Meg6_HighSR – Wide	0.1175	0.5960	0.6367	1.0891	1.1688
Meg6_HighSR – Narrow	0.1856	0.8971	0.9557	1.5924	1.7020
ImpFR4_LowSR – Wide	0.1202	0.6096	0.6541	1.1772	1.2734
ImpFR4_LowSR – Narrow	0.1717	0.7794	0.8323	1.4410	1.5512
ImpFR4_HighSR – Wide	0.1427	0.7904	0.8484	1.5158	1.6367
ImpFR4_HighSR – Narrow	0.2106	1.0930	1.1692	2.0283	2.1813

PROPOSED PARAMETERS; GRAPHS ON PREVIOUS SLIDE

*using Algebraic Model v2.02a – see backup slides for values entered in Model

Proposal for Defining Material Loss
26-Jan 12

Elizabeth Kochuparambil
Joel Goergen

Cisco

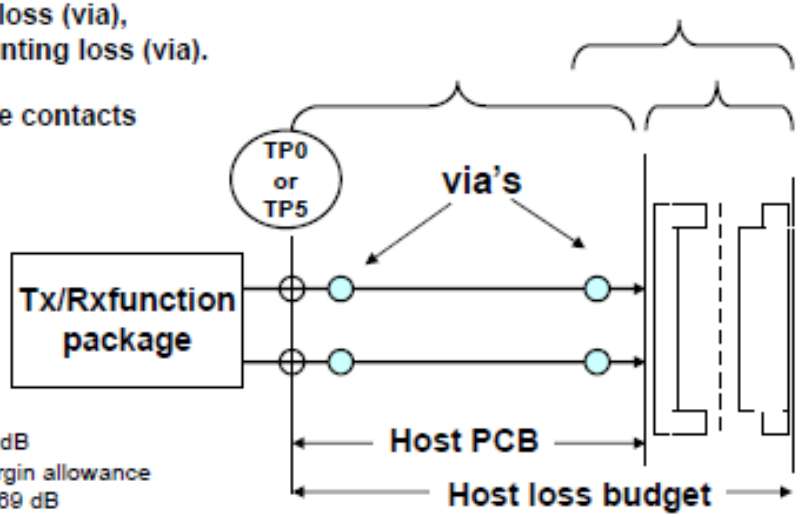
http://www.ieee802.org/3/bj/public/jan12/kochuparambil_01a_0112.pdf

Source: http://www.ieee802.org/3/bj/public/mar12/diminico_01a_0312.pdf
IEEE 802.3bj: 100GBASE-CR4 Test Points and Parameters
diminico_1a_0312.pdf

Host loss budgets

Host loss budget IL proposal

Host loss budget includes
- Chip/ball mounting loss (via),
- MDI receptacle mounting loss (via).
- MDI receptacle
- Plug connector edge contacts



Note: recommend 0.62 dB
host connector loss margin allowance
1.07 dB + 0.62 dB = 1.69 dB

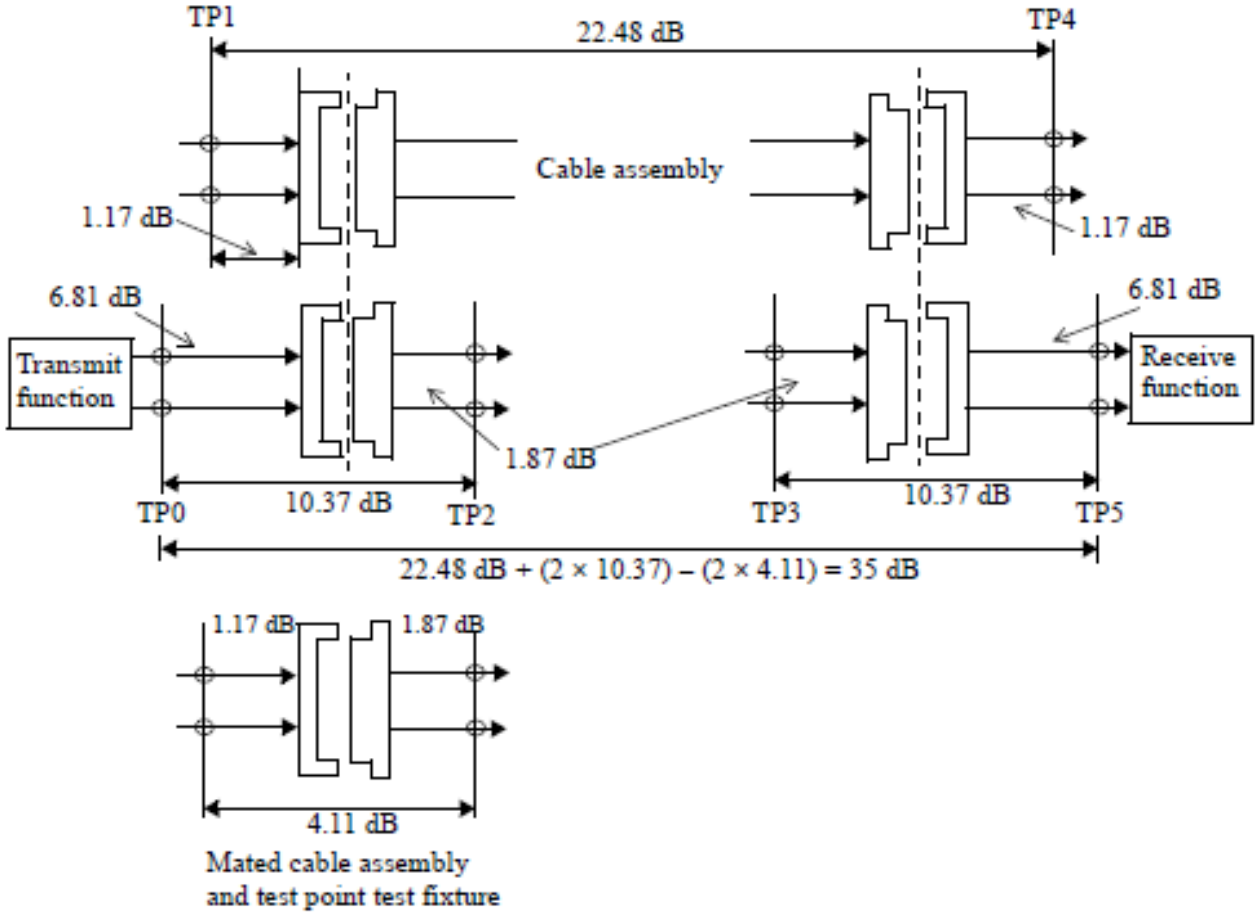
Reference	Host PCB	Mated Connector	Host loss budget - 12.89 GHz	Host loss budget – 14 GHz
CEI-28G-VSR Nov11	7.3 dB 14 GHz (PCB+2 via's) (2 via's[0.5 dB] + host trace[6.8 dB]) (4" N4000-13 or slightly worse material (up to 1.7dB/in) at 14GHz	1.2 dB @ 14 GHz	8.5 dB	8.50 dB
Diminico_01_0312.pdf	6.36 dB @ 12.89 GHz (1.59 dB/in) 6.8 dB @ 14.00 GHz (1.7 dB/in) (2 via's[0.45 dB] @ 12.89 GHz (2 via's[0.50 dB] @ 14.00 GHz	1.07 dB @ 12.89 GHz 1.20 dB @ 14.00 GHz 0.62 dB @ 12.89 GHz*	8.5 dB	8.50 dB

4

802.3bj Cu specifications

Source: http://www.ieee802.org/3/bj/public/mar12/diminico_01a_0312.pdf
IEEE 802.3bj: 100GBASE-CR4 Test Points and Parameters
diminico_1a_0312.pdf

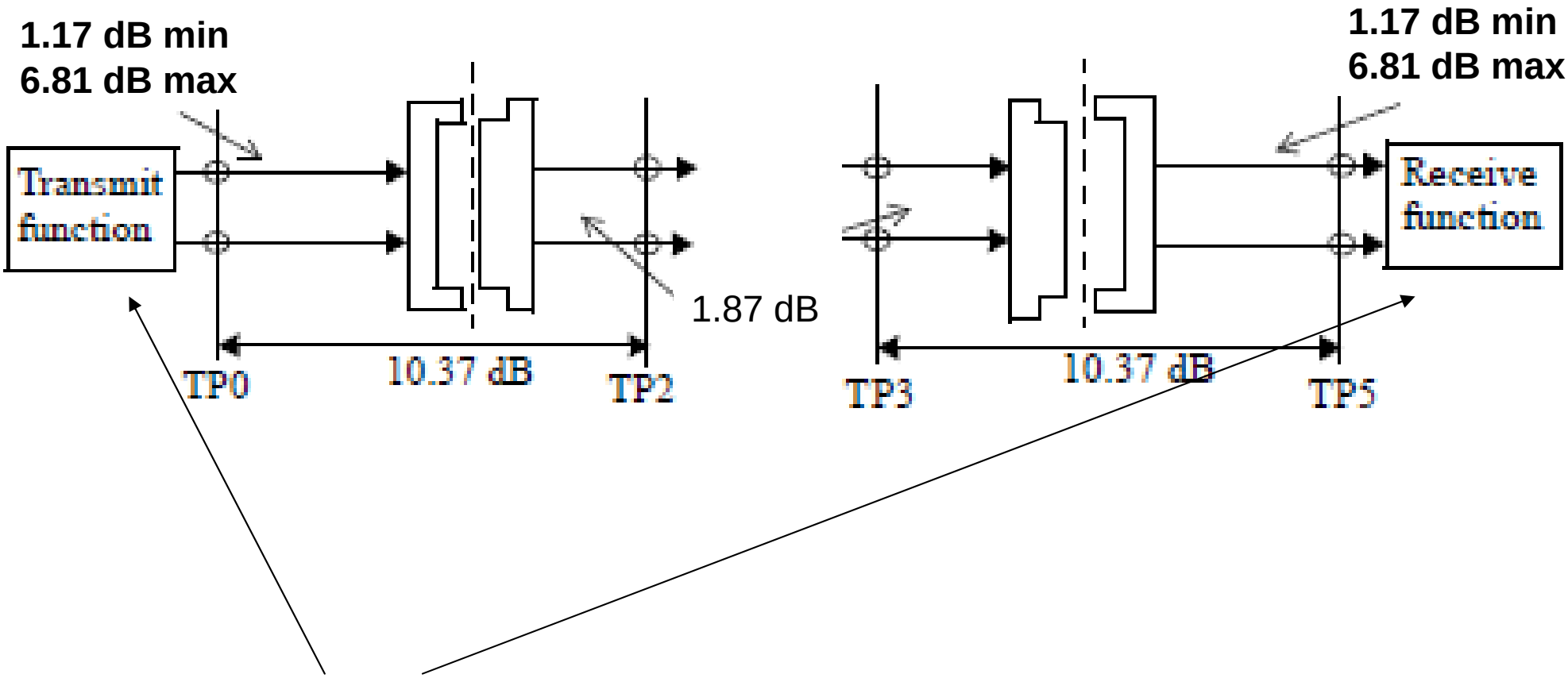
802.3bj - Channel loss budget



NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

Figure 92A–2—35 dB channel insertion loss budget at 12.8906 GHz

Tx and Rx function models



- Tx and Rx function models validated at TP2 and TP3

Transmitter at TP2 characteristics

Table 92–6—Transmitter characteristics at TP2 summary

Parameter	Subclause reference	Value	Units
Differential peak-to-peak output voltage (max) with Tx disabled	92.8.3.1	35	mV
DC common-mode voltage (max)	92.8.3.1	1.9	V
AC common-mode output voltage, v_{cmi} (max., RMS)	92.8.3.1	30	mV
Differential peak-to-peak voltage, v_{df} (max)	92.8.3.1	1200[a]	mV
Differential output return loss (min)	92.8.3.2	See Equation (92–1)	dB
Transition time (20-80%, min.), no equalization[b]	92.8.3.4	8	ps
Far-end transmit output noise (max) Low insertion loss channel High insertion loss channel	92.8.3.4	 2 1	mV
Transmitter steady-state voltage, v_f	92.8.3.5.1	0.34 min, 0.6 max	V
Linear fit pulse peak (min)	92.8.3.5.1	$0.5 \times v_f$	V
Transmitted waveform max RMS normalized error (linear fit) abs coefficient step size minimum precursor fullscale ratio minimum post cursor fullscale ratio	 92.8.3.5.2 92.8.3.5.4 92.8.3.5.5 92.8.3.5.5	 0.037 0.0083 min, 0.05 max 1.54 4	
Max output jitter (peak-to-peak) Effective deterministic jitter excluding data dependent jitter Effective random jitter Even-odd jitter Total jitter excluding data dependent jitter	92.8.3.7	 0.15 0.15 0.035 0.28	 UI UI UI UI
Signaling rate, per lane	92.8.3.8	25.78125±100 ppm	GBd
Unit interval nominal	92.8.3.8	38.787879	ps

[a]The 100GBASE-CR4 Style-1 connector may support 100GBASE-CR4 or XLPPI interfaces. For implementations that support both interfaces, the transmitter should not exceed the XLPPI voltage maximum until a 100GBASE-CR4 cable assembly has been identified.

[b]Transmit equalization may be disabled by asserting the preset control defined in Table 45–60 and 45.2.1.81.3.

- **Tx and Rx function models validated at TP2 and TP3**

Receiver at TP3 characteristics

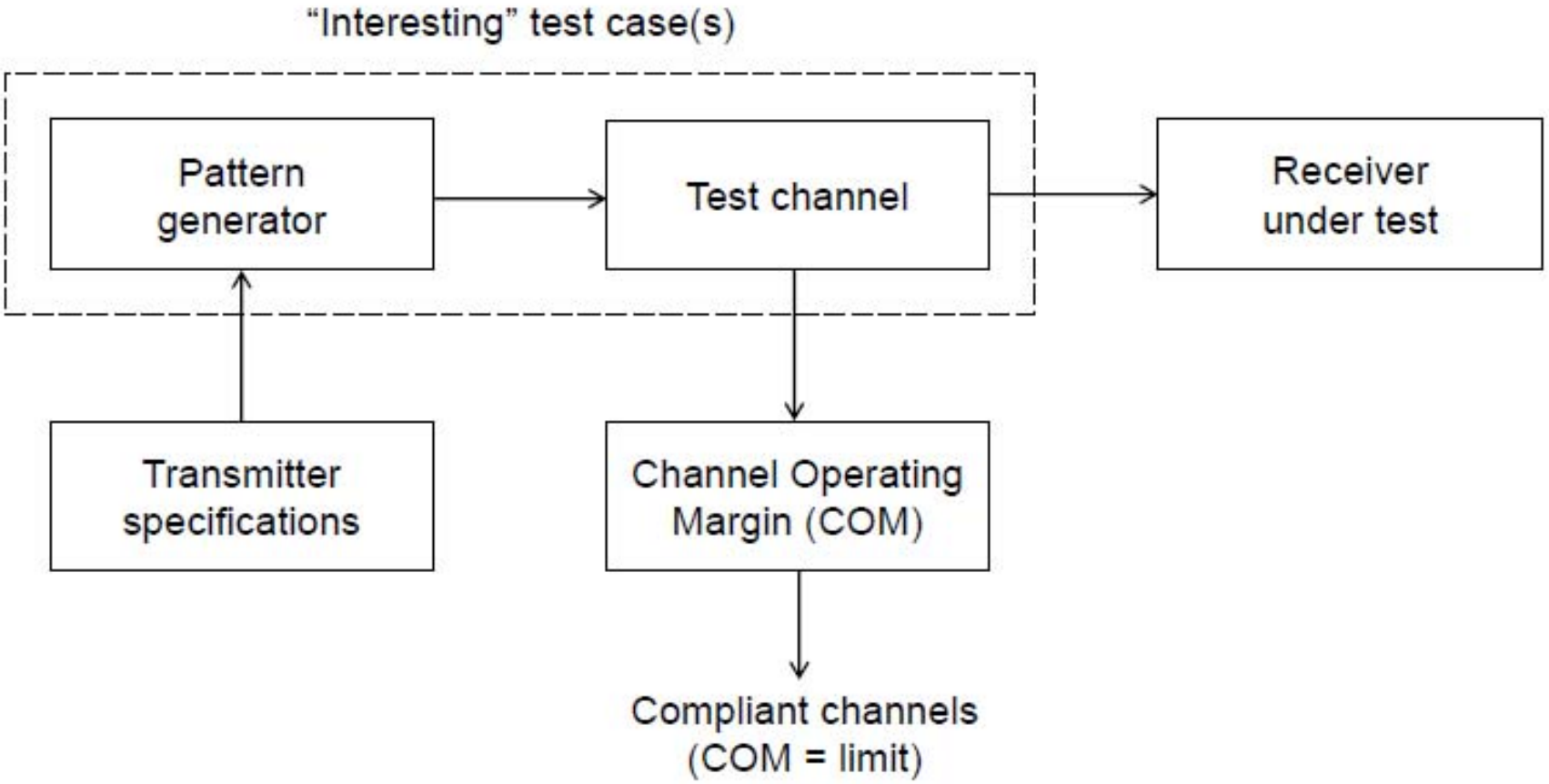
Table 92–8—Receiver characteristics at TP3 summary

Parameter	Subclause reference	Value	Units
Differential peak-to-peak input amplitude tolerance (max)	72.7.2.4	1200	mV
Differential input return loss (min)[a]	92.8.4.1	Equation (92–5)	dB
Differential to common-mode input return loss	92.8.4.2	10 min from 0.01 GHz to 19 GHz	dB
Bit error ratio	92.8.4.3	10^{-5} or better	
Signaling rate, per lane	92.8.4.5	25.78125 ± 100 ppm	GBd
Unit interval (UI) nominal	92.8.4.5	38.787879	ps

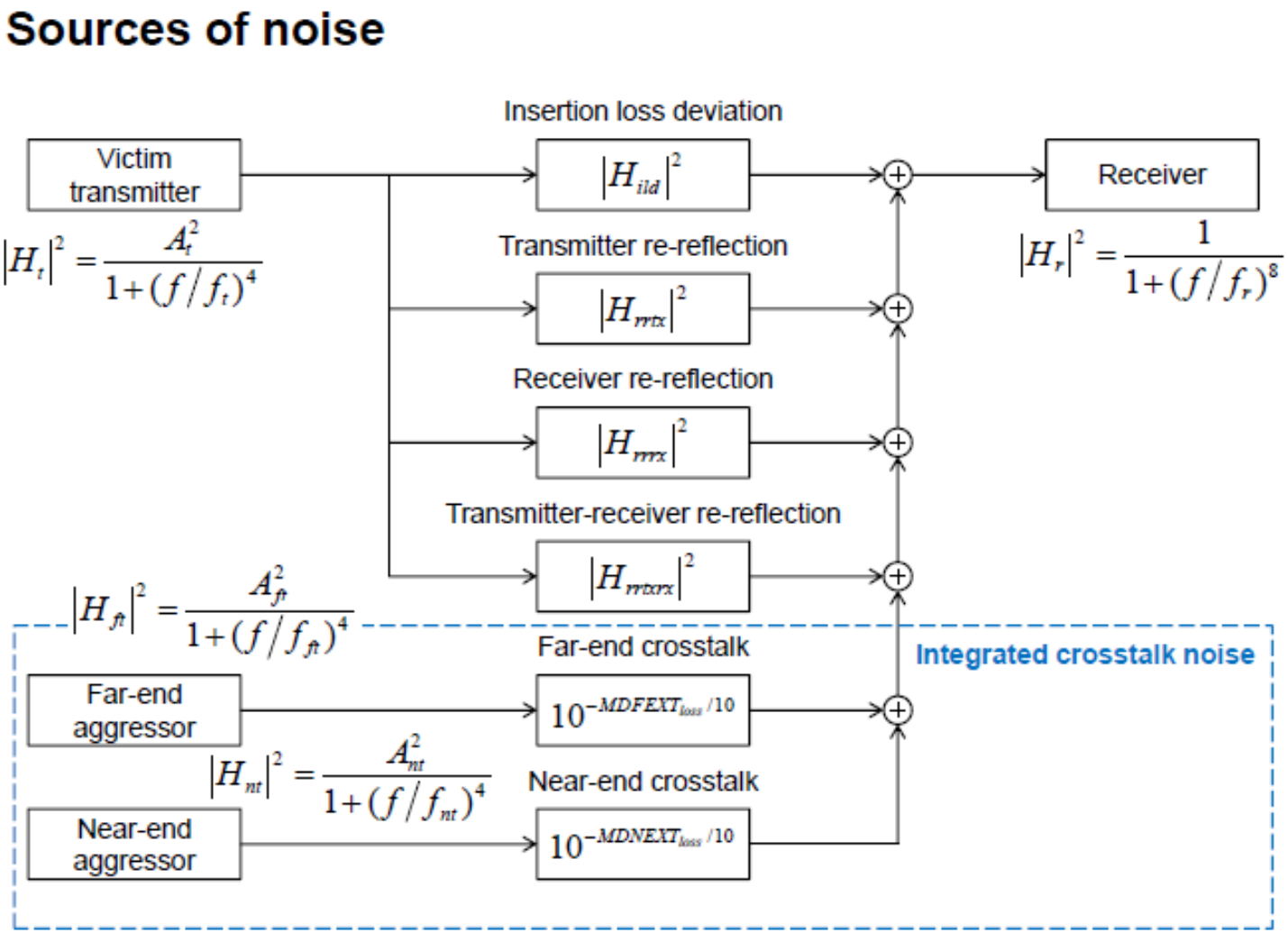
[a]Relative to 100 Ω differential.

- **Tx and Rx function models validated at TP2 and TP3**

100GBASE-CR4 - Receiver interference tolerance



Noise sources*

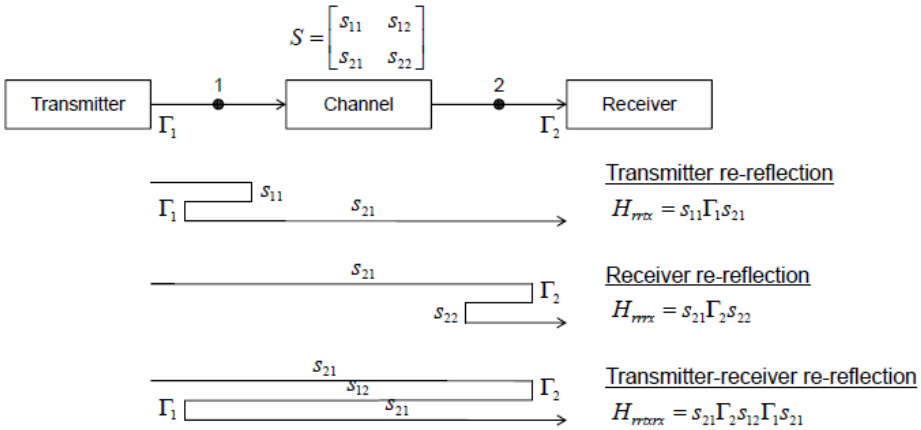


*Material extracted from:>> A method for evaluating channels, Charles Moore, Avago Technologies, Adam Healey, LSI Corporation
100 Gb/s Backplane and Copper Study Group Singapore, March 2011
http://www.ieee802.org/3/100GCU/public/mar11/moore_01_0311.pdf

Residual inter-symbol interference*

Re-reflection interference (noise)

- Transmitter, receiver, and channel return loss influence the transfer function of the assembled link



Transmitter re-reflection

$H_{rrtx} = s_{11}\Gamma_1 s_{21}$

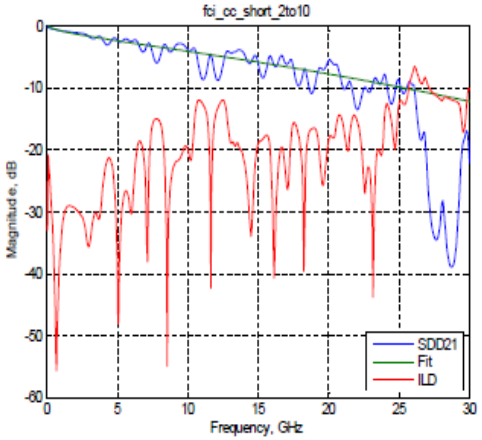
Receiver re-reflection

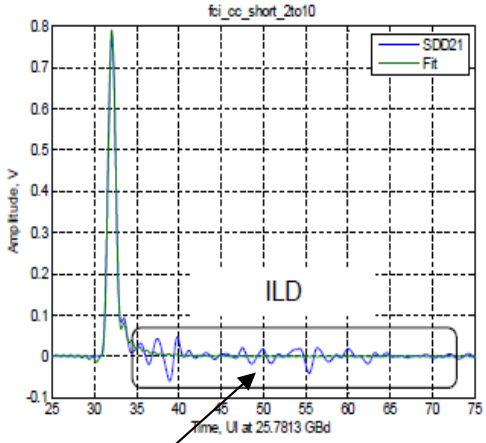
$H_{rrrx} = s_{21}\Gamma_2 s_{22}$

Transmitter-receiver re-reflection

$H_{rrtxrx} = s_{21}\Gamma_2 s_{12}\Gamma_1 s_{21}$

ILD noise example





•Residual inter-symbol interference

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http://www.ieee802.org/3/100GCU/public/mar11/moore_01_0311.pdf

802.3ba Integrated crosstalk noise

Transmitter rise time

$$|H_t(f)|^2 = \frac{1}{1+\left(fT_r/0.2365\right)^4}$$

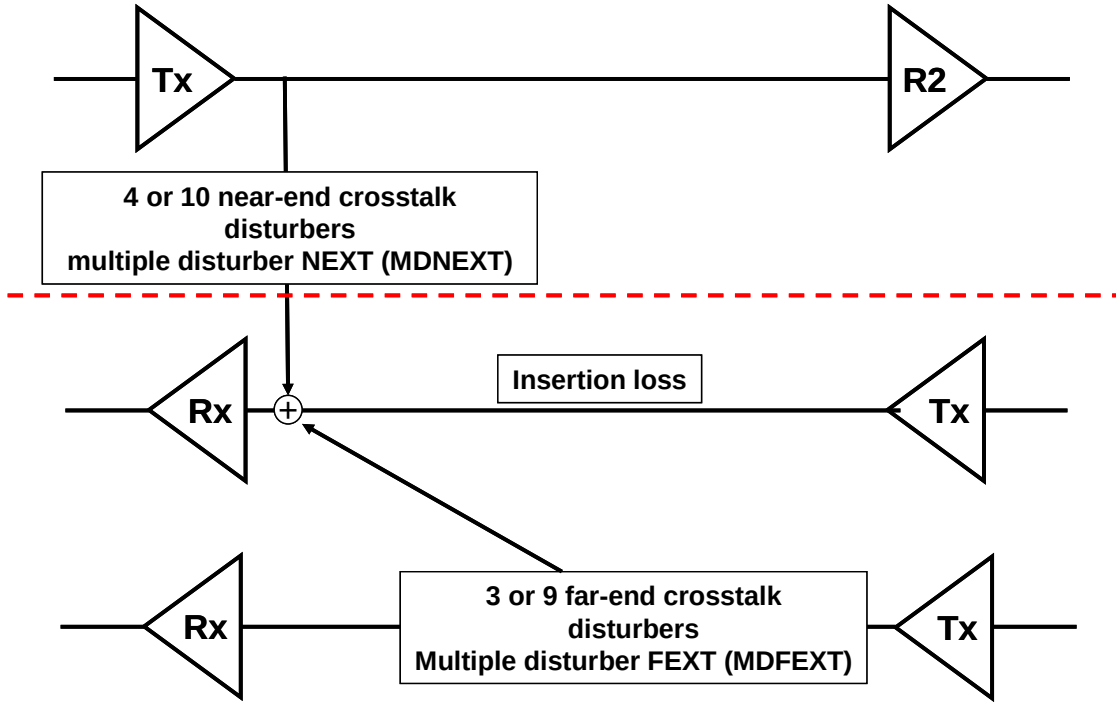
Multiple disturber crosstalk

$$|H_{nx}(f)|^2 = 10^{-MDNEXT_{loss}(f)/10}$$

$$|H_{nx}(f)|^2 = 10^{-MDFEXT_{loss}(f)/10}$$

Receiver filter

$$|H_t(f)|^2 = \frac{1}{1+\left(f/f_r\right)^8}$$

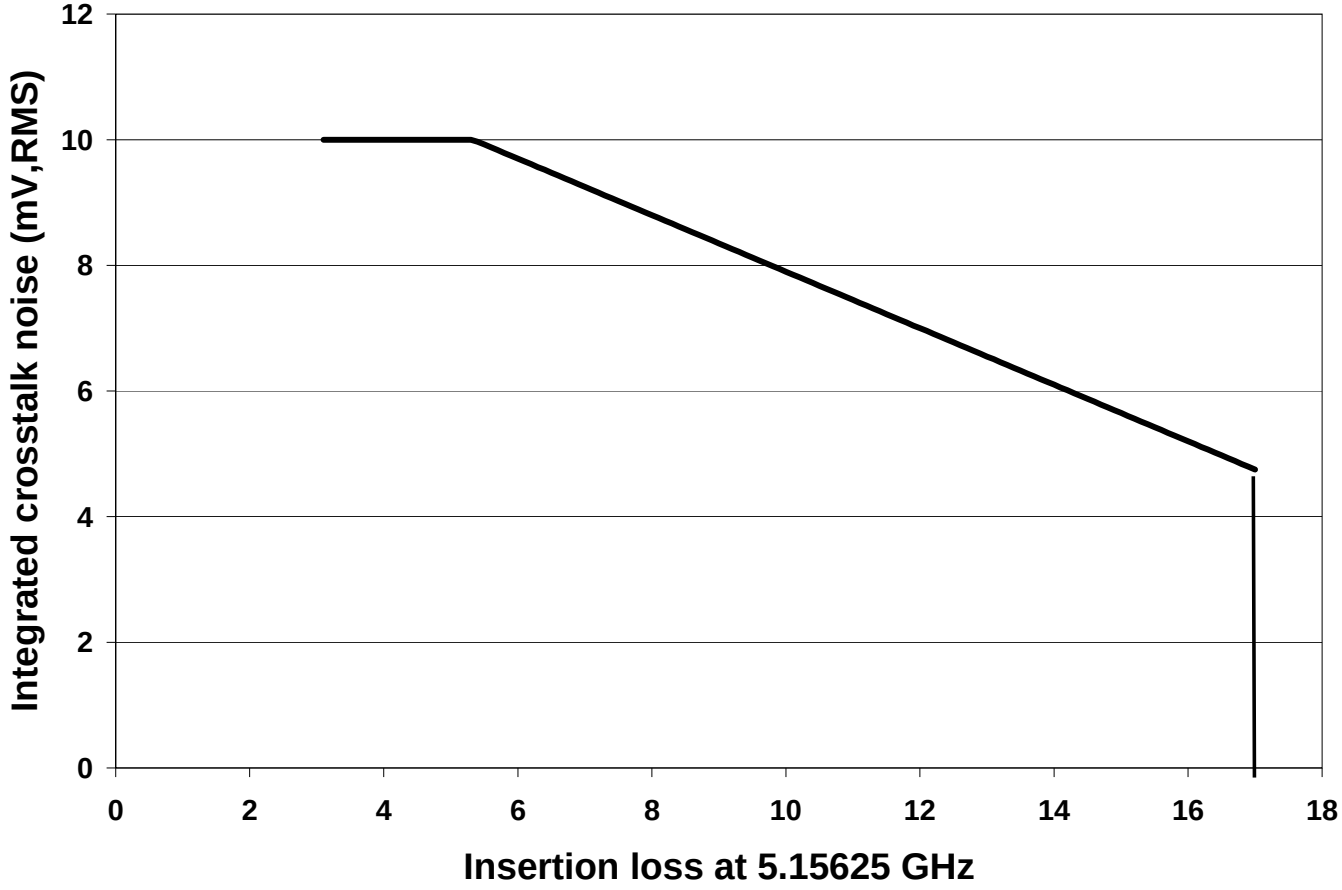


$$MDFEXT_{loss}(f) = -10\log_{10}\left(\sum_{i=1}^{i=3or9} 10^{-FEXT_{indiv}(f)/10}\right)$$

$$MDNEXT_{loss}(f) = -10\log_{10}\left(\sum_{i=1}^{i=4or10} 10^{-NEXT_{indiv}(f)/10}\right)$$

802.3ba Cable assembly ICN

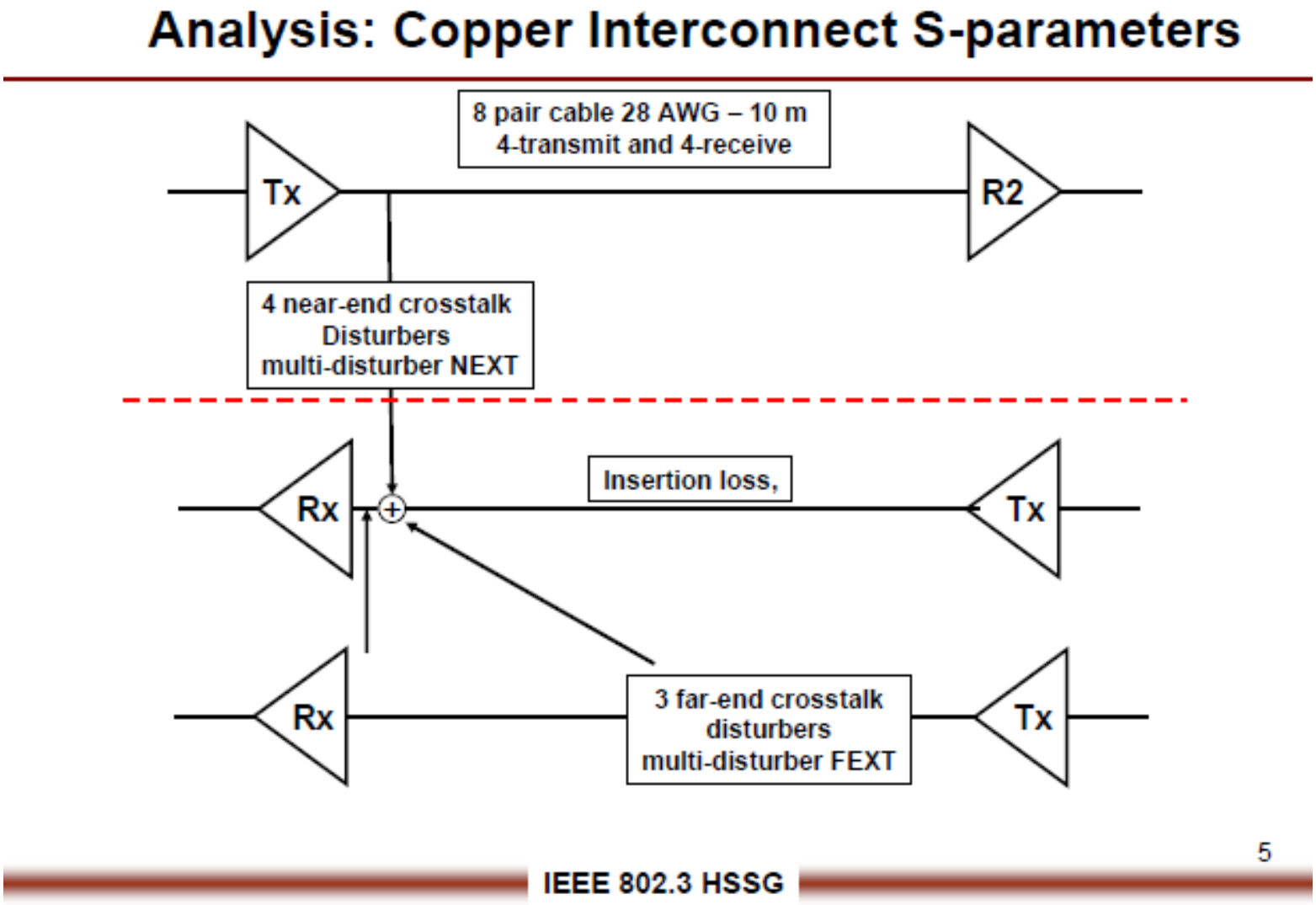
$$\sigma_{x,ca} \le \begin{Bmatrix} 10 & 3 \le IL \le 5.3 \\ 12.4 - 0.45IL & 5.3 < IL \le 17.04 \end{Bmatrix}$$



$$\sigma_{nx} = \left[2\Delta f \sum_{n} W_{nt}(f_n) 10^{-MDNEXT_{loss}(f_n)/10} \right]^{\frac{1}{2}}$$

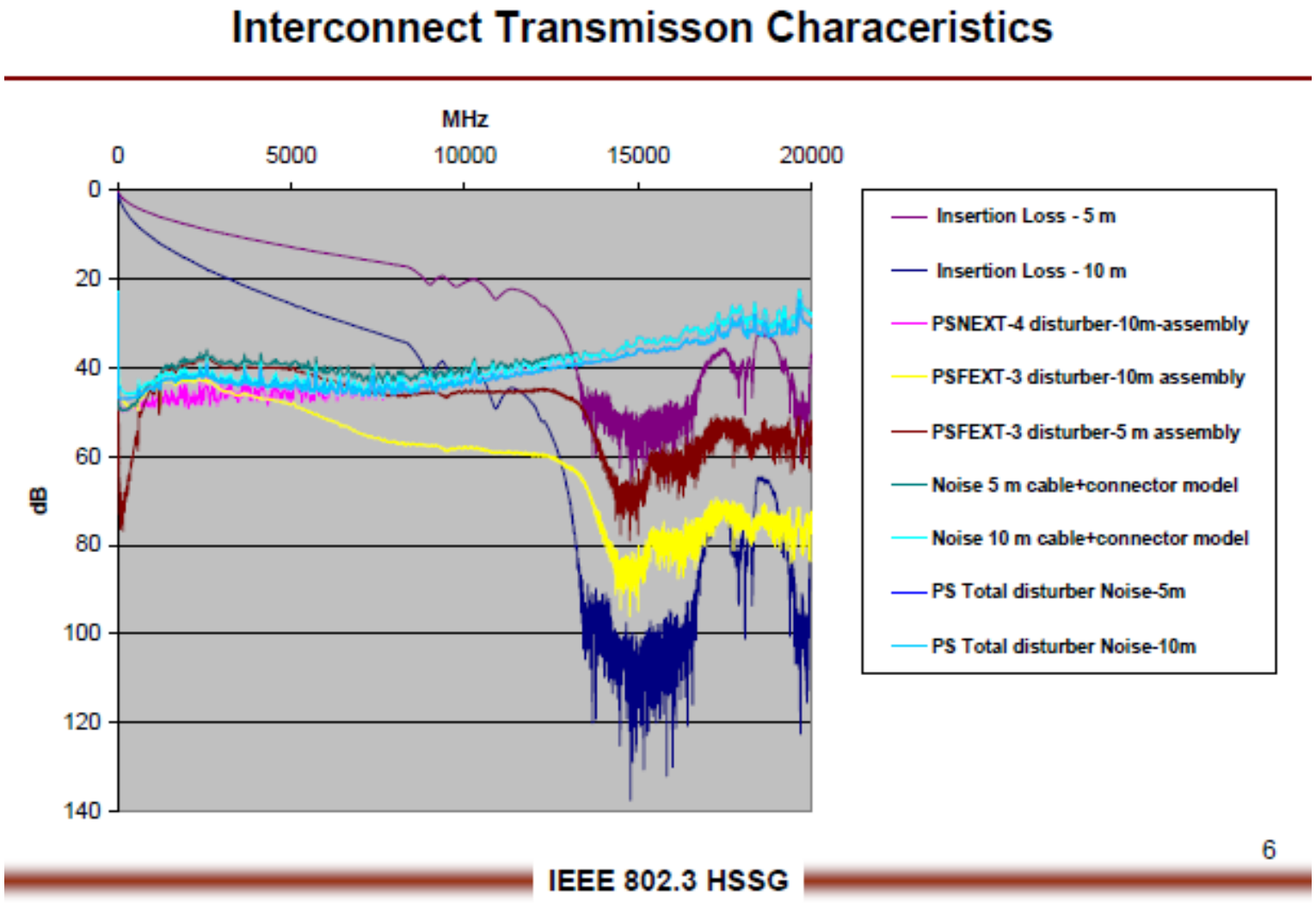
$$\sigma_{fx} = \left[2\Delta f \sum_{n} W_{ft}(f_n) 10^{-MDFEXT_{loss}(f_n)/10} \right]^{\frac{1}{2}}$$

Feasibility of a 100 Gb/s copper interconnect



Source: http://www.ieee802.org/3/hssg/public/nov06/diminico_02_1106.pdf
Feasibility of a 100 Gb/s copper interconnect
diminico_02_1106.pdf

Feasibility of a 100 Gb/s copper interconnect



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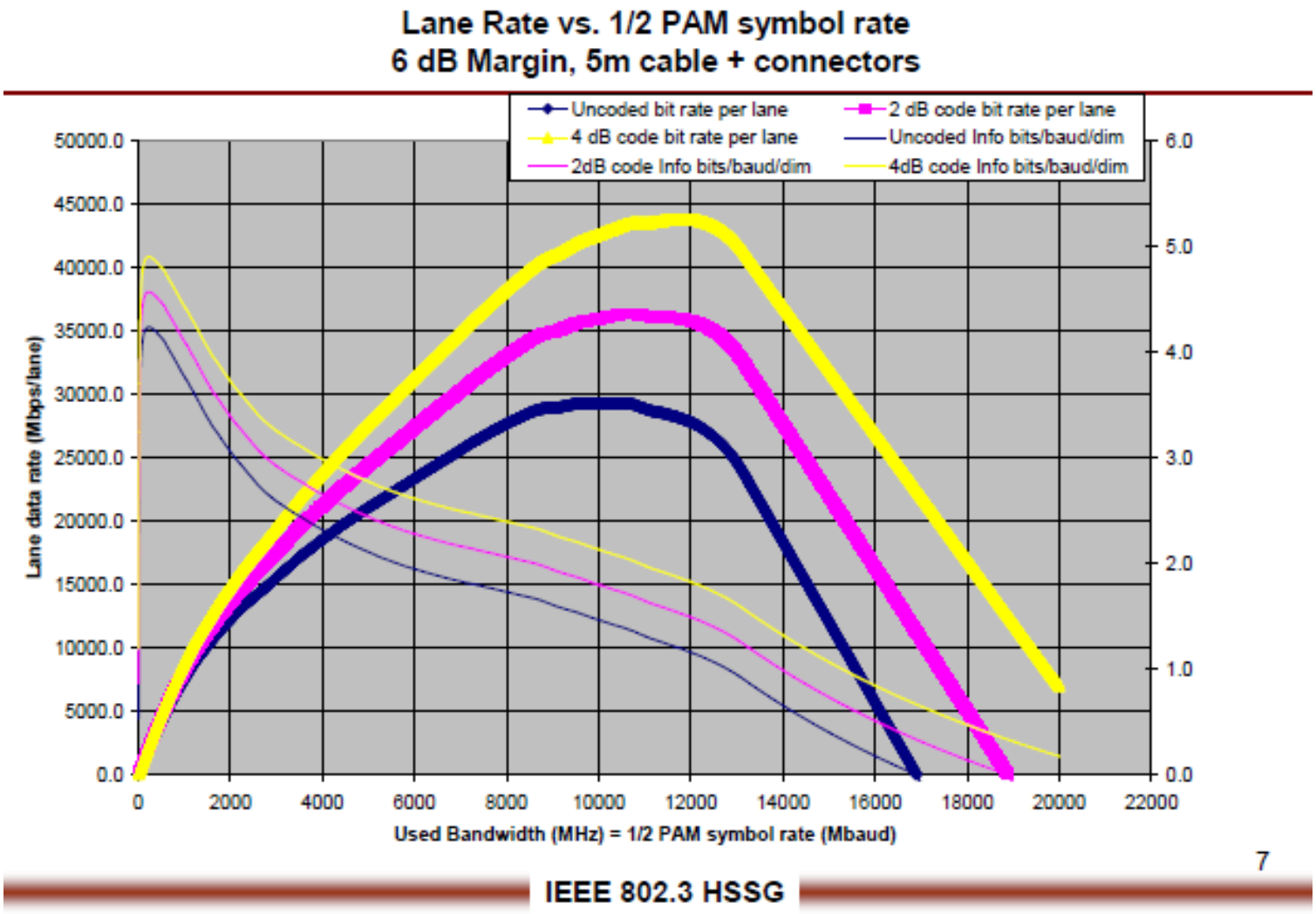
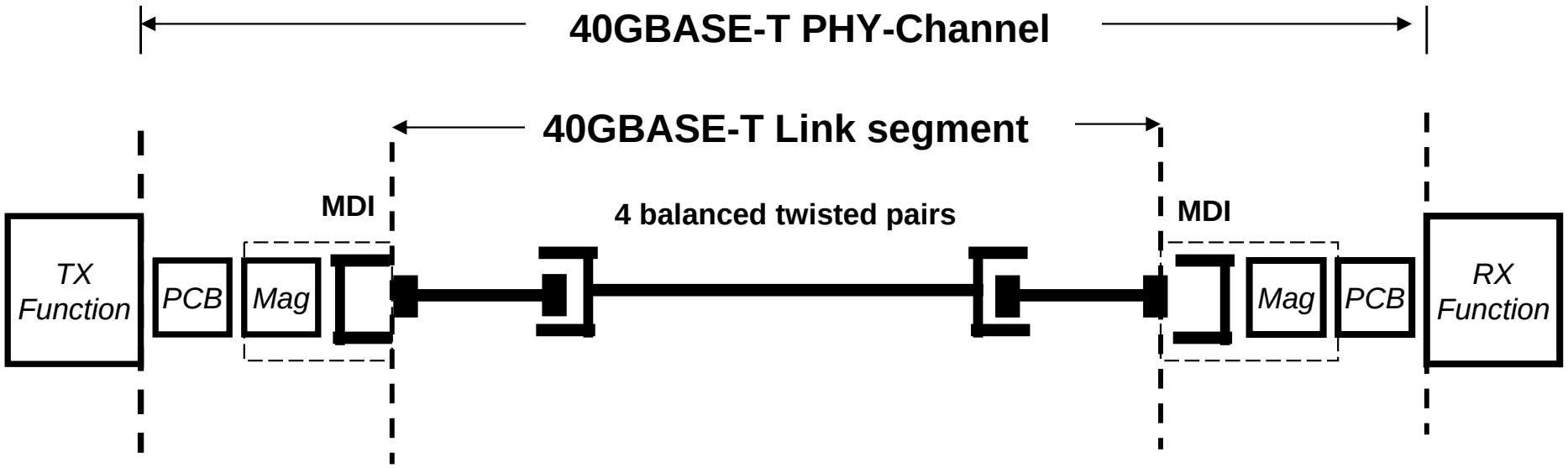


Source: George Zimmerman contributed analysis
http://www.ieee802.org/3/hssg/public/nov06/diminico_02_1106.pdf
Feasibility of a 100 Gb/s copper interconnect
diminico_02_1106.pdf

40GBASE-T PHY- Channel

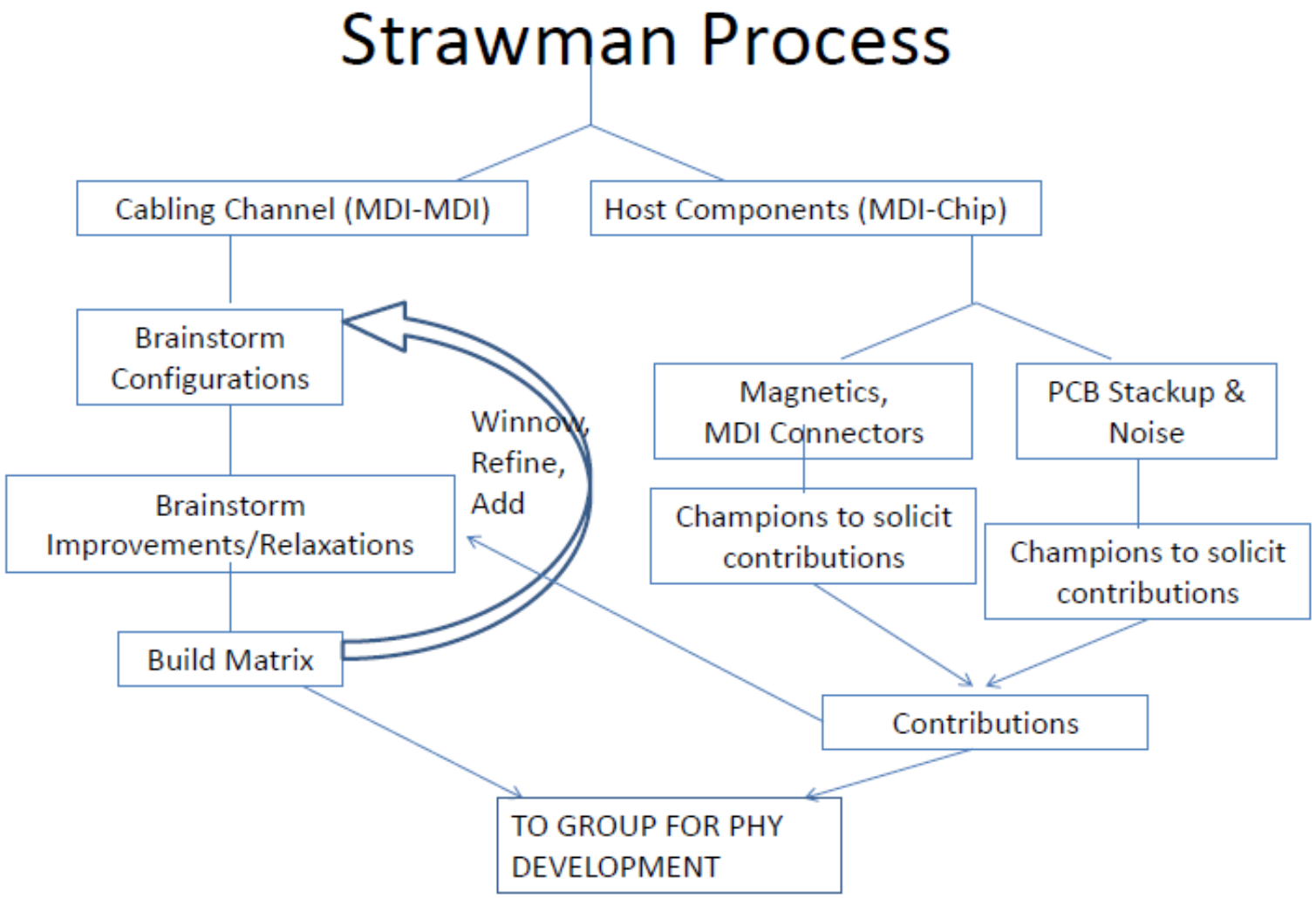


Modeling to optimize PHY and PHY-channel performance

PHY-Channel

- MDI/Magnetics
- Host PCB
- Link segment - based upon copper media specified by ISO/IEC JTC1/SC25/WG3 and TIA TR42.7
  - –4 pair, balanced twisted-pair copper cabling
  - –Up to 2 connectors
  - –Up to at least 30 meters

Channel Model Ad Hoc - Proposal for Path Forward



Source: http://www.ieee802.org/3/bq/public/channelmodeling/index.html
Potential Path Forward for Channel Modeling Ad Hoc - updated during meeting zimmerman_02_0513_40GBTah.pdf

Channel Model Ad Hoc - Proposal Channel Configurations

Possible Channel Configurations

- "X-Axis" – Cable classes
  - A: ISO Class 1, up to 30m (x-y-z)
  - B: ISO Class 2, up to 30m (x-y-z)
  - C: TIA Category 8, up to 30m (x-y-z)
    - Can this be merged with A?
- "Y-Axis" – Topologies/lengths
  - D: Short channels
    - 150mm-3m-150mm ("really short") – Worst case reflection #1
    - 0.5m-3m-0.5m ("pretty short") - Worst case reflection #2
    - 3m - Endpoint to TOR
    - 5m TOR-adjacent
  - E: Other target channels
    - 1m-10m-1m (ISO short reference channel)
    - 30m
    - 30m single patch cord (assuming there is one that meets IL…)
    - 30m asymmetric #1 (1m-26m-3m) – Data center configuration #1
    - 30m asymmetric #3 (1m-24m-5m) – Data center configuration #2
- "Z-Axis" Improvements/Relaxations on A, B, C (reference grimwood_01_0513_40GBT.pdf); "What if" scenarios
  - Improvements
    - 2, 4, 6 dB improved RL
    - 2, 4 dB improved PSNEXT (A,C)
    - Coupling attenuation (Example: Class I/Class II – Contributions show that cabling "far exceeds" current specification)
  - Relaxations
    - Bandwidth (1.6GHz vs. 2.0GHz)
    - Others TBD

Source: http://www.ieee802.org/3/bq/public/channelmodeling/index.html
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