Strawman for PHY Baseline Proposal

Contribution to IEEE 802.3: 40G-BASE-T PHY Baseline Proposal Ad Hoc
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Overview

- Motivation

- Prior Results

- Baseline Proposal

- Analysis

- Further work

Motivation

- Repeated analog front end power estimates show 40GBASE-T optimum PHY power using between 1400MHz and 1750 MHz

  – Drives spectral efficiency (bits/sec/Hz/pair) close to 10GBASE-T specification

- Reuse of existing technical approaches reduces risk and improves time-to-standard

  – Does not preclude 'upgrading' possible areas

Prior Results
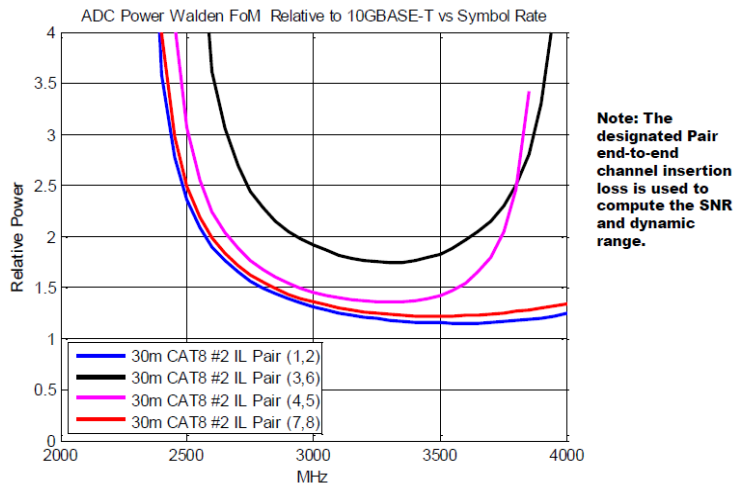
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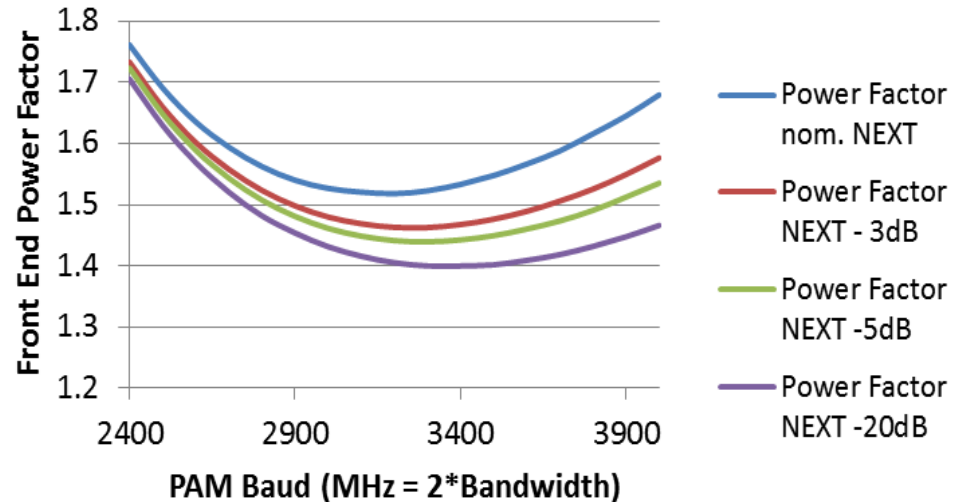
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- Refinement of models continues to show broad AFE power optimum between 2800 Mbaud and 3700 Mbaud PAM (1400 to 1850 MHz used)
  - Upper and lower frequencies get sharper, but optimum remains broad

Baseline Proposal

- Baseline PHY proposal:
  - Use PCS, Framing and Line Coding from Clause 55
  - Increase symbol rate 4X to 3200 Mbaud
  - Drop transmit power to ~ 0 dBm at MDI
- Areas for improvement/consideration:
  - Backchannel for THP dynamic update?
  - Revised FEC to cover uncoded bits?
    - Multiple ways of doing this
  - Faster startup?
  - Negotiated patch-cord operational mode?
  - Remove PBO?

Analysis

- Analog power is well modeled
  - Analysis shows 1.3 to 1.5X 10GBASE-T AFE receiver power
  - Transmit power should be reduced
- Digital power will be <4x 10GBASE-T digital power
- First-order power computation suggests 4 to 5W PHY based on current-gen 10GBASE-T
  - Biased towards digital power, so it will benefit from reductions in digital power consumption

Further Work

- PHY vendors to analyze DSP cancellation architectures for savings relative to 10GBASE-T

- Proponents to consider what modifications to 10GBASE-T are desirable & justify benefits

- Power estimation to be refined to validate

- OR: alternative strawmen to be proposed!