40GBASE-T
PHY- Channel insertion loss

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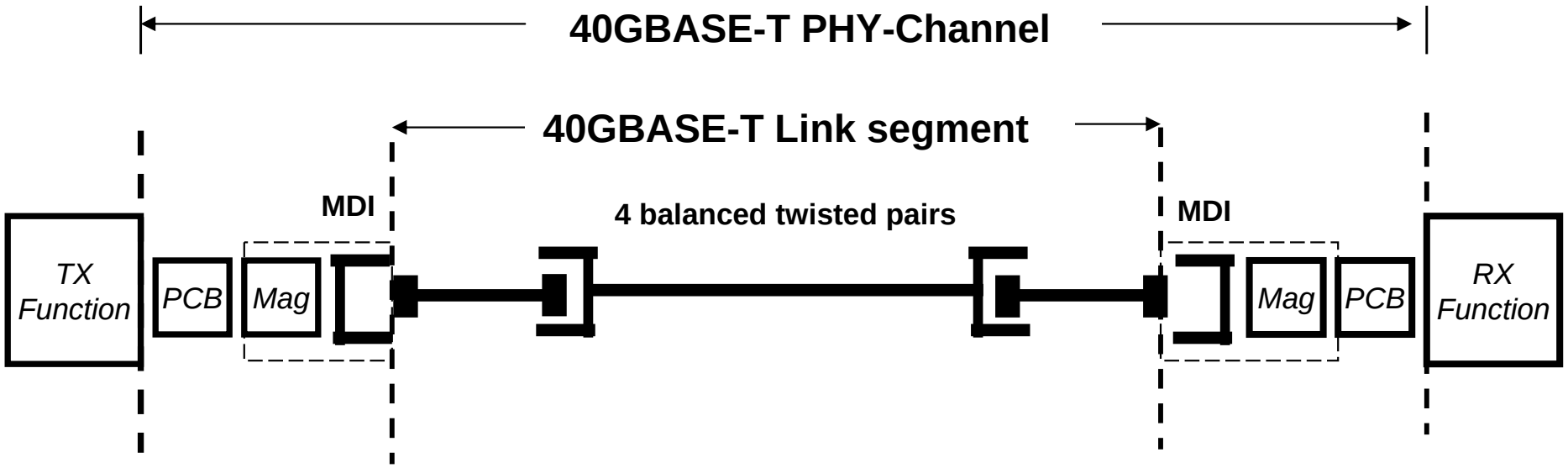
Purpose

- Specifications for 40GBASE-T
  - PHY-channel insertion loss budget
    - Host loss budget
      - ✓PCB- trace length and material
      - ✓Magnetics/MDI
    - Link segment insertion loss

40GBASE-T PHY- Channel



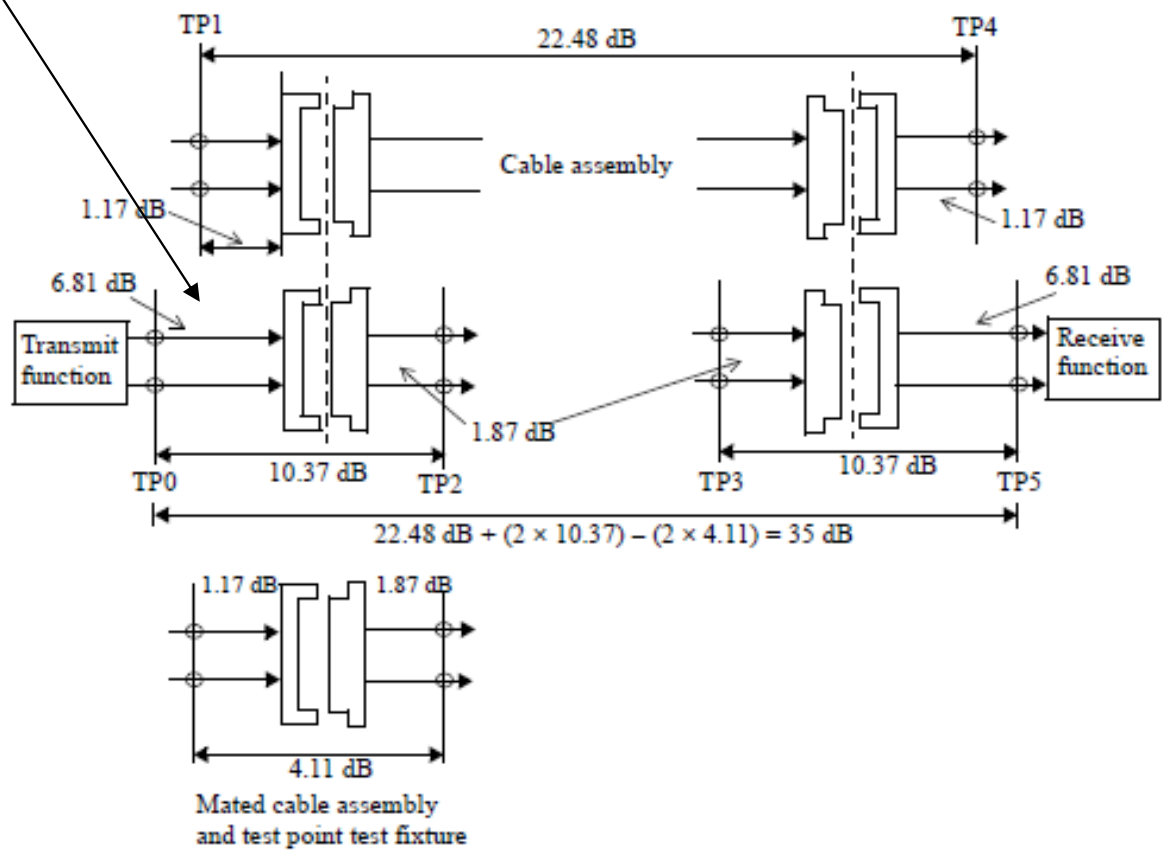
Modeling to optimize PHY and PHY-channel performance

PHY-Channel

- MDI/Magnetics
- Host PCB
- Link segment - based upon copper media specified by ISO/IEC JTC1/SC25/WG3 and TIA TR42.7
  - –4 pair, balanced twisted-pair copper cabling
  - –Up to 2 connectors
  - –Up to at least 30 meters

802.3bj - Channel loss budget

- **100GBASE-CR4 channel loss budget**
  - **5 m cable assembly**
  - **4” host trace - ~1.5924 @ 12.89 GHz**



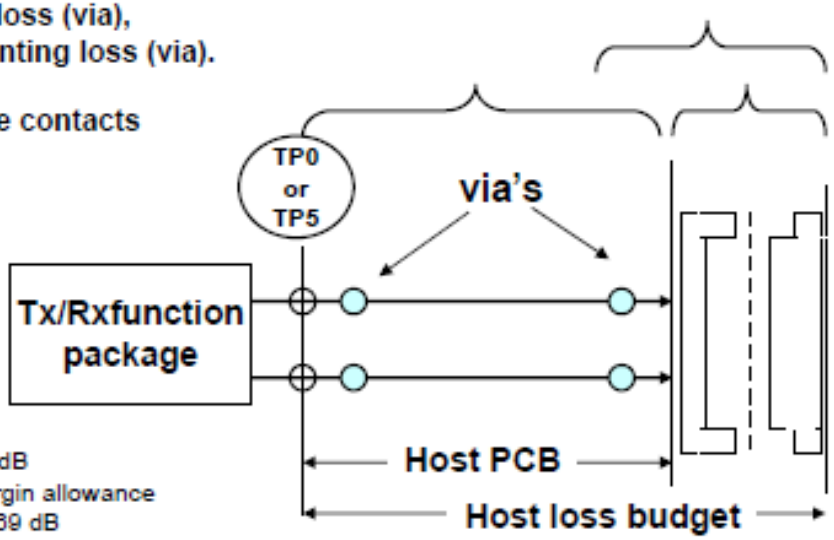
NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

Figure 92A–2—35 dB channel insertion loss budget at 12.8906 GHz

802.3bj - Host loss budgets

Host loss budget IL proposal

Host loss budget includes
- Chip/ball mounting loss (via),
- MDI receptacle mounting loss (via).
- MDI receptacle
- Plug connector edge contacts



Note: recommend 0.62 dB
host connector loss margin allowance
1.07 dB + 0.62 dB = 1.69 dB

Reference	Host PCB	Mated Connector	Host loss budget - 12.89 GHz	Host loss budget – 14 GHz
CEI-28G-VSR Nov11	7.3 dB 14 GHz (PCB+2 via's) (2 via's[0.5 dB] + host trace[6.8 dB]) (4" N4000-13 or slightly worse material (up to 1.7dB/in) at 14GHz	1.2 dB @ 14 GHz	8.5 dB	8.50 dB
Diminico_01_0312.pdf	6.36 dB @ 12.89 GHz (1.59 dB/in) 6.8 dB @ 14.00 GHz (1.7 dB/in) (2 via's[0.45 dB] @ 12.89 GHz (2 via's[0.50 dB] @ 14.00 GHz	1.07 dB @ 12.89 GHz 1.20 dB @ 14.00 GHz 0.62 dB @ 12.89 GHz*	8.5 dB	8.50 dB

4

802.3bj Cu specifications

Source: http://www.ieee802.org/3/bj/public/mar12/diminico_01a_0312.pdf
IEEE 802.3bj: 100GBASE-CR4 Test Points and Parameters
diminico_1a_0312.pdf

802.3bj – Host PCB losses

Problem Brought to Light

- Inconsistent loss numbers used in discussions
  - Improved FR4:
    - 38.2dB loss for 40in and 2 connectors (beukema_01_1111)
    - 1.04dB/in **w/o** surface roughness (kipp_01_1111, originally goergen_01_0911)
  - Megtron6:
    - 0.9dB/in (ghiasi_01_1111)
    - 0.65-0.68dB/in (kipp_01_1111)
    - 30.2dB for 1m and 2 connectors (meghelli_01_0911, originally patel_01_0911)
- Consensus group formed with goal:

  Create acceptable loss parameters (dB/length) for 802.3bj Task Force to use in discussions in order to avoid miscommunication due to varied assumptions.

Proposal for Defining Material Loss **Elizabeth Kochuparambil Cisco**
Joel Goergen
26-Jan 12
http://www.ieee802.org/3/bj/public/jan12/kochuparambil_01a_0112.pdf

802.3bj – Host PCB losses

What Do We Know?

- Definition of Improved FR-4
- Variation exists in many forms within the PCB
  - Design specifics - Trace width, stackup, etc
  - Surface roughness – Manufacturer, pre-lam adhesion treatment, etc.
  - Lamination – "Football effect", temp., pressure, book size, etc.
  - Circuit tolerances – Line width control, dielectric thickness, trace cross section, etc.

Slide from goergen_01_0511:

Definition: "Improved FR-4" as defined by IEEE P802.3ap

- Improved FR-4 (Mid Resolution Signal Integrity):
  - 100Mhz: Dk ≤ 3.60; Df ≤ .0092
  - 1Ghz: Dk ≤ 3.60; Df ≤ .0092
  - 2Ghz: Dk ≤ 3.50; Df ≤ .0115
  - 5Ghz: Dk ≤ 3.50; Df ≤ .0115
  - 10Ghz: Dk ≤ 3.40; Df ≤ .0125
  - 20Ghz: Dk ≤ 3.20; Df ≤ .0140
- Temperature and Humidity Tolerance (0-70degC, 10-90% non-condensing):
  - Dk:+/- .04
  - Df: +/- .001
- Resin Tolerance (standard +/-2%):
  - Dk:+/- .02
  - Df: +/- .0005

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802.3bj – Host PCB losses

Attenuation* (dB/in) at:	1 GHz	6.5 GHz	7 GHz	12.89 GHz	14 GHz
Meg6_LowSR – Wide	0.0951	0.4159	0.4433	0.7562	0.8127
Meg6_LowSR – Narrow	0.1466	0.5849	0.6205	1.0152	1.0847
Meg6_HighSR – Wide	0.1175	0.5960	0.6367	1.0891	1.1688
Meg6_HighSR – Narrow	0.1856	0.8971	0.9557	1.5924	1.7020
ImpFR4_LowSR – Wide	0.1202	0.6096	0.6541	1.1772	1.2734
ImpFR4_LowSR – Narrow	0.1717	0.7794	0.8323	1.4410	1.5512
ImpFR4_HighSR – Wide	0.1427	0.7904	0.8484	1.5158	1.6367
ImpFR4_HighSR – Narrow	0.2106	1.0930	1.1692	2.0283	2.1813

PROPOSED PARAMETERS; GRAPHS ON PREVIOUS SLIDE

*using Algebraic Model v2.02a – see backup slides for values entered in Model

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802.3ap – ~~Host PCB losses

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26-Jan 12	**Joel Goergen**	

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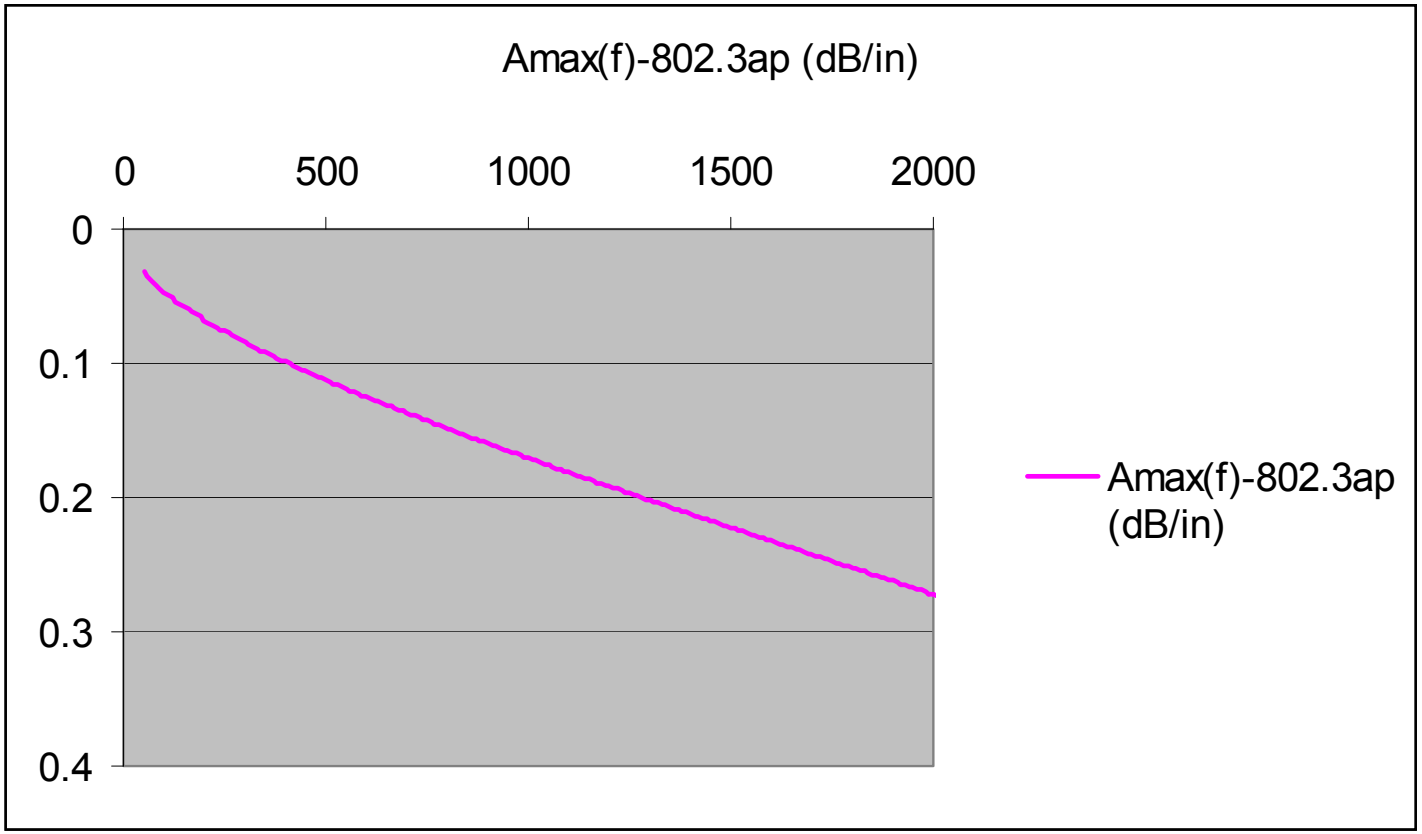
802.3bq – Host PCB losses



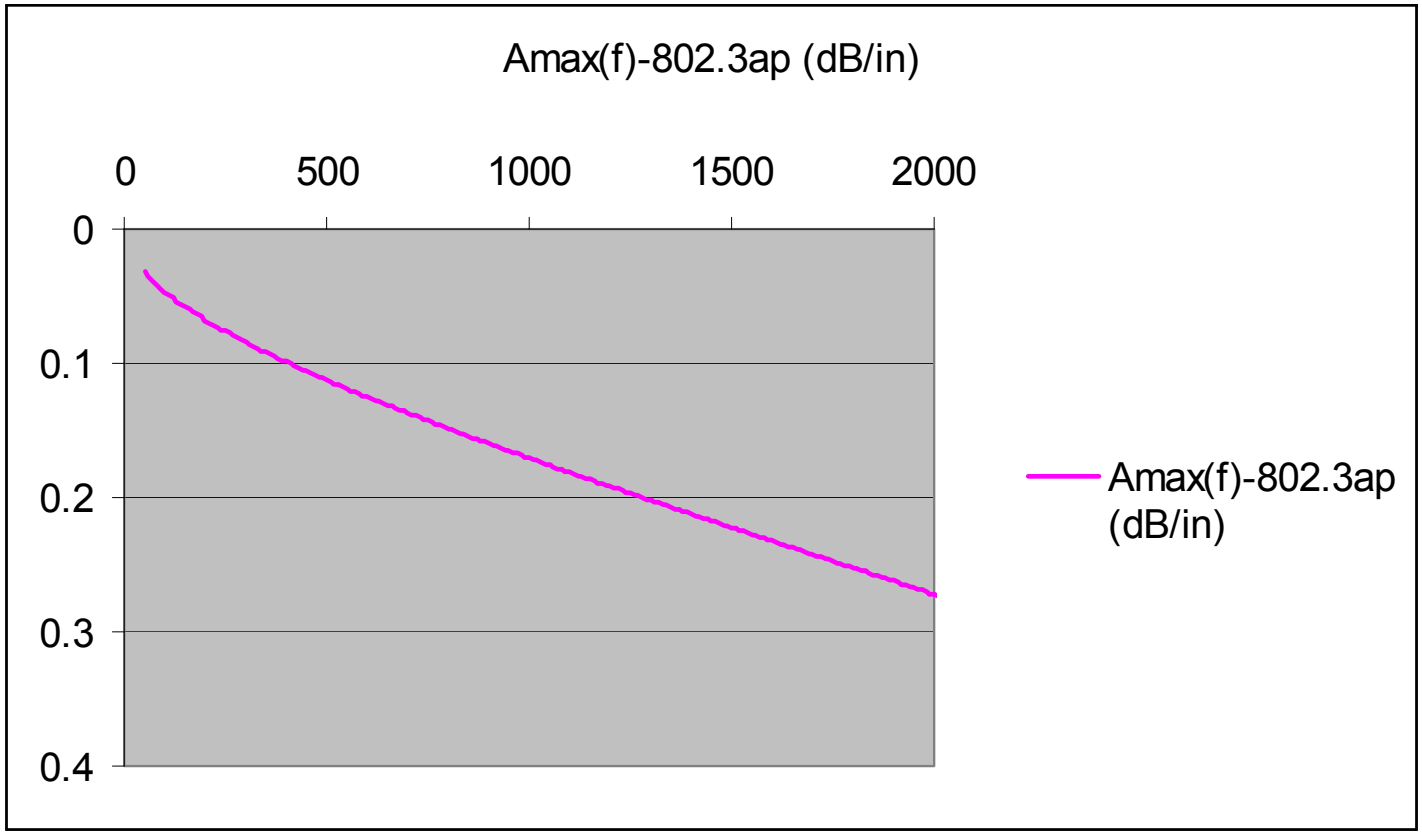
802.3ap
PCB up to at least 1 m

MHz	Amax(f)-802.3ap	dB/in
1000	6.7164	0.1706
2000	10.7082	0.2721
6500	29.0969	0.7392
7000	31.2668	0.7944
12890	55.8973	1.4202
14000	59.8078	1.5195

$$A(f) \le A_{max}(f) = 20\log_{10}(e) \times (b_1\sqrt{f} + b_2 f + b_3 f^2 + b_4 f^3) \quad \text{where } f \text{ is expressed in Hz}$$

b_1	2.00×10^{-5}	
b_2	1.10×10^{-10}	
b_3	3.20×10^{-20}	
b_4	-1.20×10^{-30}	

802.3bq – Host PCB losses



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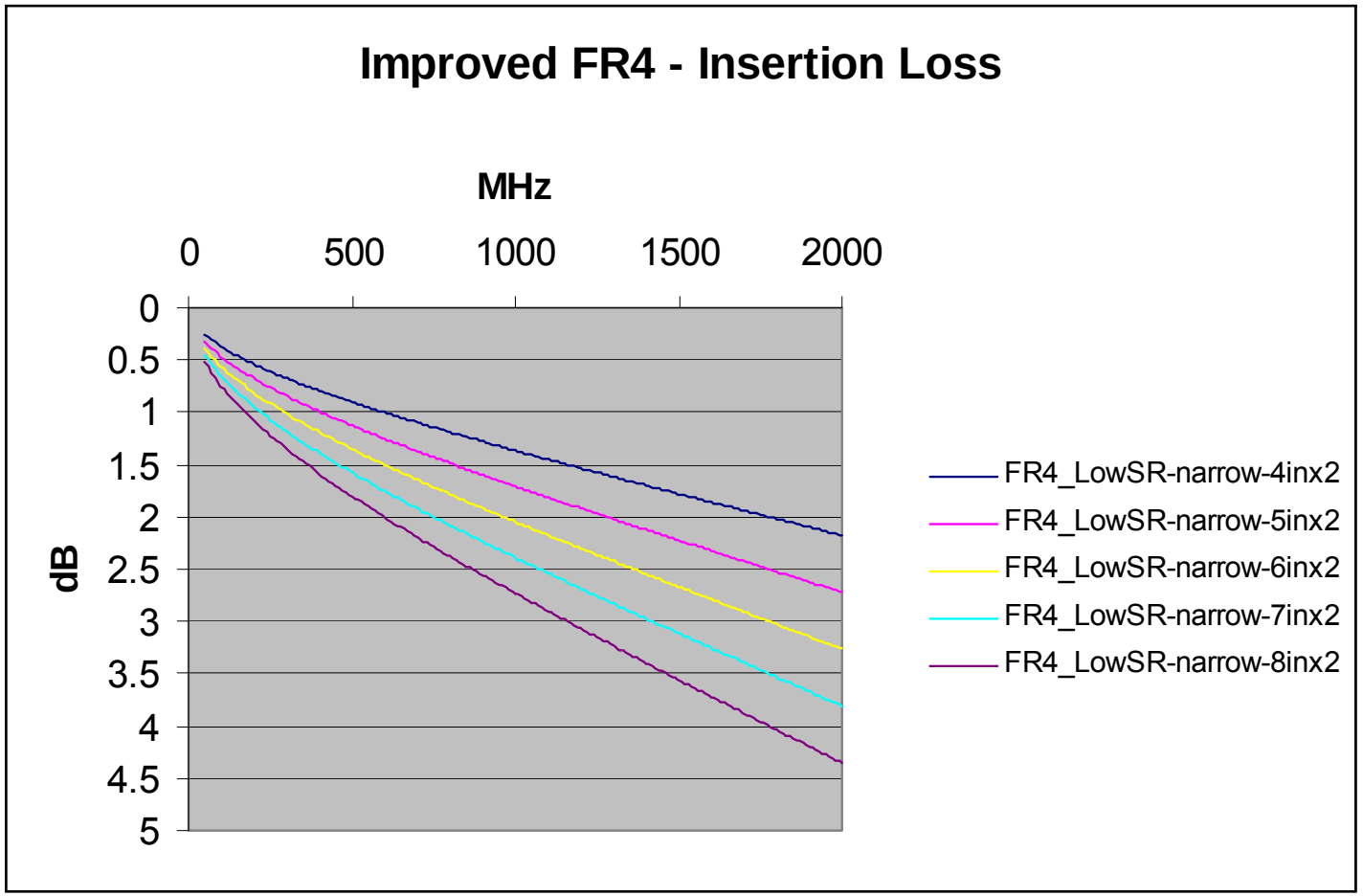

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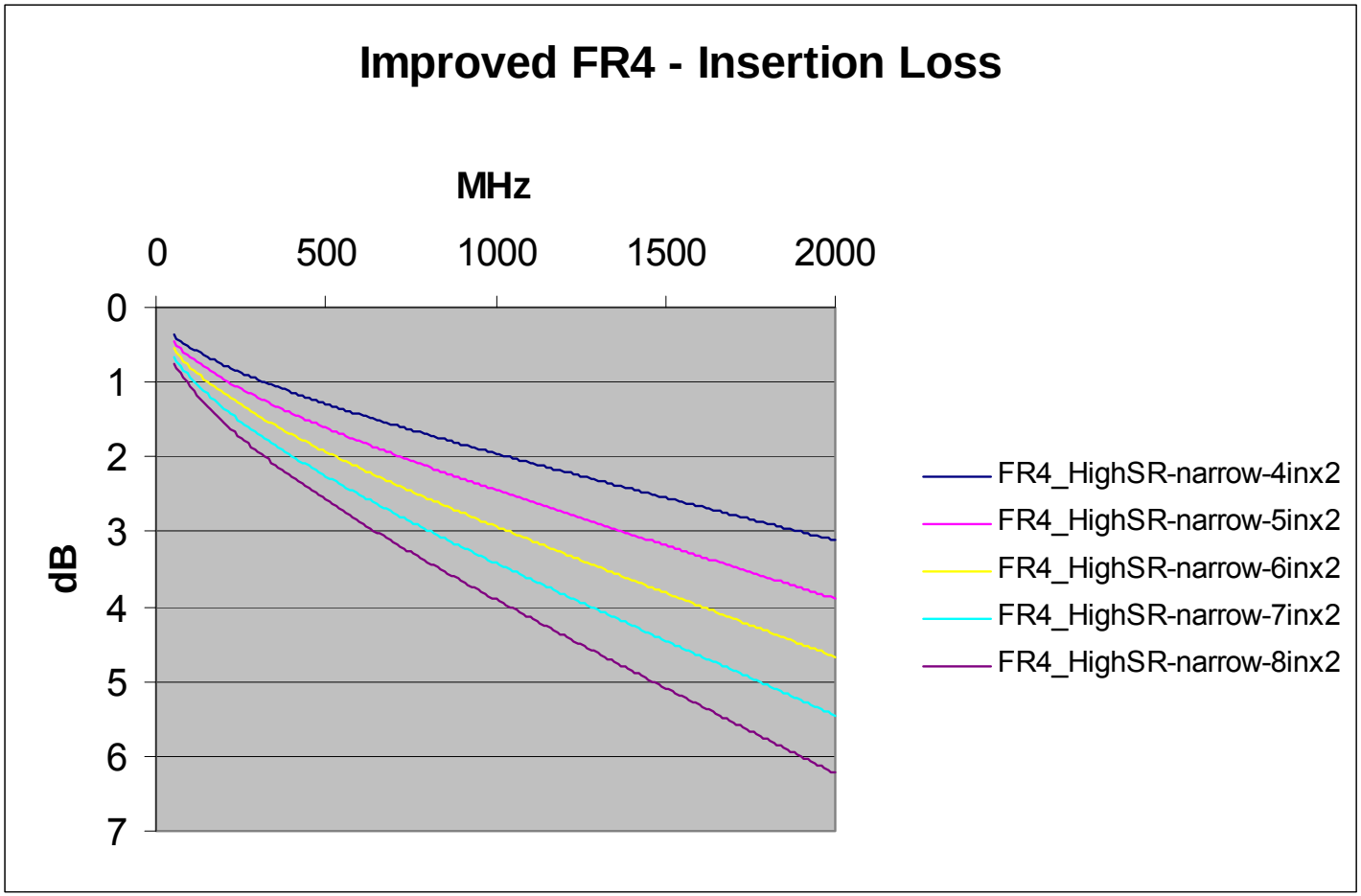
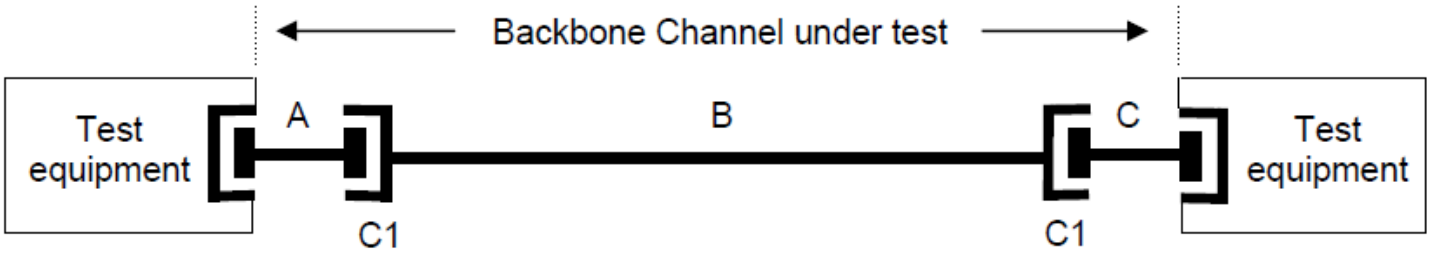
802.3bq – Host PCB losses



MHz	1.43*(Amax(f)-802.3ap)	dB/in
1000	9.6045	0.2440
2000	15.3127	0.3890
6500	41.6085	1.0571
7000	44.7115	1.1360
12890	79.9331	2.0308
14000	85.5252	2.1729

Category 8 (d0.7) – Channel Insertion Loss

schematic representation of a backbone channel test configuration



Legend

Cables and cords
Equipment cord .....A, C
Backbone cabling..... B

Connecting hardware
Interconnect C1

Channel insertion loss = 2*connecting hardware IL+ Cable IL +$ILD_{channel}$

Cable (100m) = 1≤f≤2000 (TBD) = 1.8*sqrt(f)+0.005*f+(0.25/sqrt(f)) (TBD)

Connecting Hardware=
1≤f≤500 (TBD) 0.02*sqrt(f) (TBD)
500<f≤2000 (TBD) 0.008*sqrt(f)+0.00029*f+0.5*10^(-6)*f^2 (TBD)

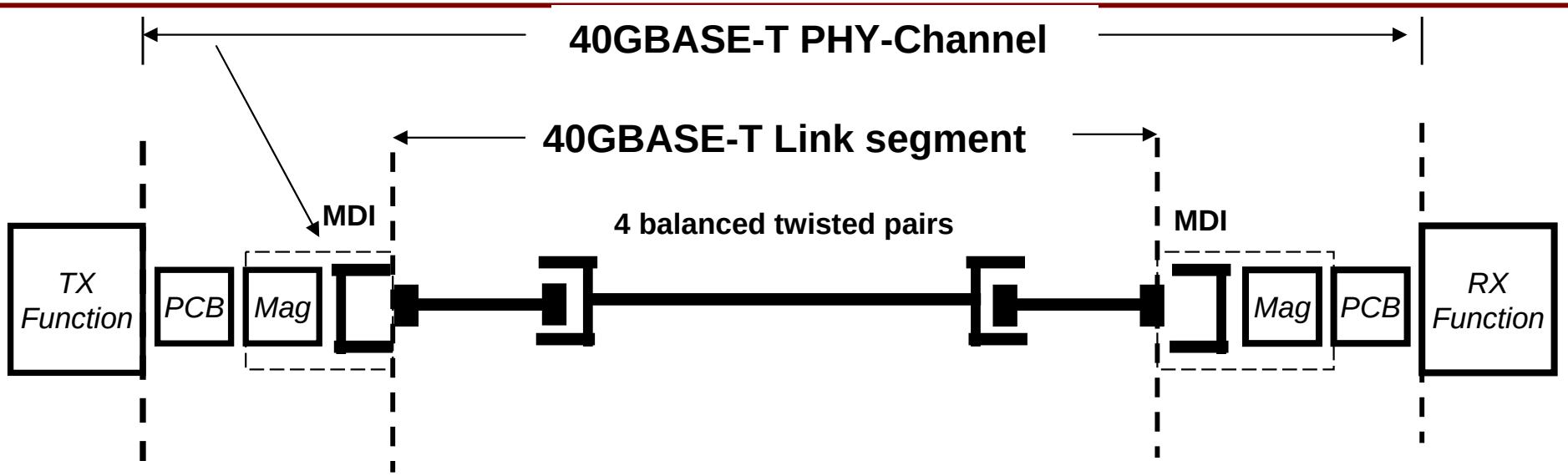
Patch cord cable = 1.2*(cable IL) (TBD)

$ILD_{channel}$ = 0.0324 *sqrt(f_{MHz}) (TBD)

Category 8 (d0.7) – Channel IL – 30m – 3m-24m-3m

F[MHz]	Category 8 - 30 m Channel IL
1	0.7
4	1.3
8	1.8
10	2.0
16	2.6
20	2.9
25	3.2
31.25	3.6
62.5	5.1
100	6.5
200	9.3
250	10.4
300	11.5
400	13.3
500	15.0
600	16.6
1000	22.4
1500	29.1
2000	35.6

MDI (Medium Dependent Interface)



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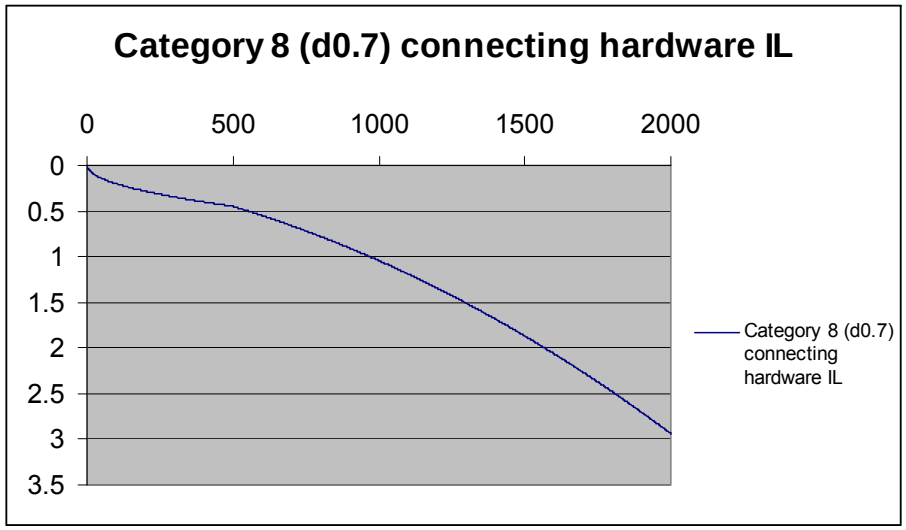
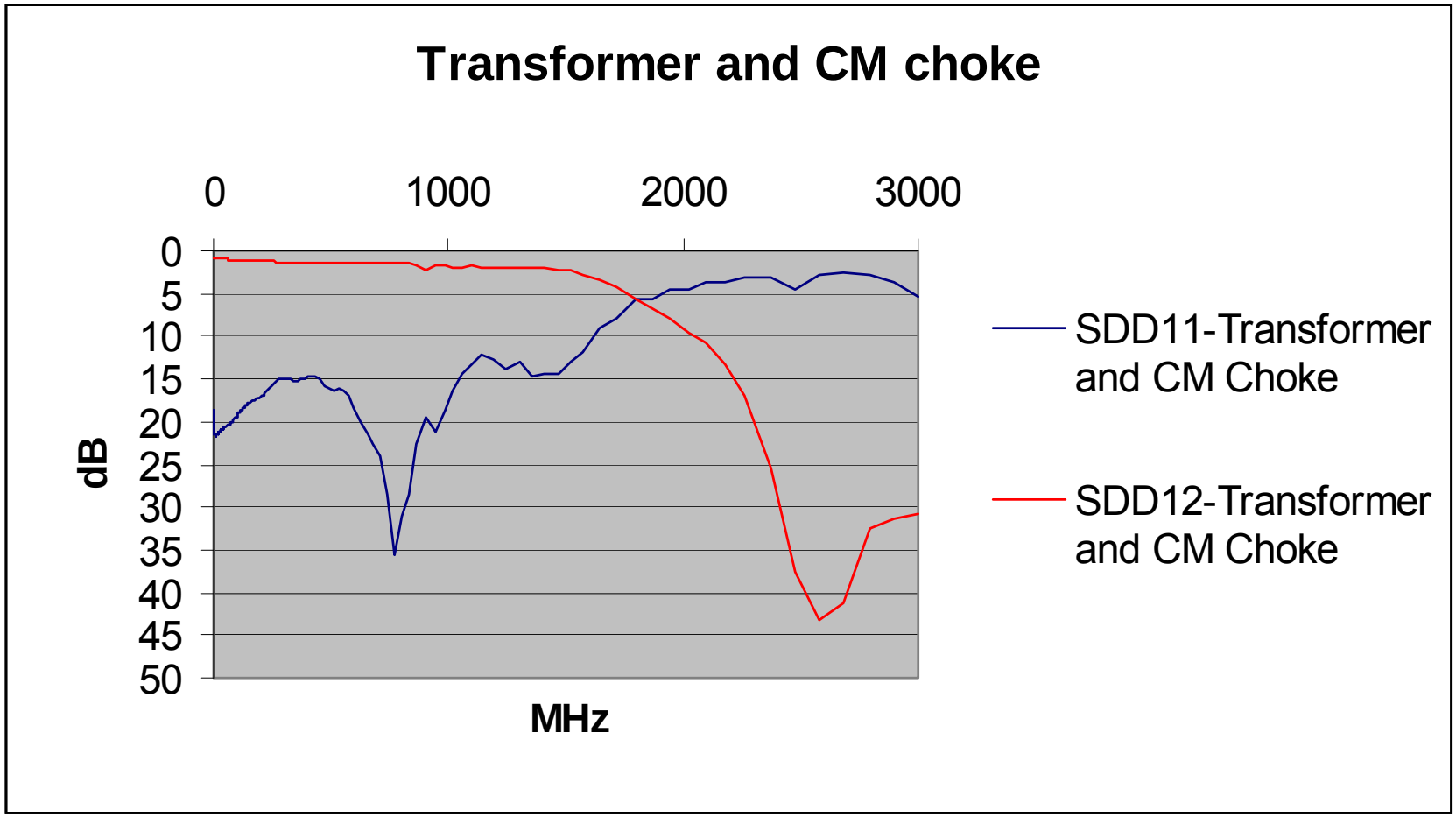


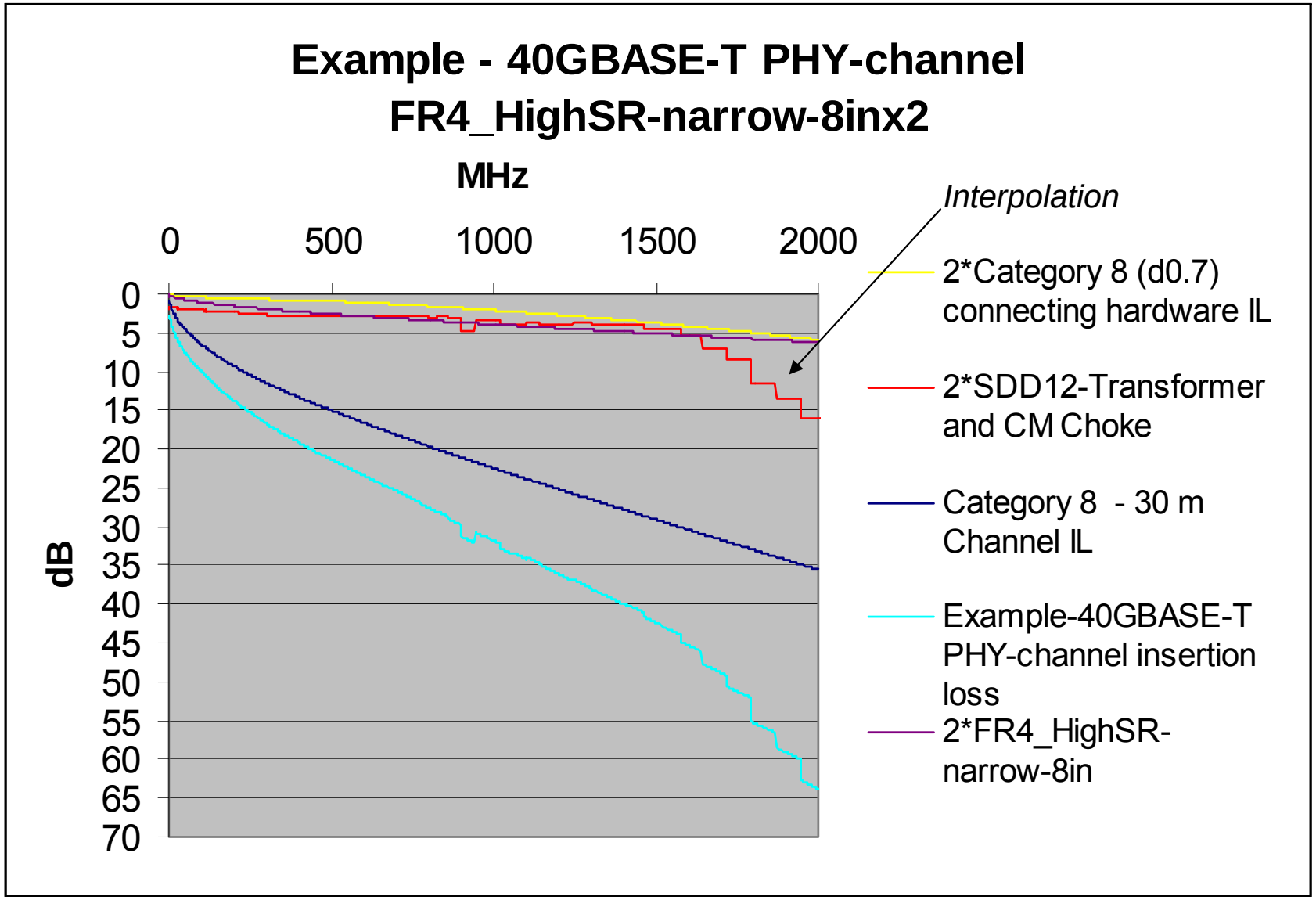
Not including magnetic's

Transformer and CM choke



Source: http://www.ieee802.org/3/bq/public/channelmodeling/index.html
Pulse_NGBase-T_Magnetic.S4P Thuyen Dinh, Pulse Electronics

Example: 40GBASE-T PHY-channel insertion loss



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    - Host loss budget
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