

A Broad Market Potential Consideration for the Baseline Proposal

IEEE P802.3bq 40GBASE-T Task Force

David Chalupsky, Intel

Victoria, BC, Canada – 16-17 May, 2013

Channel (Reach) vs. PHY Complexity

- The topic of reach vs. PHY power and complexity is being enthusiastically explored by the Task Force and Study Group.
- Thank you!
- Suggestion for further investigation follows

A Likely Port Configuration

- The vast majority of Ethernet ports shipped in the BASE-T family have been capable of multiple speeds
 - 10/100BASE-T, 10/100/1000BASE-T ports
 - now 1000/10GBASE-T, or 100/1000/10GBASE-T
- It is likely that support for lower speeds will be a common product requirement for 40GBASE-T ports
 - 10G/40GBASE-T or 1000/10G/40GBASE-T ports
 - 2, 3 or more speeds supported

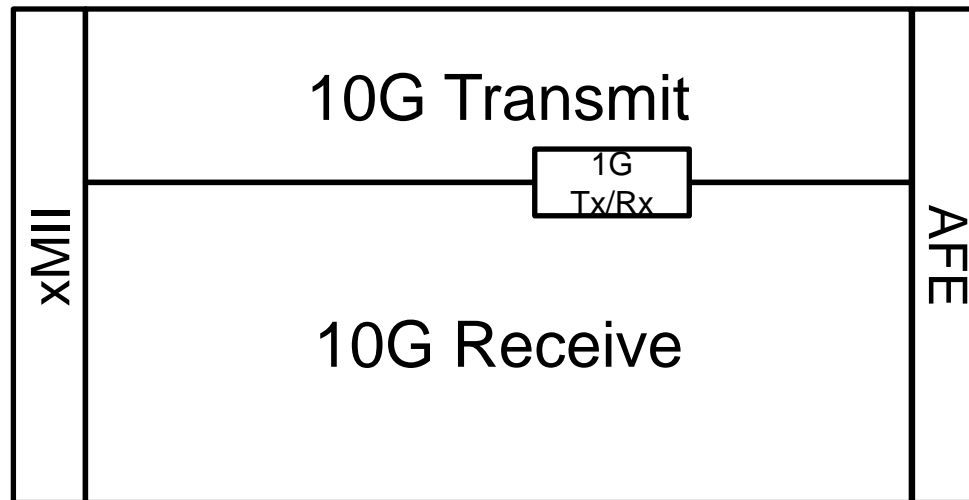
Considerations

- Definition of 40GBASE-T PHY should not break support for some lower speeds
 - Compatible MDI, autonegotiation, cabling
- Cost: Die size matters too!
- Optimizing for power alone, for 40GBASE-T implementation alone, may lead to an impractical implementation of multi-speed ports

10GBASE-T PHY Layout

In a typical 10GBASE-T PHY device

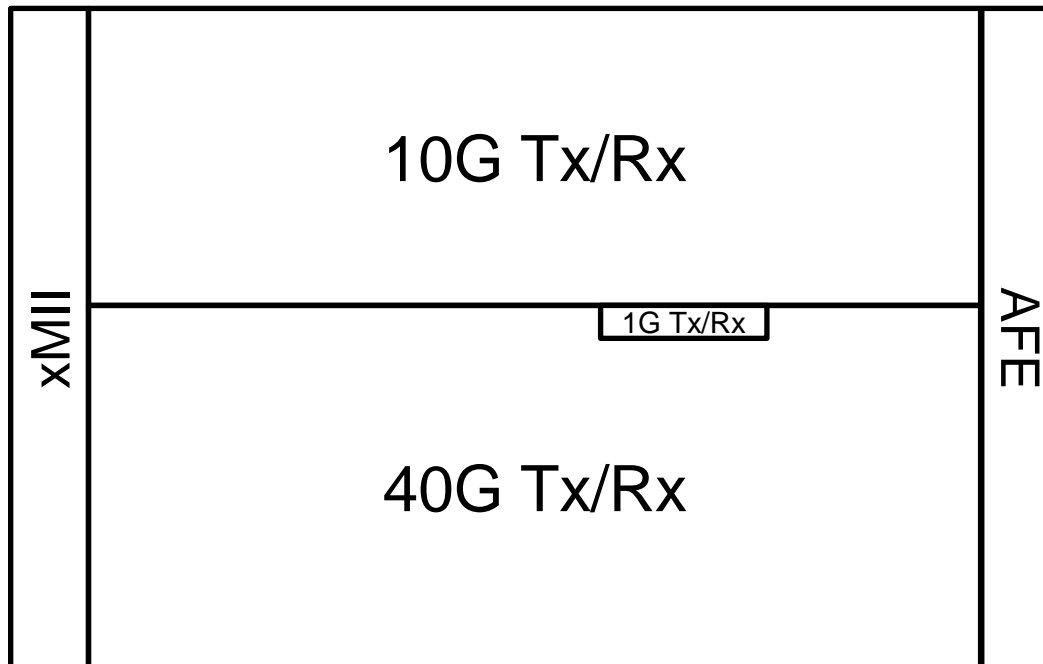
- Little reuse between the 10G and lower speed blocks
- 10G content dwarfs the lower speed content
 - Which at least means that the 1G support is not adding significant cost to a 10G PHY... trying to look at the bright side.



Artist's conception, not to scale.

What We Want to Avoid

- Avoid: Little reuse between the 10G and 40G blocks
- If die size doubles from 10G to 10/40G, broad market potential and economic feasibility may be compromised.



Artist's conception, not to scale.

Information Requested

- As we develop the ingredients of our baseline proposal
 - Bandwidth, modulation, coding, FEC, power, etc.
- Consider the trade-offs between
 - An optimal 40G-only product vs.
 - An optimal multi-speed product.

Thank You!