# Impact of Board-level Considerations on 40GBASE-T Channels

Contribution to IEEE 802.3bq 40G-BASE-T Task Force
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# Overview

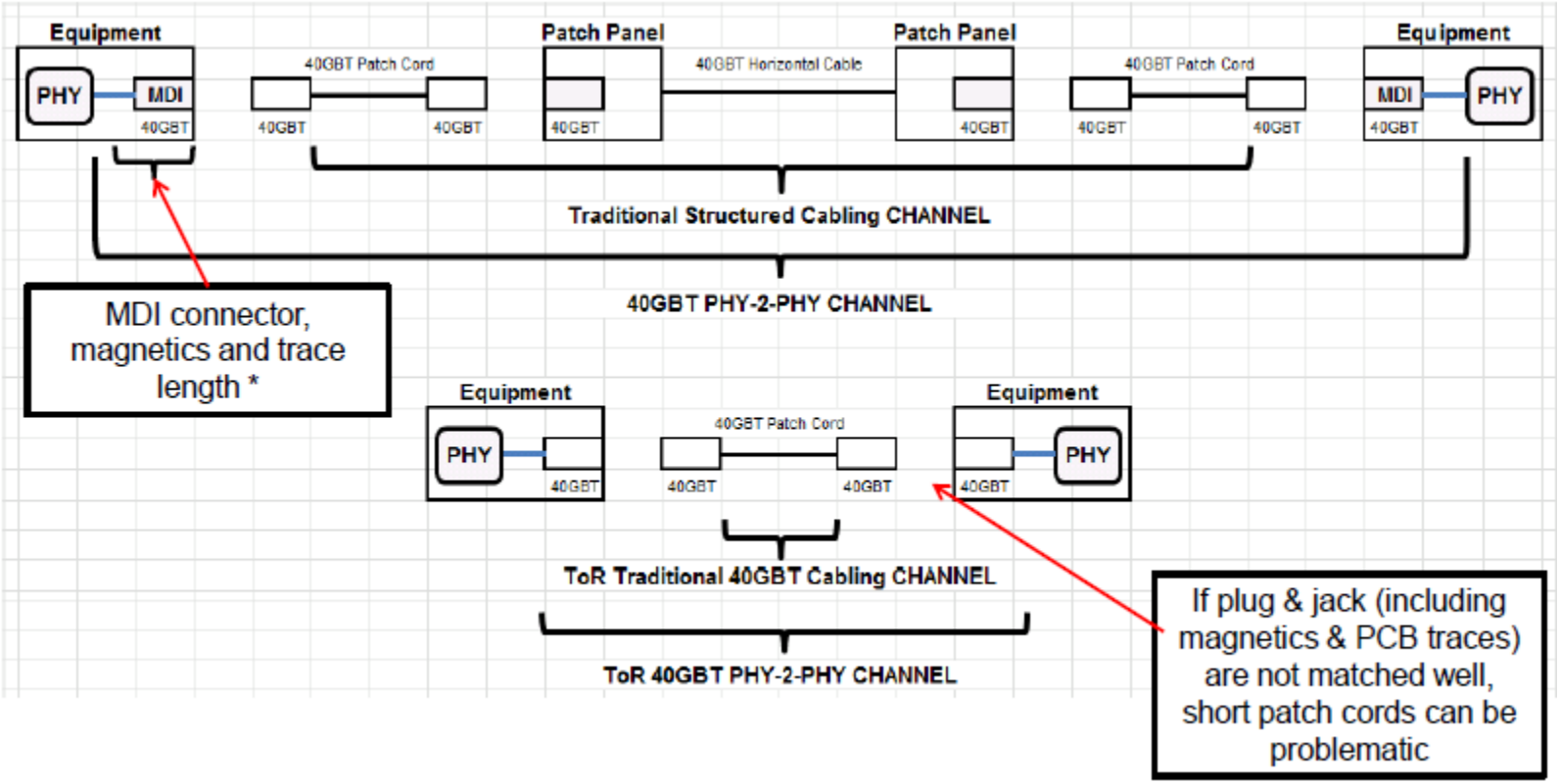
- Motivation
- Model
- Examples
- Next Steps

# Motivation

- Previous PHY modeling has relied only on cabling channel measurements or specifications to predict impacts of impairments on PHY design complexity and power
- Experience with 10GBASE-T has shown magnetics and PCB impairment levels have been equally challenging to design performance
- Expensive PCB layouts are inconsistent with BASE-T's 5 criteria responses
- Other 802.3 projects have extended channel modeling to include reference points on the PCB

# Motivation

(from nordin_01_0912)



# Motivation

- PHY power and complexity modeling
  - Power depends on the echo seen at the PHY pins, not at the MDI plane.
  - Hybrid circuits (active & passive) reduce echo behind the MDI but on-board echo and crosstalk remain
  - Low cost magnetics, connectors and PCB processes necessary for BASE-T economics drive these specs

# Model for Standardization

- Specify normative channel at the MDI
- Include informative modeling of on-board components
  - Chip pins -> PCB -> magnetics -> MDI
- Model for informative board-level reference points already exists in 802.3

# Model for Standardization: from Backplane Ethernet

**71.6.1 Link block diagram**

For purposes of system conformance, the PMD sublayer is standardized at test points TP1 and TP4 as shown in Figure 71–1. The transmitter and receiver blocks include all off-chip components associated with the respective block. For example, external AC-coupling capacitors, if required, are to be included in the receiver block.

The electrical path from the transmitter block to TP1, and from TP4 to the receiver block, will affect link performance and the measured values of electrical parameters used to verify conformance to this specification. It is therefore recommended that this path be carefully designed.

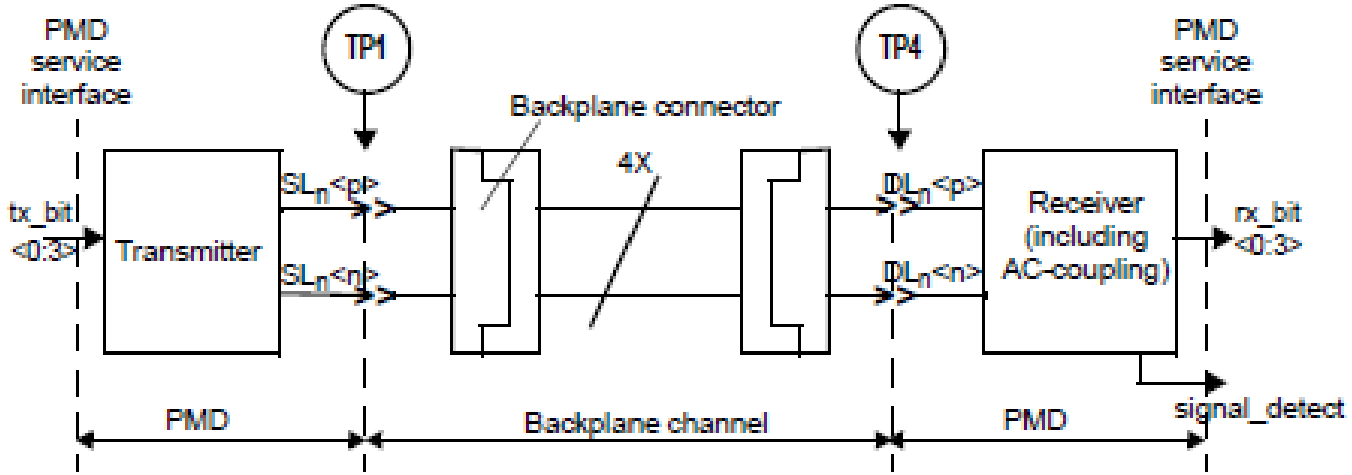



Figure 71–1—Link block diagram

# Model for Standardization: Test Fixtures

**71.7.1.1 Test fixtures**

The test fixture of Figure 71–2, or its functional equivalent, is required for measuring the transmitter specifications described in 71.7.1, with the exception of return loss.

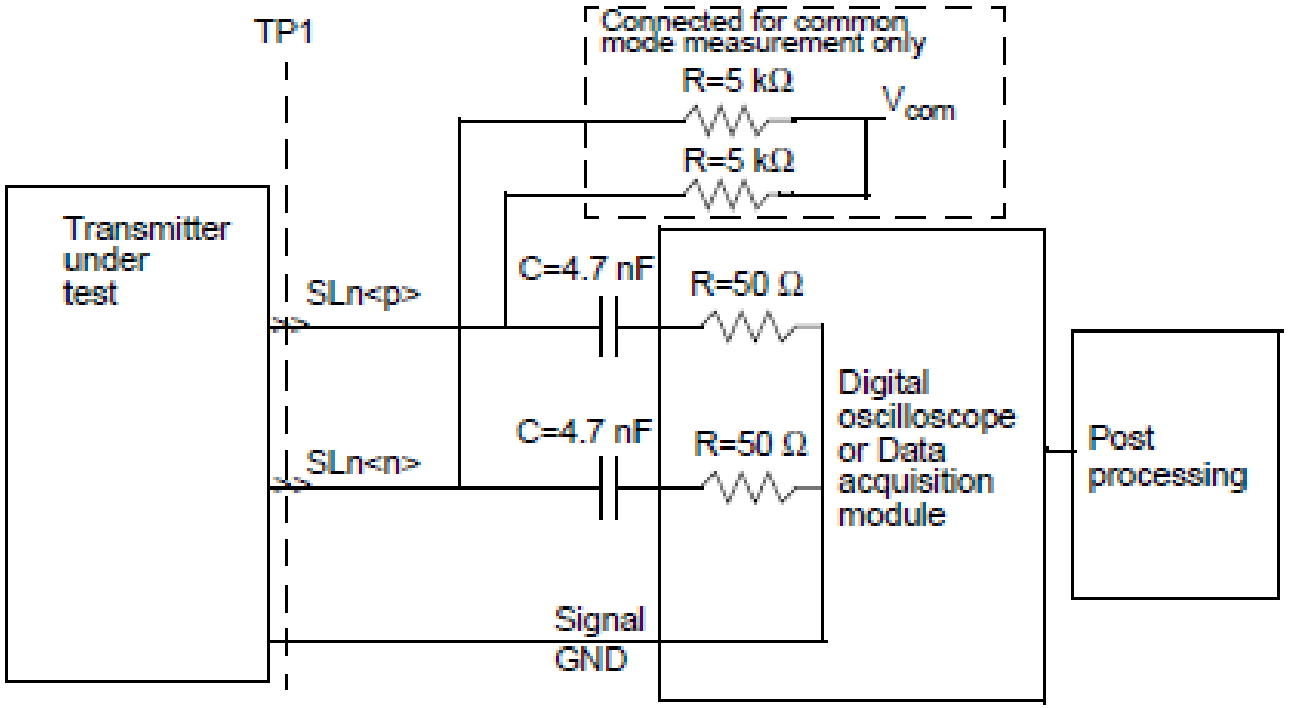
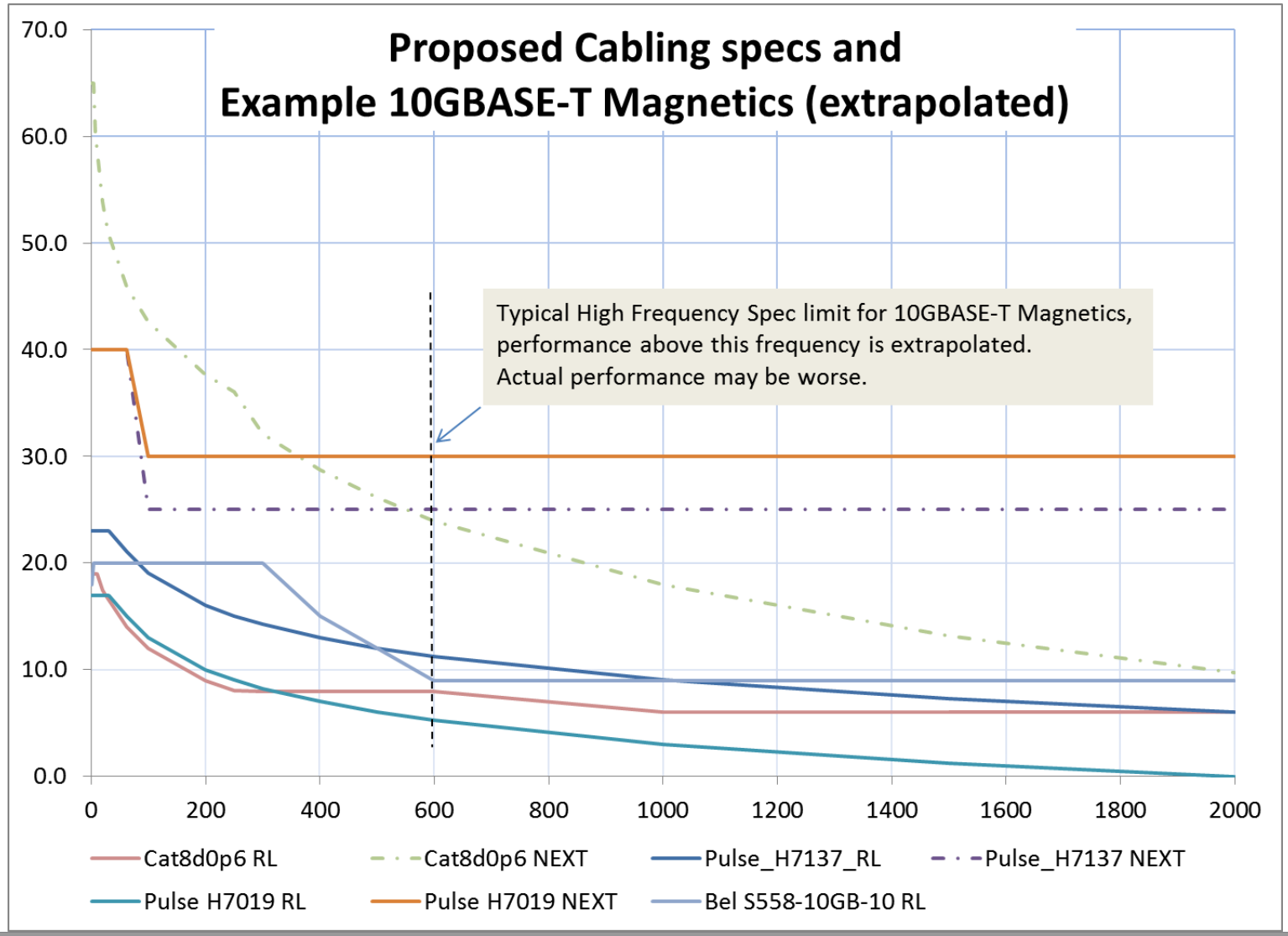



Figure 71–2—Transmit test fixture for 10GBASE-KX4

# Examples of Impacts

- Without informative board-level model, new channels could appear much better than they were
- Challenges to deployment could go unmet
  - Magnetics/MDI development contributed to 10GBASE-T delays
- Cost optimization & broad acceptance makes it important to match specifications of channels to board-level components

# Example: Magnetics vs. Cabling



# Issues: PCB Stackup in Servers

- BASE-T doesn't drive the motherboard design considerations, to be successful, it must live with them!
- Impedance mismatches can be significant
  - Use of standard FR4 materials
  - Use of no tighter than +/- 10% tolerances
    - Better tolerances may be possible, but are inconsistent with low-cost broad market
  - For servers, compatibility with other high-performance interconnects, e.g., PCI-e, drives <100ohm nominal traces, increasing the maximum mismatch
- Noise on long traces
  - Often > 8", and traverses SDRAM and PCI-e

# Next Steps

- Determine granularity of reference model for on-board components
  - One or more test points?
- Determine feasible straw man specifications for components
  - Contribution driven
- Incorporate into a combined channel model for PHY performance modeling