Delay Constraints in 40GBASE-T

IEEE 802.3: 40G-BASE-T Task Force

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Outlines

- Review delay constraints (i.e., latency) limit for 10GBASE-T
  - 25600BT- (i.e., 8 LDPC frames, 2.56us)
    - Defined in Clause 55.11
    - The sum of TX & RX path delays (PHY Medium delay not included)
  - Main latency
    - Frequency domain Echo/Next cancellation (in a typical 10GBase-T transceiver) and LDPC decoder
- 40GBASE-T
  - Analysis on latency numbers for 40GBASE-T transceivers

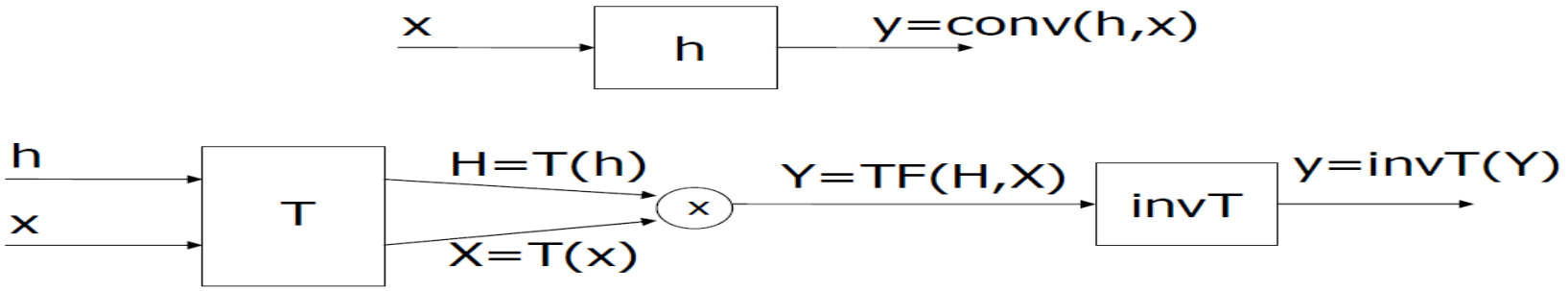
Latency at 10GBASE-T transceivers

- The main latencies are shown in ns and LDPC frames
- The latency is traded off for power at ENX and some blocks

Blocks	Latency (ns)	LDPC frames	Note
LDPC decoder	> 640ns	> 2	RX
Echo/Next canceller	600 ~ 1200ns	2~ 4	TX or RX side Frequency domain Filtering Trade off power and latency
Others: FIFO, pipelines and PCS etc.	mid~high 100's ns	1 ~2	TX and RX
Total latency	2000~2500ns	6 ~ 8	marginal meets 8 frame latency limit

Why DFT FIR for Filtering with long taps ?

DFT FIR:



	ECHO	NEXT	FEXT	FF EQ	**Total FIR**
FIR length	500	300	100	80	
BlockSize or net samples	524	724	156	176	
FFTsize	1024	1024	256	256	
log2N	10	10	8	8	
Real operations/sample for FIR	**500**	**300**	**100**	**80**	**7120**
Total operations/block for DFT FIR (4*(N/2)log_2(N)*2+4*N)/2	22528	22528	4608	4608	
Real operations/sample for FFT	**43**	**31**	**30**	**26**	**1005**
Approx Savings	**91%**	**90%**	**70%**	**67%**	**86%**
Gain	**11x**	**10x**	**3x**	**3x**	**7x**

*Reference: http://www.ieee802.org/3/10GBT/public/sep03/kasturia_1_0903.pdf

Echo/NEXT cancellation – DFT FIR

- At 10GbaseT:
  - Total XTALK cancellation tap number at a 10G port: ~1000*4 (echo)+300*12 (Next)+128*12 (Fext) ~ 9000 taps!!!
  - With 90% power savings compared to time domain FIRs
    - Real implementations vary with selection of block size of FIRs, bit width of calculations, possible custom cells and taps turn off …
  - Time domain FIR implementation is not an favorable option considering power consumptions.
- Cons for DFT FIR:
  - Higher latency
  - Algorithm latency (algorithm – FFT size/2) and implementation latency
  - Selection of smaller size FFT will reduce algorithm delay and increase flexibility , but will increase complexity

Extrapolation of Latency at 40GBASE-T

- 30meter cable with 4x of symbol rate:
  - Echo Taps requirements = $N_{10GBASE\text{-}T}$*30/100*4 ~ (1.2*$N_{10GBASE\text{-}T}$)
  - Still preferable to do ENX in DFT FIRs

Latency at 40GBASE-T transceiver

Blocks	10GBASE-T (LDPC frames)	40GBASE-T (LDPC frames)
LDPC decoder	> 2	> 2*
Echo/Next canceller	2~ 4	2.4~ 4.8 Higher because of longer taps
Others: FIFO, pipelines and PCS etc.	1 ~2	1 ~2* (might be challenging)
Total latency	6 ~ 8	6 ~ 8*

* *65nm to 16nm may not hit 4X speed, more parallel architecture may increase latency.*

Conclusions:

- keep latency constraints not lower than 25600BT.
- Challenges to meet:
  - Echo will take longer
  - More parallelism will take longer
- Let the PHY venders to find the best trade off for power and latency under this constraints.

Thank you