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Delay Constraints in 40GBASE-T

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Goal

- **Balance market requirements and technical feasibility for delay in 40GBASE-T**

Supporters

- **Peter Wu, Marvell**
- **(your name here)**

Background – 10 G Market Reality

- **Latency is important in high-speed applications**
  - Specialized high-speed training
  - Multi-hop networking
- **10GBASE-T Delay constraint is 25600 bit times**
  - Clause 55.11 , the sum of Tx & Rx path delays
  - 25600 BT is 2.56 usec at 10Gb/s
    - Competition (BASE-R PCS + PMD or XAUI) was ~4000BT
- **This was perceived as much too high for performance conscious users (the early market)**
  - A barrier to adoption!

Competitive Situation at 40G

- **25600 BT is 640 nsec at 40Gb/sec**
  - Much more palatable… but still noticeable
- **Competition:**
  - 40G MAC, RS and MAC Control layers 16384 BT
  - 40GBASE-CR4 requires:
    - 40GBASE-R PCS + PMA 15360 BT
    - And 40GBASE-CR4 PMD 4096 BT
  - 40GBASE-CR4 = 19456BT
- **40GBASE-T parts may embed part of 40GBASE-R as an interface, making situation similar to 10G**

Delay Distribution at 10GBASE-T

- **10GBASE-T 25600 BT is driven by:**
  - 2 frames (3200BT each) PCS/LDPC framing latency
  - 19200 BT miscellaneous, largely signal processing pipelining or block transformations, and decoding iterations
    - Achievable since 90nm generation
    - Latency, power and area ALWAYS a trade off
    - Todays 10G improves latency, use up to 4X faster clocks
    - Highly dependent on architecture and granularity choices

Delay management in 40GBASE-T

- **40GBASE-T baseline uses same framing size**
  - PCS/LDPC framing latency the same: 6400BT (160nsec)
  - DSP parallelization block size similar to 10G (see Wu_3bq_01_0514)
- **40G Channel improves latency**
  - Sparse cancellation favors shorter time-blocks (langner_3bq_01_0114)
    - Makes smaller granularity more power efficient AND lowers latency
  - Improved implementation margin enables faster decoding
- **Process improvements improve delay time**
  - Some vendors today running <1.5usec latency at 10G
  - Result: <850nsec for signal processing at 10G today
- **Improvement required: 850nsec -> 480nsec, less than 2X**

Setting the Delay Spec

- **Allowing 'vendors to differentiate' doesn't work for delay**
  - Interoperability considerations
  - Marketing can't overcome specification in the standard
- **10GBASE-T learning:**
  - Once the delay spec is set, interoperability considerations lock it in despite technology improvements
- **Need to balance implementation and market, and go aggressively**

Proposal

- **Do not reduce delay below 25600BT**
- **Maintain 25600BT for 40GBASE-T delay**