Change rows in Table 45–210 as appropriate..

Table 45–210—EEE advertisement register (Register 7.60) bit definitions

Bit(s)	Name	Description	Clause reference; Next Page bit number	R/W[a]
7.60.9	~~Reserved~~40GBASE-T EEE	~~Value always 0, writes ignored~~1 = Advertise that the 40GBASE-T has EEE capability 0 = Do not advertise that the 40GBASE-T has EEE capability	~~113.6.1; U21~~	~~RO~~R/W

[a]R/W = Read/Write, RO = Read only

Insert new paragraph after 45.2.7.13.9 and re-number remaining clauses accordingly.

45.2.7.13.10 40GBASE-T EEE supported (7.60.9)

If the device supports EEE operation for 40GBASE-T as defined in 113.6.1, and EEE operation is desired, this bit shall be set to one.

Change rows in Table 45–211 as appropriate.

Table 45–211—EEE link partner ability (Register 7.61) bit definitions

Bit(s)	Name	Description	Clause reference; Next Page bit number	R/W[a]
7.61.9	~~Reserved~~	~~Value always 0, writes ignored~~1 = Link partner is advertising EEE capability for 40GBASE-T 0 = Link partner is not advertising EEE capability for 40GBASE-T	~~28.2.3.4.128; U3 / 113.6.1; U24~~	RO

[a]R/W = Read/Write, RO = Read only

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113.4.2.5.10; Infofield Octet 12 bit 7

Author: bmc Subject: Replacement Text Date: 5/12/2015 3:53:51 PM
113.4.2.5.10; Infofield Octet 12 bit 7

113. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, Physical Medium Dependent (PMD) sublayer, and baseband medium, type 40GBASE-T

113.1 Overview

The 40GBASE-T PHY is one of the 40 Gigabit Ethernet family of high-speed CSMA/CD network specifications. The 40GBASE-T Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), Physical Medium Dependent (PMD) and baseband medium specifications are intended for users who want 40 Gb/s performance over balanced twisted-pair structured cabling systems. 40GBASE-T signaling requires four pairs of balanced cabling, as specified in ISO/IEC 11801-1 Edition 3 and ANSI/TIA-568-C.2-1-201x Addendum 1: Specification for 100ohm Category Cabling with appropriate augmentation as specified in 113.7.

This clause defines the type 40GBASE-T PCS, 40GBASE-T PMA, type 40GBASE-T PMD sublayer, and type 40GBASE-T Medium Dependent Interface (MDI). Together, the PCS, PMA and the PMD sublayer define a 40GBASE-T Physical Layer (PHY). Functional, electrical, and mechanical specifications for the type 40GBASE-T PMA, PMD, and MDI are provided in this document. This clause also specifies the baseband medium used with 40GBASE-T. Management is specified in Clause 30.

This clause also specifies 40GBASE-T Low Power Idle (LPI) as part of Energy-Efficient Ethernet (EEE). This allows the PHY to enter a low power mode of operation during periods of low link utilization as described in Clause 78.

40GBASE-T PHYs may optionally support a fast retrain mechanism. Implementation of the fast retrain option is recommended. ~~Configurations wishing to disable fast retrain on the link may do so by advertising lack of support in Clause 28 AutoNegotiation, thus preventing the link partner from attempting fast retrain and potentially dropping the link.~~

113.1.1 Objectives

The objectives of 40GBASE-T are as follows:

a) Support full duplex operation only
b) Preserve the 802.3 / Ethernet frame format utilizing the 802.3 MAC
c) Preserve minimum and maximum frame size of the current IEEE 802.3 standard
d) Support a BER of less than or equal to 10^{-12} at the MAC/PLS service interface
e) Support Auto-Negotiation (Clause 28)
f) Support Energy-Efficient Ethernet (Clause 78)
g) Support local area networks using point-to-point links over structured cabling topologies, including directly connected link segments
h) Do not preclude meeting CISPR/FCC EMC requirements
i) Support a speed of 40 Gb/s at the MAC/PLS service interface
j) Define a link segment based upon copper media specified by ISO/IEC JTC1/SC25/WG3 and TIA TR42.7 meeting the following characteristics:
— 4-pair, balanced twisted-pair copper cabling
— up to 2 connectors
— up to at least 30 m
k) Define a single 40 Gb/s PHY supporting operation on the link segment

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Configurations wishing to disable fast retrain on the link may do so by advertising lack of support in register 7.32, thus preventing the link partner from attempting fast retrain and potentially dropping the link. See 45.2.7.10.

signal is followed by a wake signal, composed of LDPC frames containing only IDLE 512B/513B and 64B/65B blocks. After a short recovery time the normal operational mode is resumed.

In the receive direction the transition to the LPI mode is triggered when the PCS Receive function detects LPI control characters within received LDPC frames. This indicates that the link partner is about to enter the LPI transmit mode. Following these frames the link partner ceases transmission and begins quiet-refresh signaling. During the quiet time it is highly recommended that the local receiver power off circuits to reduce power consumption. Periodically the link partner transmits refresh frames that are used by the receiver to update adaptive coefficients and timing circuits. This quiet-refresh cycle continues until the link partner transmits the alert signal, initiating a transition back to the normal operational mode. The alert signal is detected in the PMA and signals that normal data frames will follow. The alert signal is followed by a wake signal that allows the local receiver time to prepare for the normal operational mode. The wake signal is composed of repeated IDLE 512B/513B and 64B/65B blocks. After a short recovery time the normal operational mode is resumed.

~~Support for the EEE capability is advertised during Auto Negotiation.~~ Transitions to and from the LPI transmit mode are controlled via XLGMII signaling. Transitions to and from the LPI receive mode are controlled by the link partner using sleep, alert, and wake signaling.

The PCS 64B/65B Transmit state diagram in Figure 113–17 and Figure 113–18 includes additional states for EEE. The PCS 64B/65B Receive state diagram in Figure 113–19 and Figure 113–20 includes additional states for EEE. The EEE Transmit state diagram is contained in the PCS Transmit function and is specified in Figure 113–21.

113.1.4 Signaling

40GBASE-T signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over each wire pair. The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<63:0> and TXC<7:0> to four-dimensional symbols in the transmit path.
c) Algorithmic mapping from the received four-dimensional signals on the MDI port to RXD<63:0> and RXC<7:0> on the XLGMII interface.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling both directions on any pair combination.
f) No correlation between symbol streams on pairs BI_DA, BI_DB, BI_DC, and BI_DD.
g) Block framing and other control signals.
h) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
i) Ability to automatically detect and correct for pair swapping and crossover connections.
j) Ability to automatically detect and correct for incorrect polarity in the connections.
k) Ability to automatically correct for differential delay variations across the wire-pairs.
l) Ability to support refresh, quiet and alert signaling during LPI operation.

The PHY operates in two modes—normal mode or training mode. In normal mode, PCS generates a continuous stream of four-dimensional symbols that are transmitted via the PMA at one of eight power levels. In training mode, the PCS is directed to generate only PAM2 symbols for transmission by the PMA, which enable the receiver at the other end to train until it is ready to operate in normal mode. (See the PCS reference diagram in 113.2.)

PHYs may also support the EEE capability as described in 113.1.3.3. Transitions to the LPI mode are supported after reaching normal mode.

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Support for the EEE capability is advertised in the Infofield (Octect 12 bit 7) during the PMA_PBO_Exch state.

Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Message Field	SNR Margin	Reser-ved	Transition Counter	~~Reser-ved~~	Vendor Specific	CRC16
4 octets	3 octets	1 octet	4 bits	2 bits	10 bits	2 octets	2 octets	2 octets

Figure 113–24—InfoField transition counter format

Start of Frame Delimiter 0xBBA70000	3 Transmitter Settings	Message Field	SNR Margin	Coefficient Exchange	Coefficient Field	CRC16
4 octets	3 octets	1 octet	4 bits	1.5 octets	4 octets	2 octets

Figure 113–25—InfoField coefficient exchange format

Start of Frame Delimiter 0xBBA70000	3 Transmit-ter Settings	Message Field	SNR Margin	Reserved	~~LPI Dis-able Time~~	Vendor Specific	CRC16
4 octets	3 octets	1 octet	4 bits	1.5 octets	2 octets	2 octets	2 octets

Figure 113–26—InfoField not transition counter and not coefficient exchange format

113.4.2.5.1 Infofield notation

For all the InfoField notation below, Reserved<bit location> represents any unused values and shall be set to zero and ignored by the link partner. For all PBO InfoField values below, the PBO<6:4> are unsigned 3-bit values 000, 001, 010, 011, 100, 101, 110, and 111 shall indicate power backoffs of 0 dB, 2 dB, 4 dB, 6 dB, 8 dB, 10 dB, 12 dB, and 14 dB respectively. The InfoField is transmitted following the notation described in 113.3.2.2.3 where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Oct1 is sent first).

113.4.2.5.2 Start of Frame Delimiter

The start of Frame Delimiter consist of 4 octets [Oct1<7:0>, Oct2<7:0>, Oct3<7:0>, Oct4<7:0>] and shall use the hexadecimal value 0xBBA70000. 0xBB corresponds to Oct1<7:0> and so forth.

113.4.2.5.3 Current transmitter settings

Current transmitter setting (1 octet). Represented by the octet Oct5{Valid<7>, PBO<6:4>, Reserved<3:0>} and shown in Figure 113–27. Used to announce the current fixed PBO setting during PMA_Training_Init_M, PMA_Training_Init_S and PMA_PBO_Exch, and the current programmable PBO setting during PMA_Coeff_Exch. For every other state this octet is set to zero and ignored by the link

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Reserved / Ability

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Reserved / Ability

0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110 shall indicate the decision point SNR margin values of –1.5, –1, –0.5, 0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5 dB respectively. The value 0001 shall indicate a margin of –2 dB or less, and the value 1111 shall indicate 5 dB or more. Finally the value 0000 shall indicate that the SNR margin value is unknown.

113.4.2.5.8 Transition counter

Transition counter (10 bits). Represented by the 1.25 octets [Oct9<1:0>, Oct10<7:0>]. When configured as Transition counter (Coeff_exchange<2>=0 and a transition is announced to PMA_Coeff_Exch, PMA_Fine_Adjust or PCS_Test) this field is used as a 10 bit counter that counts the number of remaining frames until the next transition (PMA_Coeff_Exch, PMA_Fine_Adjust, PCS_Test).

113.4.2.5.9 Coefficient exchange handshake

Coefficient exchange handshake (12 bits). Represented by the 1.5 octets [Oct9<3:0>, Oct10<7:0>]. If Coeff_exchange<2>=1, this field is configured as a Coefficient exchange handshake and is used as a handshake control channel during programmable THP coefficient exchange. The details of the coefficient exchange are described in 113.4.2.5.14.

~~113.4.2.5.10 Reserved Fields~~

~~All InfoField fields denoted Reserved in Figure 113–24, Figure 113–25, and Figure 113–26 are reserved for future use. This includes octets Oct11 and Oct12 when Coeff_exchange<2>=0, Oct9<3:2> when transition counter is announced and [Oct9<3:0>, Oct10<7:0>] when no transition is announced and no coefficients are exchanged.~~

113.4.2.5.11 Vendor-specific field

If Coeff_exchange<2>=0 octets, Oct13 and Oct14 are vendor-specific fields. If during Auto-Negotiation both transceivers agree on the use of the two vendor-specific octets, they may be used as a PHY communication channel; otherwise they are set to zero and ignored by the link partner. Represented by the 2 octets [Oct13<7:0>, Oct14<7:0>].

113.4.2.5.12 Coefficient Field

Coefficient Field (4 octets). Represented by the octets [Oct11<7:0>, Oct12<7:0>, Oct13<7:0>, Oct14<7:0>]. When Coeff_exchange<2>=1, this field is used to exchange programmable THP coefficients. It transmits four 8-bit THP coefficients out of the total of 64 (16 coefficients over each of the 4 pairs). The order is pair A, coefficients 0:3, followed by coefficients 4:7, followed by 8:11 and 12:15. For all cases the first coefficient (indices 0, 4, 8 and 12) is mapped to Oct11, the second coefficient (indices 1, 5, 9, 13) is mapped to Oct12 and so on. The same coefficient order is followed to transmit the coefficients for pair B, followed by pair C, and finally pair D. The details of the coefficient exchange are described in 113.4.2.5.14.

113.4.2.5.13 CRC16

CRC16 (2 octets). Shall implement the CRC16 polynomial $(x+1)(x^{15}+x+1)$ of the previous 10 octets, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, Oct10<7:0>, Oct11<7:0>, Oct12<7:0>, Oct13<7:0>, and Oct14<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 113–28. In Figure 113–28 the 16 delay elements S0,..., S15, shall be initialized to zero. Afterwards Oct5 through Oct14 are used to compute the CRC16 with the switch connected, which is setting CRCgen in Figure 113–28. After all the 10 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

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113.4.2.5.10 Ability Field
Ability field (1 octet). Represented by the octet Oct12(EEE Ability<7>, THP Bypass Request<6>,Fast Retrain<5>, Reserved<4:0>). Used to advertise the abilities of the PHY during the PMA_PBO_Exch state when Message<7:6> = 01.
For every other state, this octet is set to zero and ignored by the link partner. The Ability bits are defined as follows:
Oct12<4:0> = Reserved
Oct12<5> = Fast Retrain
0 = Fast Retrain not supported
1 = Fast Retrain supported
Oct12<6> = THP Bypass Request in PMA_Coeff_Exchstate
0 = Local device requests link partner not to bypass THP during fast retrain
1 = Local device requests link partner to bypass THP during fast retrain
Oct12<7> = EEE Ability
0 = EEE not supported
1 = EEE supported

113.4.2.5.11 Reserved
All InfoField fields denoted Reserved in Figure 113–24, Figure 113–25, and Figure 113–26 are reserved for future use. This includes octets Oct11 and Oct12 when Coeff_exchange<2>=0 and Message<7:6>~= 01, Oct9<3:2> when transition counter is announced and [Oct9<3:0>, Oct10<7:0>] when no transition is announced and no coefficients are exchanged.

While in states PMA_Training_Init_S, PMA_PBO_Exch, or PMA_Coeff_Exch, whenever a SLAVE operating in loop timing mode loses the MASTER timing reference (for example, after transmit power level transitions) it sets timing_lock_OK=0, which is communicated to the link partner via the InfoField. Otherwise, timing_lock_OK is set to one.

In MASTER mode, PHY Control enters the PMA_PBO_Exch state after loc_SNR_margin=OK and in SLAVE mode PHY Control enters the PMA_PBO_Exch state after the loc_SNR_margin=OK and ~~minwait_timer expires. In the PMA_PBO_Exch state,~~ after the MASTER has computed the final desired programmable PBO level, it shall request a PBO change using the requested transmitter setting in the InfoField (octet 7). In SLAVE mode, after the MASTER has requested the desired PBO level, the SLAVE shall request a desired PBO level that is within two levels (within 4 dB) of the requested MASTER PBO level. Both MASTER and SLAVE shall use the lower of the two PBO levels (i.e., that providing the larger transmit power).

Following PBO exchange for both transceivers, each PHY shall announce the next PBO setting using the next transmitter setting (octet 6). Afterwards, each PHY announces a transition to the PMA_Coeff_Exch state using the trans_to_Coeff_Exch=1 and transition_count as described in 113.4.5.1. MASTER initiates the transition to PMA_Coeff_Exch count with the trans_to_Coeff_Exch=1 flag and a transition counter value of 2^9. The SLAVE responds prior to the MASTER transition counter reaching 2^6 by setting trans_to_Coeff_Exch=1 flag and a transition counter value matching the MASTER. The PMA frame after each transceiver transition_count reaches zero, the PHYs shall enter the PMA_Coeff_Exch state and enable the requested PBO. Therefore, both PHYs will enter the PMA_Coeff_Exch state within one PMA frame.

While both MASTER and SLAVE are in state PMA_Coeff_Exch, when either end has computed the programmable THP settings, the programmable THP coefficient exchange process can begin, using the 1.5 octet Coefficient exchange handshake and the 4 octet Coefficient Field as follows:

a) During PMA_Coeff_Exch each PHY begins a coefficient exchange by setting the Coeff_Exchange flag to 1 in the Message Field.
b) During coefficient exchange, the transition counter bits are used as the Coefficient Exchange Handshake
   1) Oct9{Reserved<3:0>}: unused
   2) Coefficient Pair Received, Oct10<7:6>: 01 for local transmitter pair A, 10 for B, 11 for C and 00 for D (default). This is the handshake to tell the remote unit the last coefficients received.
   3) Coefficient Group Received, Oct10<5:4>: 01 for coefficients 0:3, 10 for 4:7, 11 for 8:11 and 00 for 12:15 (default). This is the handshake to tell the remote unit the last coefficients received.
   4) Coefficient Pair Sent, Oct10<3:2>: 01 for remote transmitter pair A, 10 for B, 11 for C and 00 for D (default). This is the handshake to tell the remote unit the current coefficients being sent.
   5) Coefficient Group Sent, Oct10<1:0>: 01 for 0:3, 10 for 4:7, 11 for 8:11 and 00 for 12:15 (default). This is the handshake to tell the remote unit the current coefficients being sent.
c) The Coefficient Field is used to send 4 8-bit coefficients in each frame designated by the Coefficient Pair Sent and Coefficient Group Sent bits. The coefficient format is:
   1) 8 bits per coefficient. Use one octet per coefficient in twos complement notation
   2) Coefficient range is –2.0 to 1.984375 in steps of 0.015625
   3) The sign of the coefficients shall be consistent with Equation (113–6)
d) Each PHY begins the exchange by sending pair A coefficients 0:3 with Coefficient Pair Sent=01 and Coefficient Group Sent=01.
e) The remote unit acknowledges by setting Coefficient Pair Received=01 and Coefficient Group Received=01.
f) Following each acknowledgement, the PHY increments through the Coefficient Group and then Coefficient Pair settings until Coefficient Pair Sent=00 and Coefficient Group Sent=00 and Coefficient Pair Received=00 and Coefficient Group Received=00. At this time, coefficient exchange is done and both PHYs set Coeff_Exchange=0.

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**minwait_timer expires. In the PMA_PBO_Exch state while Infofield Message<7:6> = 01, the PHY advertises EEE and Fast Retrain capability in octet 12 of the Infofield. When both the local device and remote device advertise EEE capability then EEE is supported. When both the local device and remote device advertise Fast Retrain capability then Fast Retrain is supported.
In the PMA_PBO_Exch state,**

113.4.2.5.15 Fast retrain function

PHYs that support the fast retrain capability shall implement the fast retrain state diagram shown in Figure 113–34. PHYs may request a fast retrain by setting the variable loc_fr_req to TRUE. This causes the transmission of an easily-detected link failure signal specified in 113.4.2.2.2. ~~After completing the link failure signal the PHY shall transition to the PMA_Coeff_Exch state, keep its THP turned on with its previously exchanged coefficients, and send PAM2 signaling within a time period equivalent to 9 LDPC frame periods.~~

After the detection of the link failure signal, a PHY shall transition to the PMA_Coeff_Exch state and respond with PAM2 signaling within a time period equivalent to 9 LDPC frame periods after receiving the link failure signal.

The PAM2 symbols are generated using the PMA sidestream scrambler polynomials shown in Figure 113–14. The training sequence without periodic re-initialization described in 113.3.4 shall be used during fast retraining, with the scramblers free-running from PCS Reset. If scrambler re-initialization is used for normal training, it shall be disabled and the scramblers shall begin free-running when the PHY Control state diagram enters the PCS_Test state and the variable fr_active is FALSE.

Note that reliable traffic on the transmitter may be interrupted when the local receiver requests a fast retrain.

Following the link failure signal, the two link partners transition back to the PMA_Coeff_Exch state and follow the training procedure described in 113.4.2.5.14, with the exception that the initial infofield countdown values are reduced as indicated in Figure 113–30 and Figure 113–31.

To ensure interoperability the training times in Table 113–13 should be observed during the fast retrain.

Table 113–13—Recommended fast retrain sequence timing

State	Recommended maximum time (ms)
PMA_Coeff_Exch state	20
PMA_Fine_Adjust state	10

113.4.2.6 Link Monitor function

Link Monitor determines the status of the underlying receive channel and communicates it via the variable link_status. Failure of the underlying receive channel typically causes the PMA's clients to suspend normal operation.

The Link Monitor function shall comply with the state diagram of Figure 113–32.

Upon power on, reset, or release from power down, the Auto-Negotiation algorithm sets link_control=SCAN_FOR_CARRIER and, during this period, sends fast link pulses to signal its presence to a remote station. If the presence of a remote station is sensed through reception of fast link pulses, the Auto-Negotiation algorithm sets link_control=DISABLE and exchanges Auto-Negotiation information with the remote station. During this period, link_status=FAIL is asserted. If the presence of a remote 40GBASE-T station is established, the Auto-Negotiation algorithm permits full operation by setting link_control=ENABLE. As soon as reliable transmission is achieved, the variable link_status=OK is asserted, upon which further PHY operations can take place.

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After completing the link failure signal the PHY shall transition to the PMA_INIT_FR state followed immediately by the PMA_Coeff_Exch state. If the link partner requested THP bypass for fast retrain the PHY will bypass the THP (or set THP coefficients to zero). Otherwise the PHY will keep its THP turned on with its previously exchanged coefficients, and send PAM2 signaling within a time period equivalent to 9 LDPC frame periods.

Table 113–20—40GBASE-T Base and Next Pages bit assignments

Bit	Name	Description
U31:U26	Reserved, transmit as 0	
U25	~~40GBASE-T EEE~~ ~~(1 = Advertise EEE capability for 40GBASE-T~~ ~~0 = Do not advertise EEE capability for 40GBASE-T)~~	~~Defined in 45.2.7.13.10~~
U24	10GBASE-T EEE (1 = Advertise EEE capability for 10GBASE-T 0 = Do not advertise EEE capability for 10GBASE-T)	Defined in 45.2.7.13.4
U23	1000BASE-T EEE (1 = Advertise EEE capability for 1000BASE-T 0 = Do not advertise EEE capability for 1000BASE-T)	Defined in 45.2.7.13.5
U22	100BASE-TX EEE (1 = Advertise EEE capability for100BASE-TX 0 = Do not advertise EEE capability for 100BASE-TX)	Defined in 45.2.7.13.6
U21	40GBASE-T ability (1 = support of 40GBASE-T and 0 = no support)	Defined in 45.2.7.10.4
U20	LD PMA training reset request (1 = Local Device requests that Link Partner reset PMA training PRBS every frame 0 = Local Device requests that Link Partner run PMA training PRBS continuously)	Defined in 45.2.7.10.5
U19	Fast retrain ability (1 = Advertise PHY as supporting fast retrain, 0 = Advertise PHY as not supporting fast retrain)	Defined in 45.2.7.10.6
U18	PHY short reach mode (1 = PHY of Local Device is operating in short reach mode 0 = PHY of Local Device is operating in normal mode)	Defined in 45.2.1.63.2
U17	LD loop timing ability (1 = Advertise PHY as capable of loop timing (mandatory for 40GBASE-T) and 0 = do not advertise PHY as capable of loop timing)	Defined in 45.2.7.10.7
U16	10GBASE-T ability (1 = support of 10GBASE-T and 0 = no support)	Defined in 45.2.7.10.4
U15	1000BASE-T half duplex (1 = half duplex and 0 = no half duplex)	
U14	1000BASE-T full duplex (1 = full duplex and 0 = no full duplex)	
U13	Port type bit (1 = multiport device and 0 = single-port device)	Defined in 45.2.7.10.3
U12	40/10GBASE-T MASTER-SLAVE config value (1 = MASTER and 0 = SLAVE) This bit is ignored if 7.32.15 =0.	Defined in 45.2.7.10.1
U11	40/10GBASE-T MASTER-SLAVE manual config enable (1 = manual configuration enable) This bit is intended to be used for manual selection in a particular MASTER-SLAVE mode and is to be used in conjunction with bit 7.32.14.	Defined in 45.2.7.10.2
U10	MASTER-SLAVE seed Bit 10 (SB10) (MSB)	
U9	MASTER-SLAVE seed Bit 9 (SB9)	
U8	MASTER-SLAVE seed Bit 8 (SB8)	
U7	MASTER-SLAVE seed Bit 7 (SB7)	

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Reserved, transmit as 0