PHY Channel Model Updates

Mike Grimwood, Broadcom

IEEE P802.3bq 40GBASE-T Task Force

Dallas, Texas

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Supporters

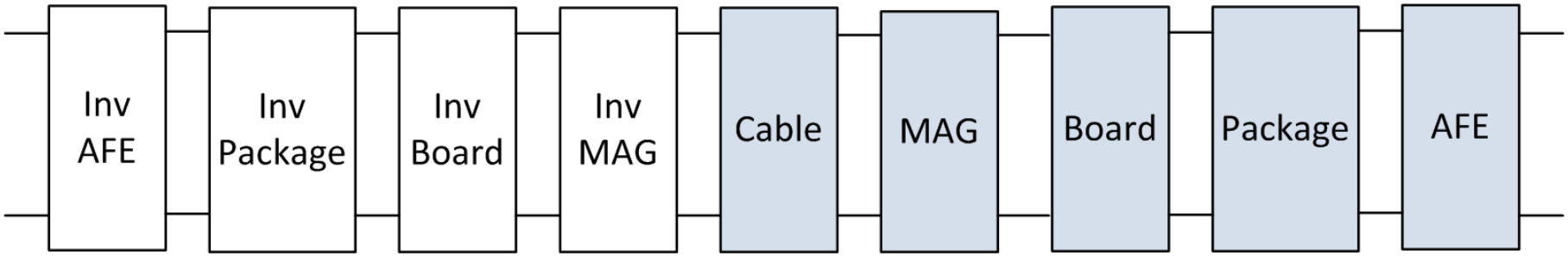
- George Zimmerman, CME Consulting and Commscope
- Thuyen Dinh, Pulse
- Victor Renteria, BelFuse
- Brian Buckmeier, BelFuse
- Wayne Larsen, Commscope

Overview

- Simulation results presented include S-parameter models that have been submitted to the IEEE 802.3bq related to the efforts of the PHY Channel ad hoc subcommittee.

- The simulation results show the estimated 40GBASE-T PHY ADC power Figure of Merit (FoM) as a function of symbol rate.

PHY-to-PHY Channel



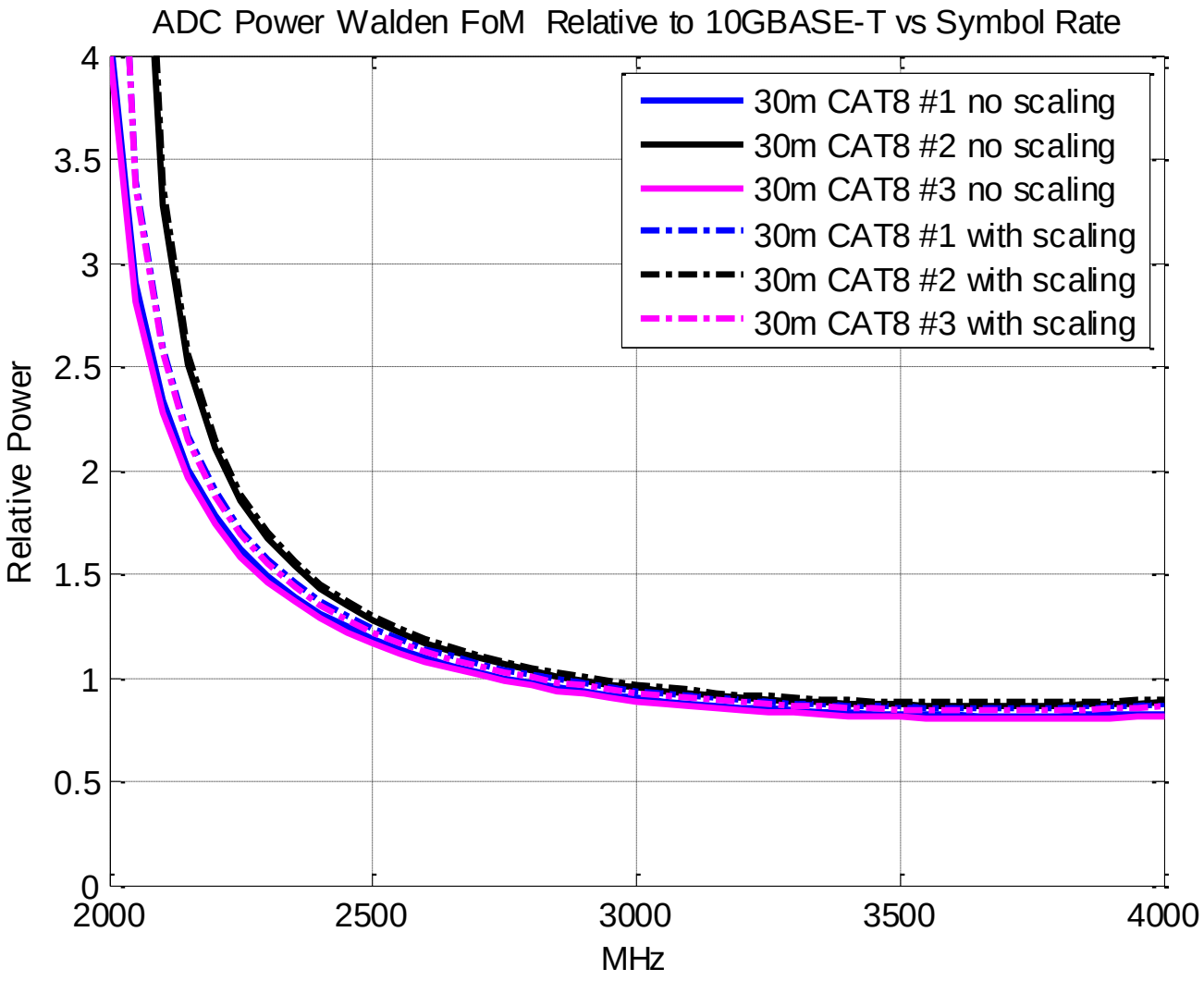
- Cascade S-parameters for composite channel.
- “Cable” is the two-connector channel model.
- “Mag” includes the transformer, common-mode chokes and MDI connector.
- “AFE” is the Analog Front End of the PHY and includes circuits between the package connections and the ADC and DAC.
- “Inv” indicates that the transpose S-parameter matrix should be used since the model may be asymmetric.

16-port PHY Models

- **Board:** 16-port S-parameters, 2 and 8 inch preliminary models from 10GBASE-T LOM. Models include a nominal 100 ohm characteristic impedance.
  - http://www.ieee802.org/3/bq/public/channeldata/10GBaseT_PCB_channel_models.zip
- **Isolation Path**: 16-port S-parameters from ICM measurements.
  - http://www.ieee802.org/3/bq/public/channeldata/BellCM2.S16P.zip
- **Cable:** 16-port S-parameters from preliminary Cat8 measurements of the two connector cable channel (Note that the reference to cable numbering in subsequent plots is randomized and therefore has no intended correspondence with the order of the following list).
  - http://www.ieee802.org/3/bq/public/channeldata/Panduit_Channel_30m_V1.s16p
  - http://www.ieee802.org/3/bq/public/channeldata/wlarsen_long_channel_3-24-3.s16p.rar
  - http://www.ieee802.org/3/bq/public/channeldata/Mike_Good3m24m3mCat8MDI.zip
- **Chip package and AFE models used are the same as described in grimwood_01a_0513_40GBT.pdf presented in May 2013.**

Note: For the analysis in this presentation, the Cable models are scaled by the methods presented in "larsen_3bq_channel_model_ad_hoc_Oct-16-13_limit_line_scaling.pdf" that was presented to the 802.3bq PHY Channel ad hoc. The Board and Isolation Path models are not scaled.

ADC Relative Power, ICM 2in/30mil PCB trace, 30m Cat8

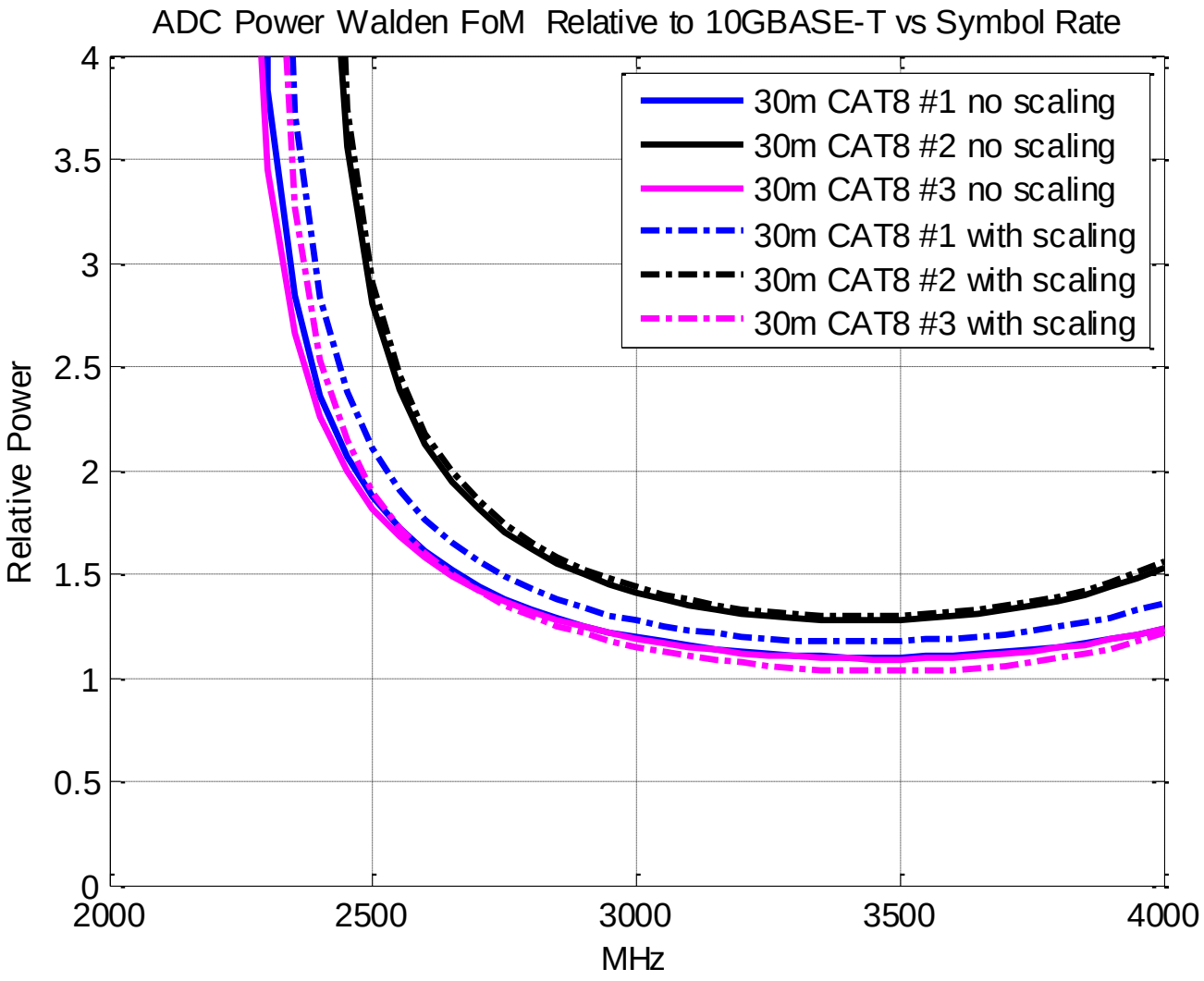


"no scaling" means that measurements are used as is.

"with scaling" means that measurements are scaled to CAT8 limits.

Note:
The arithmetic mean insertion loss from all four pairs used to compute the SNR and dynamic range.

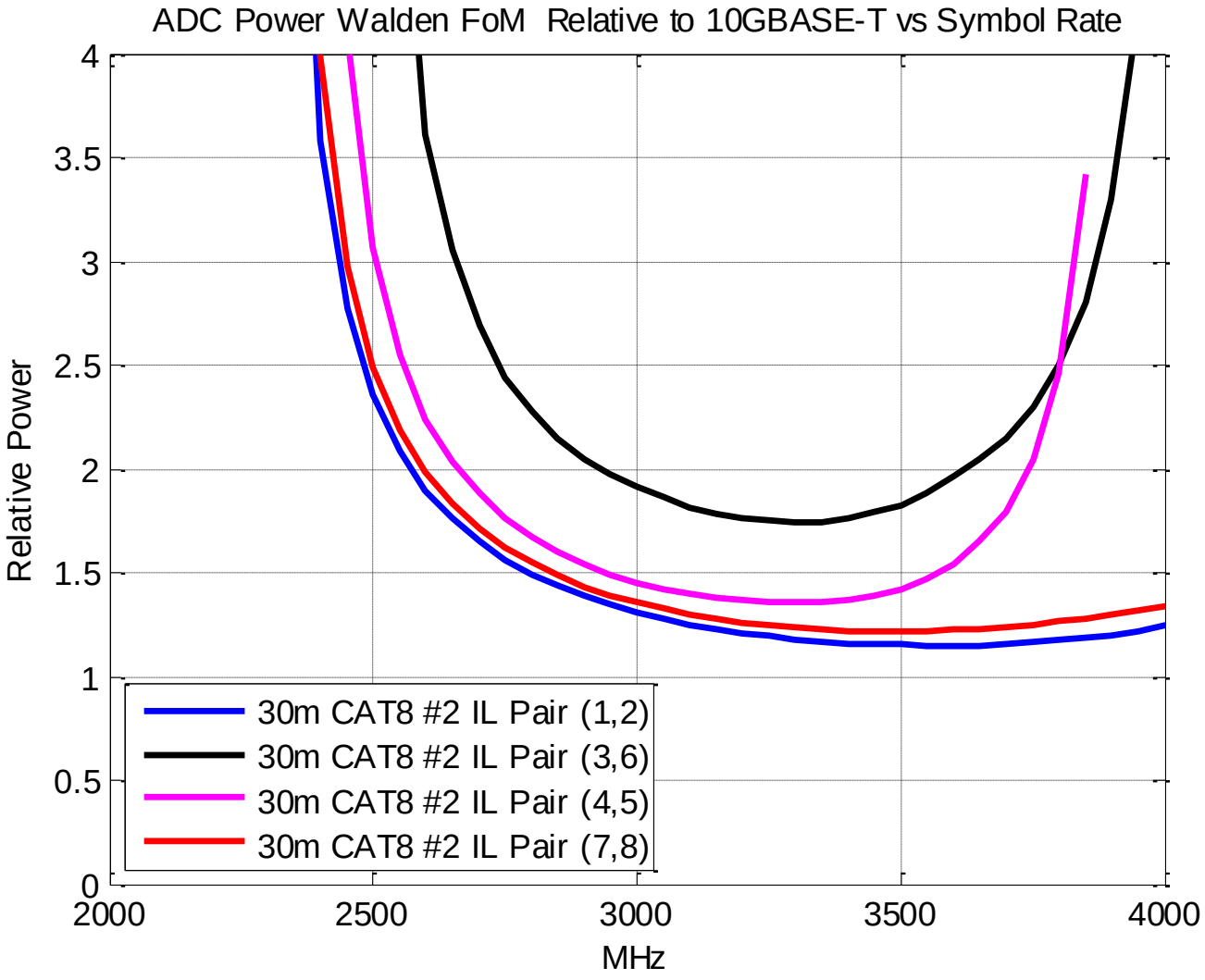
ADC Relative Power, ICM 8in/15mil PCB trace, 30m Cat8



Note:
The arithmetic mean insertion loss from all four pairs used to compute the SNR and dynamic range.

ADC Relative Power, ICM 8in/15mil PCB trace, 30m Cat8

Apply Designated Channel Insertion Loss



Note: The designated Pair end-to-end channel insertion loss is used to compute the SNR and dynamic range.

Conclusions and Next Steps

- Cable limit scaling doesn't have much impact on the ADC estimated power.

- PCB trace and ICM insertion loss variability both have significant impact.

- Next Steps:
  - Analyze channels in the time-domain to estimate digital power.
  - Finalize PCB and ICM budgets.

Thank you