Delay Constraint Considerations for 40GBASE-T

IEEE P802.3bq 40GBASE-T Task Force

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PHY Proposal ad hoc
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Overview

- Motivation:
  - Build consensus for the delay constraint (i.e., latency) limit for 40GBASE-T
- Status:
  - 802.3bq adopted 10GBASE-T modulation at 4x baud rate as baseline (with enhancements for consideration) in March'14
  - This *implies* a delay constraint value as well
  - Delay constraint carries very little text in the standard, but
    - has end user impact
    - Can be contentious!
    - Affects implementation options

802.3bq Task Force Motion #3

March 2014

- Move to adopt the proposal on page 6 of zimmerman_3bqah_1213.pdf, based on a 4X rate scaling of Clause 55 signaling, as a baseline PHY specification with future consideration of the proposed modifications listed on the same slide.

- M: George Zimmerman
- S: Peter Wu
- Y: 18 N:0 A:1
- (PASS) (Technical >=75%)

- Slide 6 of zimmerman_3bqah_1213.pdf

Baseline Proposal

- Baseline PHY proposal:
  - Use PCS, Framing and Line Coding from Clause 55
  - Increase symbol rate 4X to 3200 Mbaud
  - Drop transmit power to ~ 0 dBm at MDI
- Areas for improvement/consideration:
  - Backchannel for THP dynamic update?
  - Revised FEC to cover uncoded bits?
    - Multiple ways of doing this
  - Faster startup?
  - Negotiated patch-cord operational mode?
  - Remove PBO?

Extrapolating the Existing Limit

- 10GBASE-T Delay constraint is 25600 bit times
  - Clause 55.11
  - the sum of Tx & Rx path delays
- 25600 BT is 2.56 usec at 10Gb/s
  - This was perceived as much too high for performance conscious users. A barrier to adoption.
- 25600 BT is 640 nsec at 40Gb/sec
  - Much more palatable… but still noticeable
  - For comparison:

40G MAC, RS and MAC Control layers	16384 BT
40GBASE-R PCS + PMA	15360 BT
40GBASE-CR4 PMD	4096 BT

Recommendation

- 40GBASE-T Delay Constraint should be no more than 25600 BT
- Reducing this number could enhance the broad market potential of 40GBASE-T

Thank You!