# PHY Power Components and variations

#### G. Zimmerman CME Consulting, Inc. 12/5/13

IEEE 802.3bq 40GBASE-T Task Force – Dec 5 2013, PHY Proposal Ad Hoc

# Outline

- PHY Power Components
- Channel Variations under Consideration
- Fixed Power Components

   Elimination of Crosstalk Cancellers
- Analog Receiver Power vs. Bandwidth
- First-Order Overall Power
- Architecture Dependence need to study

# **PHY Power Components**

- Largely fixed with respect to channel parameters
  - TX Power
  - Equalizer
  - Echo Canceller
  - FEC coder/decoder
  - PCS framing
  - Interfaces & adaptation overhead
- Possibly variable
  - Analog front-end receiver power
  - NEXT cancellation
  - FEXT cancellation
- Savings in the above may result in tighter margins on the "fixed" components, increasing their power

#### **Channel Variations Under Consideration**

- Class 1 and Class 2 channels
  - Same: IL, ILD, Background noise (alien xtalk minimal)
  - Minor differences in RL, Connector RL
  - Substantial difference (10dB or more): NEXT, FEXT
- PCB 2 stackups, 2 lengths
  - 8 in PCB IL significant at 1.5GHz and above
  - 2 in PCB IL not a substantial impairment (use 8 in as limiting)
- MDI
  - Connectors
    - Same: IL, RL for both channels
  - Isolation
    - Magnetic loss, attributed to hand-wound variation
    - Tends to dominate over connector attributes
    - Possible packaging differences in connector/isolation for ICMs

## Fixed PHY Power Components

- FEC, PCS, Adaptation & Overhead
  - Primarily changes required SNR, robustness of solution
- Analog Transmit Power
  - Driven mainly by channel IL, non-40GBASE-T noise at the receiver and (weakly) by bandwidth
    - All parameters are equivalent for both cable classes
    - For PHY used bandwidths <= 1.7 GHz, MDI choices have little effect (losses look like <2dB, similar to other PHYs)</li>
  - PCB and Isolation choices will impact this
- Equalizer
  - Driven by channel IL & ILD (equivalent in both classes)
- Echo Canceller
  - Driven by line-side MDI Return Loss + Insertion Loss, channel Return Loss, Robustness to bending, and channel deformation
  - Equivalent for most choices

#### Power in Crosstalk Cancellers

- Analog power = 50% PHY power, typically
- DSP: 40% (overhead/leakage is 10%)
  - Maximizing NEXT/FEXT estimate below
    - Equalizer remains (~10% DSP power)
    - Echo canceller multipliers remain (~30% DSP power)
      - Including transform engines
    - FEC remains (20% DSP power)
    - NEXT/FEXT canceller power (<40% DSP power)
- RESULT: NEXT/FEXT cancellers ~16% PHY power, and often integrated with other functions

## Elimination of Crosstalk Cancellers

- Complete elimination of crosstalk
   cancellers is unlikely and problematic
- Analysis has shown case for elimination is marginal
- Cancellers make BASE-T robust
  - Enable reduced cost / complexity PCB design
  - Enable lower-cost MDI crosstalk
  - Protect against defects in cabling installation, patch connections

# Analog Receiver Power vs. Bandwidth (8 in PCB, from grimwood\_3bq\_01\_1113, slide 7)



- Minima at 3450 Mbaud PAM
  - 1725 MHz used
- Increases below 1600 MHz
  - ~20% by 1500 MHz
  - ~50% by 1350 MHz
  - ~100% by 1250 MHz
- Slightly less sensitive w/2in PCB
  - Digital power will favor lower bandwidths

## First-Order Overall Power

#### Components

- Analog Front End Power
  - 1.3-1.5x 10GBASE-T
  - Assume 50% component of 10GBASE-T PHY power
- DSP power:
  - Proportional to clock speed for same signal processing
  - Nominal 4X 10GBASE-T clock
  - Reduced complexity due to channel relaxation or less than 4X rate (0 to 25%?)
  - Assume 40% component of 10GBASE-T PHY power
- Overhead/Interface power
  - 10% component of 10GBASE-T
  - Assume 40G similar to 10GBASE-T

#### Based on 2Watts for 10GBASE-T PHY

- AFE:
  - 1W goes to 1.3W to 1.5W
  - Bandwidth dependence is reverse correlation to DSP power
- DSP:
  - 0.8W goes to 2.4W to 3.2W
    - Note 2.4W likely only goes with 1.5W analog
- Overhead/interface:
  - 0.2W remains 0.2W
- BALLPARK: 4.1W to 4.9W

CONCLUSION: We're in the range, but need to be careful!

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# Digital Architecture Dependence – Need to Study

- Digital power is vendor/architecture dependent
  - Will need PHY vendors to produce their own best estimates
- 2-connector topology and reduced channel IL requirement means optimal power architectures may be different from 10GBASE-T
- Receiver EQ/Cancellation is an area for vendor differentiation & innovation
  - Description is not needed for standardization
  - Confidence in hitting power requirements is needed

#### Conclusions

- Used bandwidth is viable between 1.4GHz and 1.7 GHz to control analog power
- Most digital power fixed or baud rate dependent
   Favors lower analog bandwidths
- Vendor-specific receiver architecture tradeoffs are likely more important than standards definition of modulation & coding
- We're close, but need to be careful!