Rudimentary Host PCB channel model for 10GBASE-T LOM

IEEE P802.3bq 40GBASE-T Task Force

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Overview

- Motivation:
  - Provide 10GBASE-T host trace models as a starting point for 40GBASE-T modeling
  - Future PCB design requirements could be more stringent, but this is representative of the current state of high volume server design
- Status:
  - Rudimentary s16p model available
  - 2” and 8” length
  - Several trace geometry variations

Model Development Path

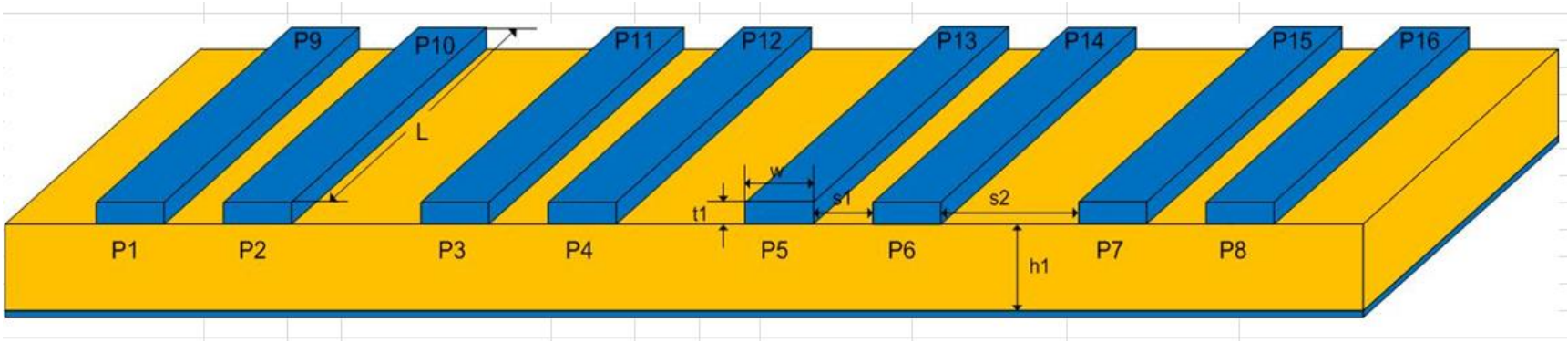
- PCB stack up and material representative of 2012 high volume server reference board
- Test channel boards built and measured
- Correlated to HSFF models
- Multiple variations modeled in HFSS

What Works, What Doesn't

- Model is a good representation of
  - Insertion loss
  - Crosstalk
- Model is optimistic on return loss
  - Only nominal impedance
  - No vias

- Future work
  - Impedance variation, 90ohm, 110ohm.
  - Include internal layer routing and vias

Stack Up



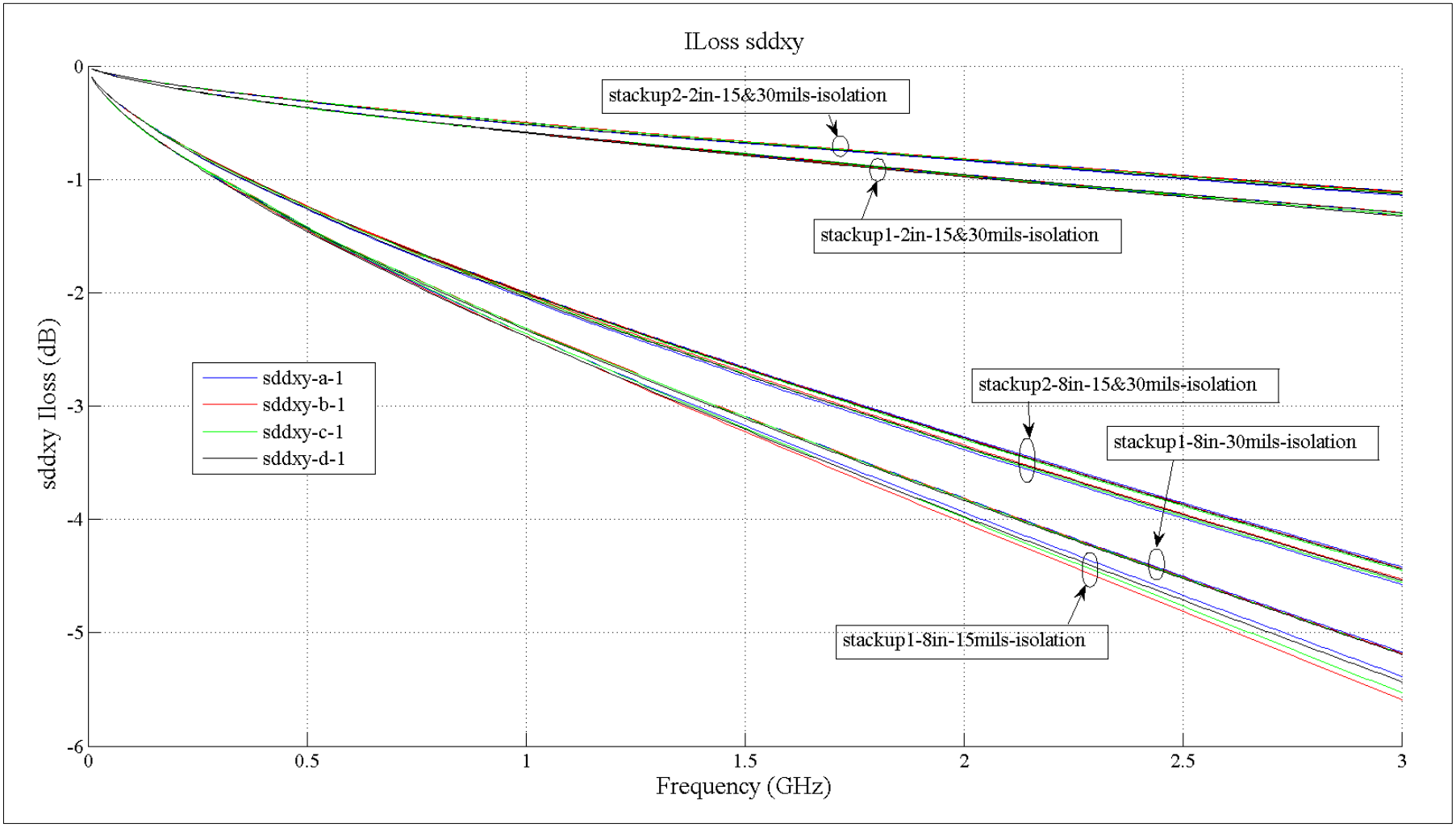
Stack-up 1			Stack-up 2	
w (mils)	4		w (mils)	4
h1 (mils)	2.7		h1 (mils)	3.5
s1 (mils)	11		s1 (mils)	5.1
t1 (mils)	2		t1 (mils)	2
dk	4.04		dk	4.04
df	0.02		df	0.02
s2 (mils)	varied		s2 (mils)	varied
calculated Zdiff (ohms)	99.6		calculated Zdiff (ohms)	100.2
calculated Zcomm (ohms)	27.3		calculated Zcomm (ohms)	34.1

Various configurations:

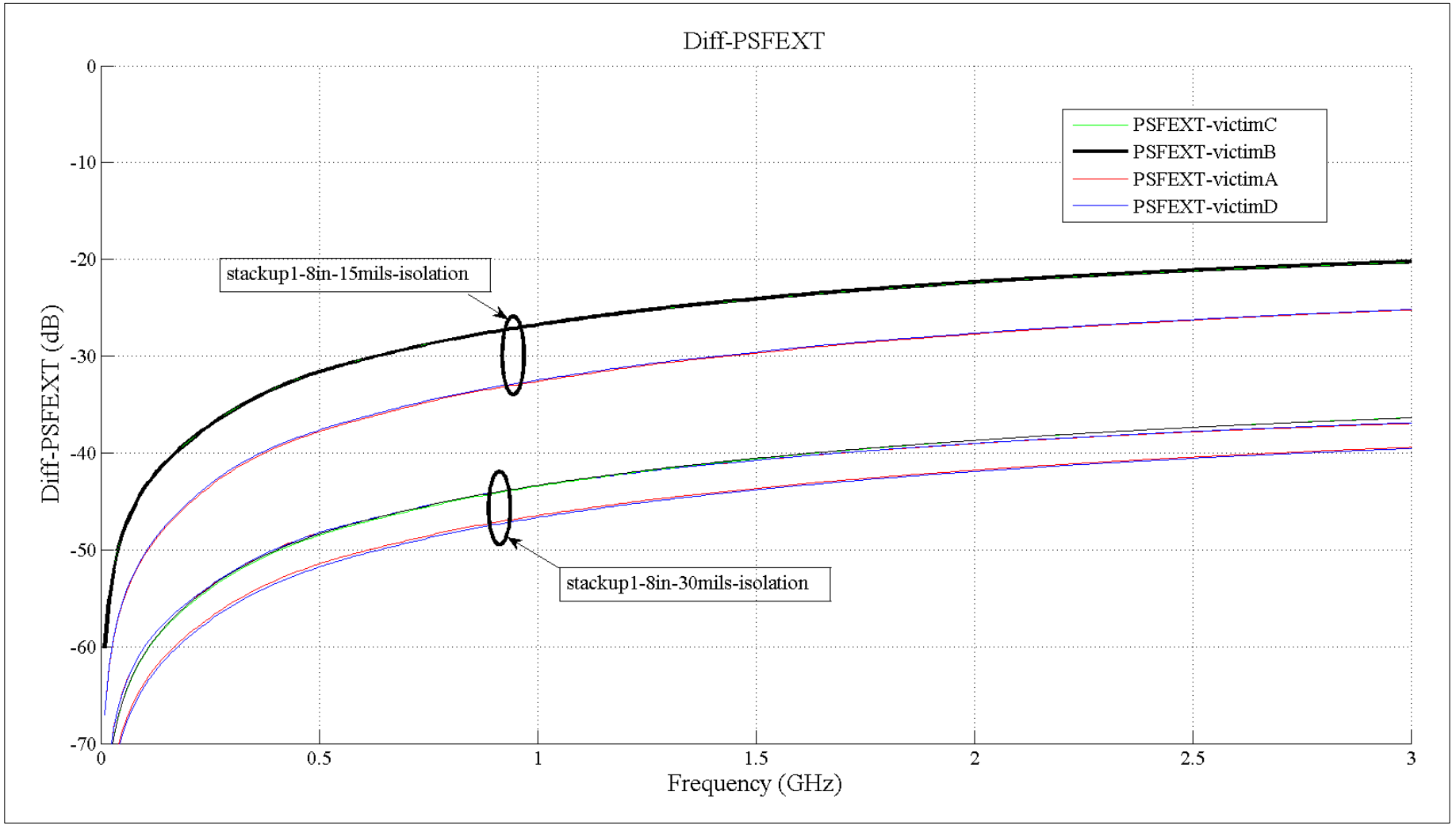
- 2” & 8” length
- Separation from 15-30mils

- 1um copper roughness

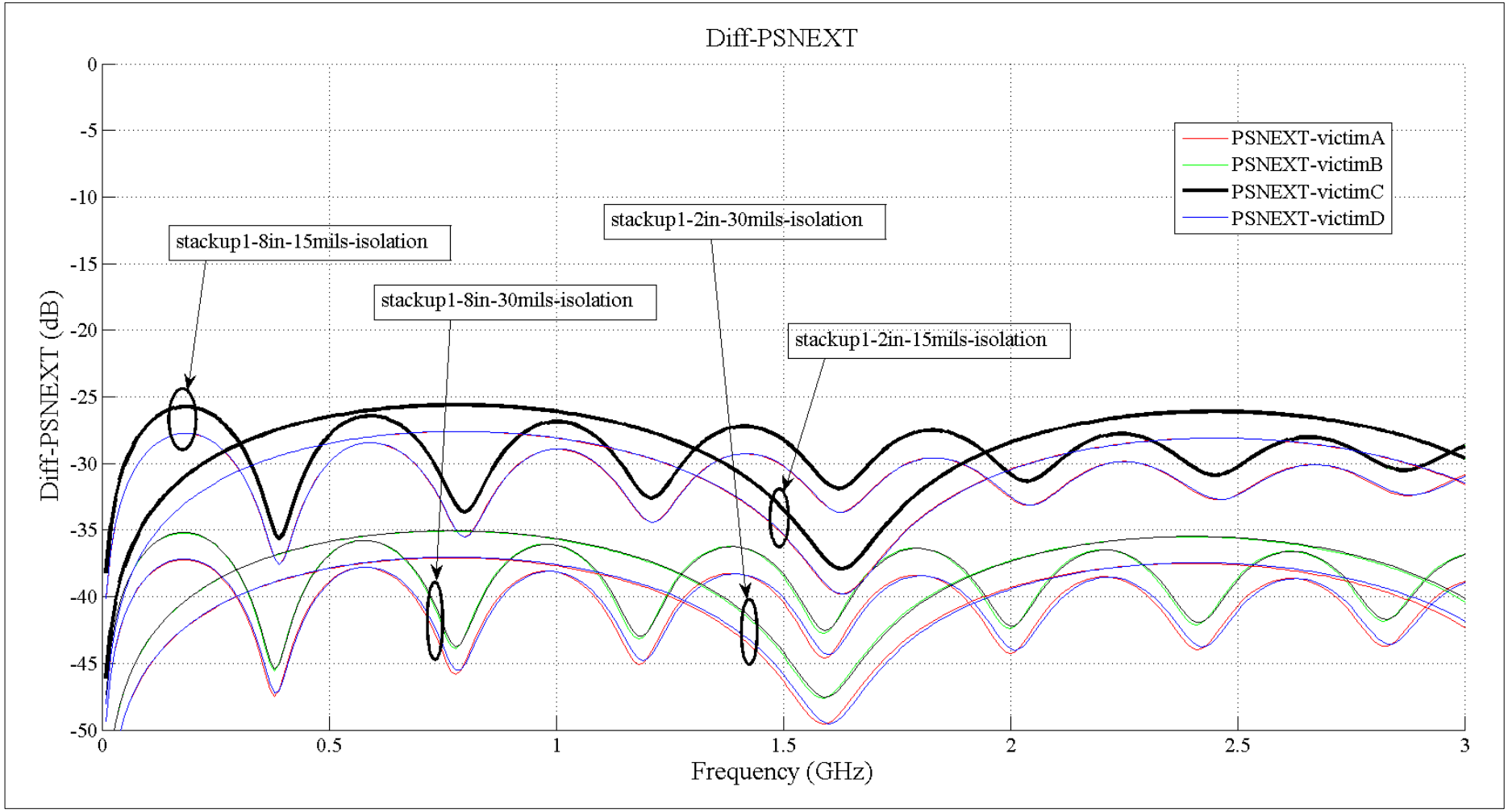
Insertion Loss



Power Sum Diff FEXT



Power Sum Diff NEXT



Data Summary

- Worst cases for this nominal impedance simulation set:
  - PSFEXT; stackup1_8in_15mils_isolation (chB,chC)
  - PSNEXT; stackup1_8&2in_15mils_isolation
  - Iloss; stackup1_8in_15mils_isolation

Thank You!