PHY Channel Model Updates

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Overview

- This presentation is a follow-up to “grimwood_01_0513_40GBT” presented in Victoria, BC in May 2013.

- Simulation results presented include S-parameter models that have been submitted to the IEEE 802.3bq related to the efforts of the PHY Channel ad hoc subcommittee.

- The simulation results show the estimated 40GBASE-T PHY ADC power Figure of Merit (FoM) as a function of symbol rate.

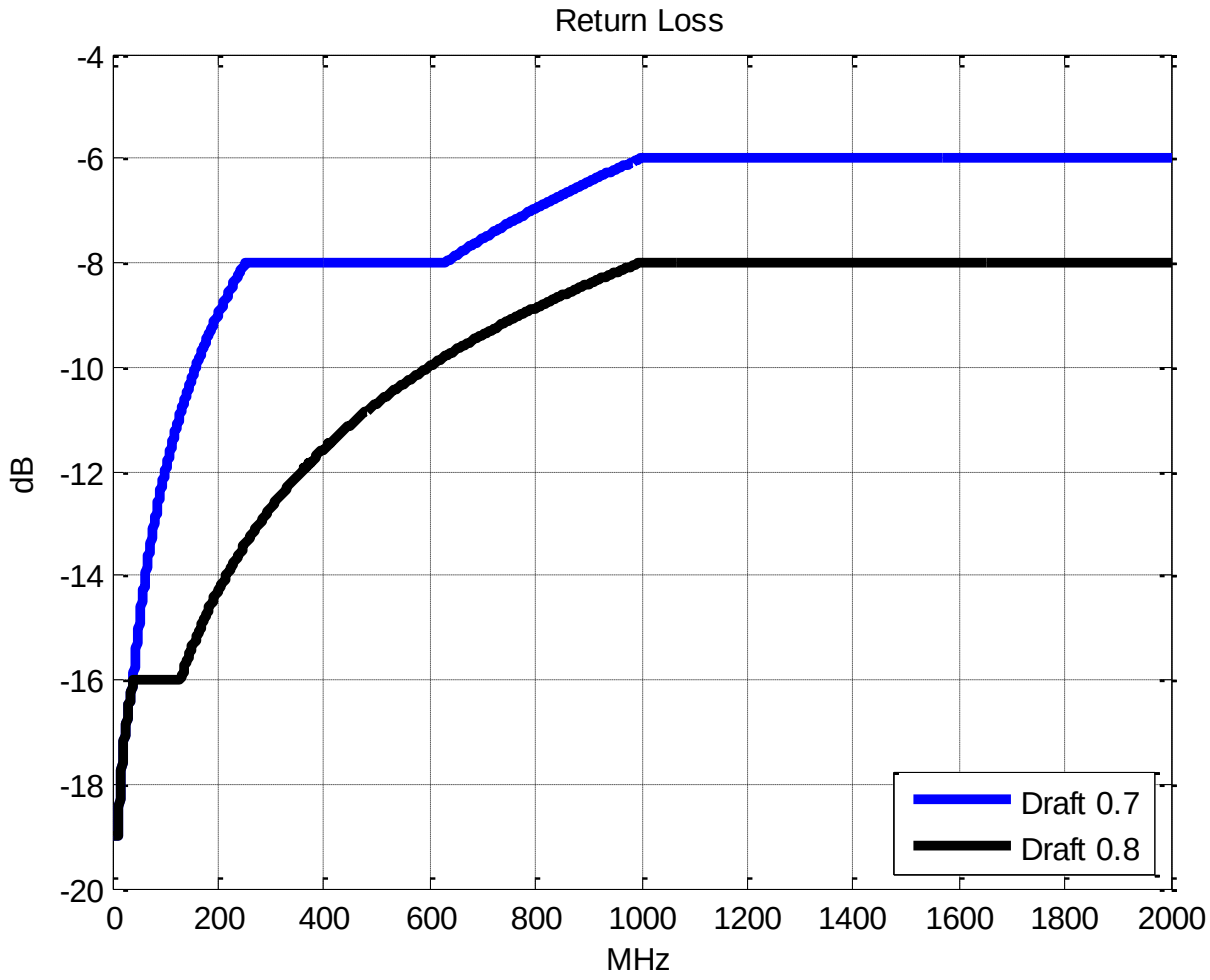
Updated PHY Models

- **Board:** 16-port S-parameters, 2 and 8 inch preliminary models from 10GBASE-T LOM. Models include a nominal 100 ohm characteristic impedance without variation.
  (1) http://www.ieee802.org/3/bq/public/channeldata/10GBaseT_PCB_channel_models.zip
- **Isolation Path**: 4-port S-parameters from preliminary transformer and choke measurements.
  (1) http://www.ieee802.org/3/bq/public/channelmodeling/Pulse_NGBase-T_Magnetics.S4P
- **Cable:** 16-port S-parameters from preliminary Cat8 measurements of the two connector cable channel.
  (1) http://www.ieee802.org/3/bq/public/channeldata/Panduit_Channel_30m_V1.s16p
  (2) http://www.ieee802.org/3/bq/public/channeldata/wlarsen_long_channel_3-24-3.s16p.rar
  (3) http://www.ieee802.org/3/bq/public/channeldata/wlarsen_short_channel_1-3-1.s16p.rar

Note 1: The TIA PN-568-C.2-1 Draft 0.8/0.9 CAT8 Return Loss limits are applied unless otherwise noted.

Note 2: For the analysis in this presentation, the Cable models are scaled such that the return loss, insertion loss and crosstalk magnitudes are at the TIA CAT8 limits at all frequencies. The Board and Isolation Path models are not scaled.

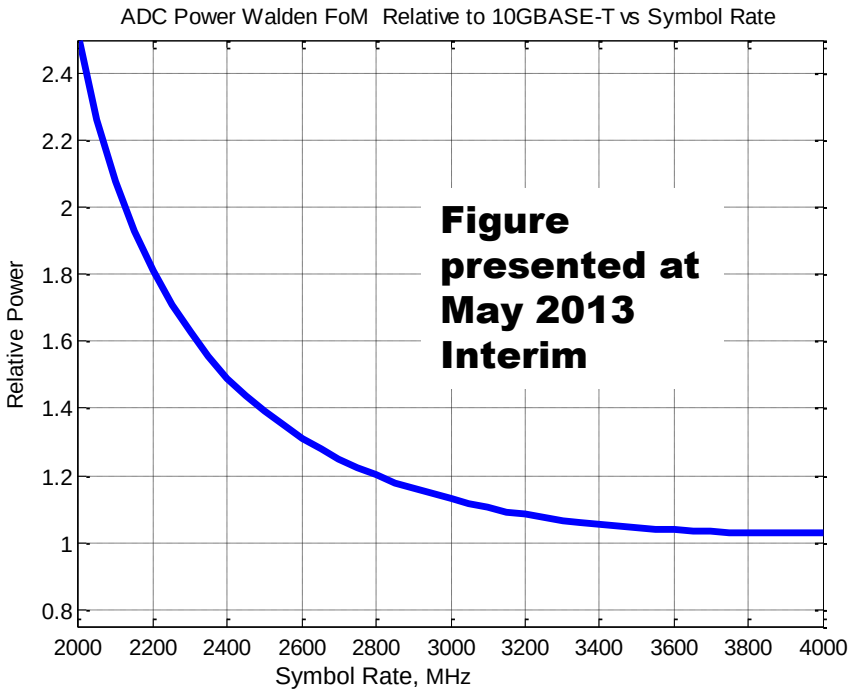
TIA PN-568-C.2-1 Draft Category 8 Channel Return Loss Limits



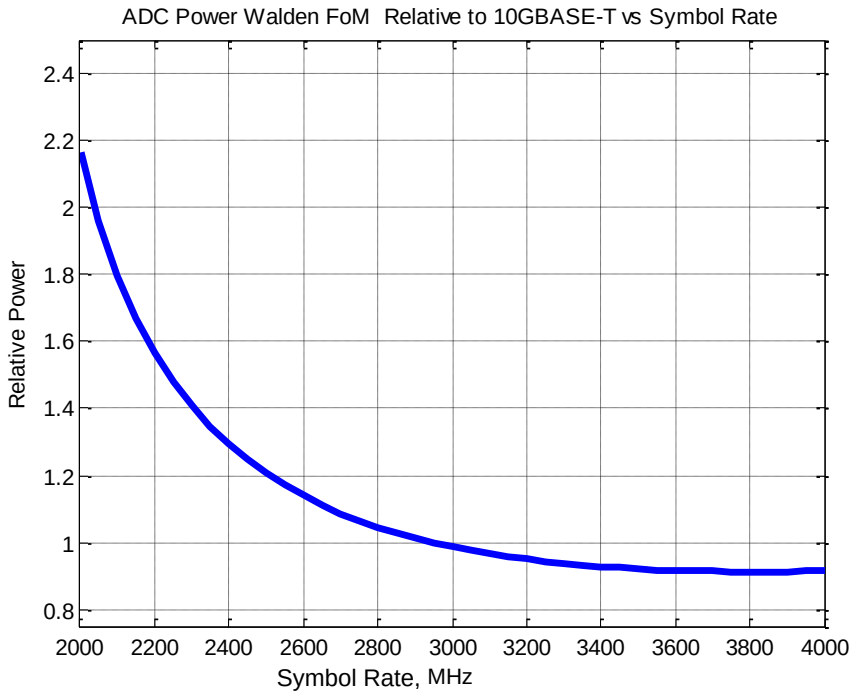
Note: Draft limits are noted as "TBD" and are therefore subject to change.

CAT8 Return Loss Spec Improvement ADC Power FoM vs Symbol Rate

With CAT8 Draft 0.7 RL



With CAT8 Draft 0.8/0.9 RL

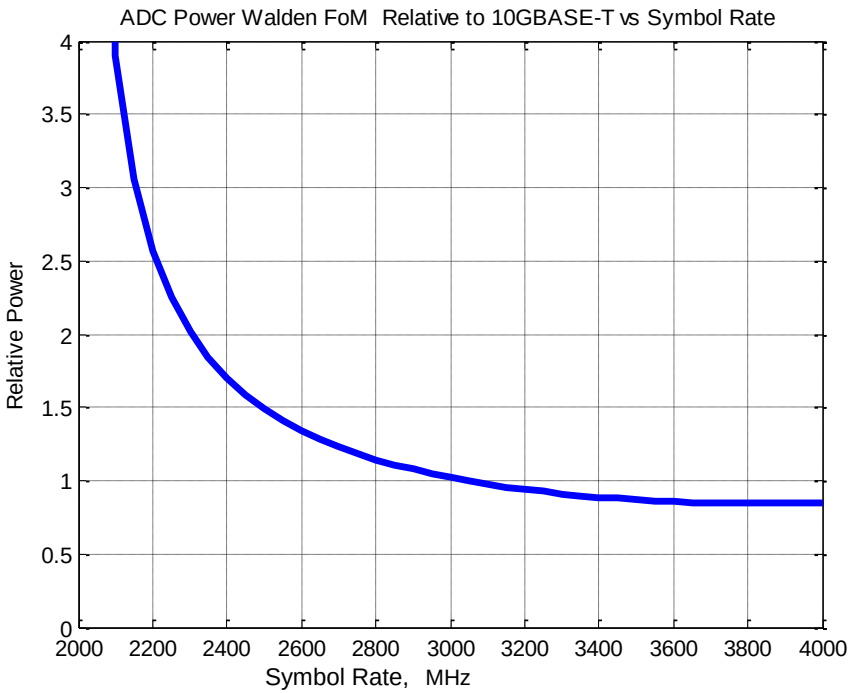


Using worst-case limit-line scaling, the TIA Draft 0.8 RL improvement results in about a 12% decrease in the estimated ADC power.

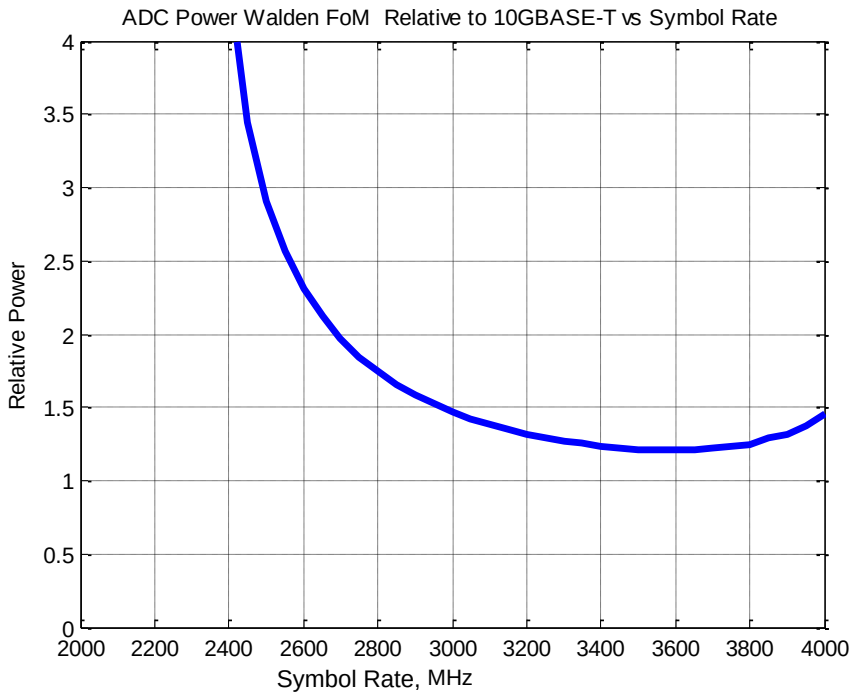
Cat8 long channel 3-24-3.s16p (Initial model later replaced with version distributed to .3bq)
Pulse_NGBase-T_Magnetics.S4P
4-port 8cm trace model

Analysis of 16-Port PCB Models ADC Power FoM vs Symbol Rate

stackup2_2in_30mils_isolation.s16p



stackup1_8in_15mils_isolation.s16p



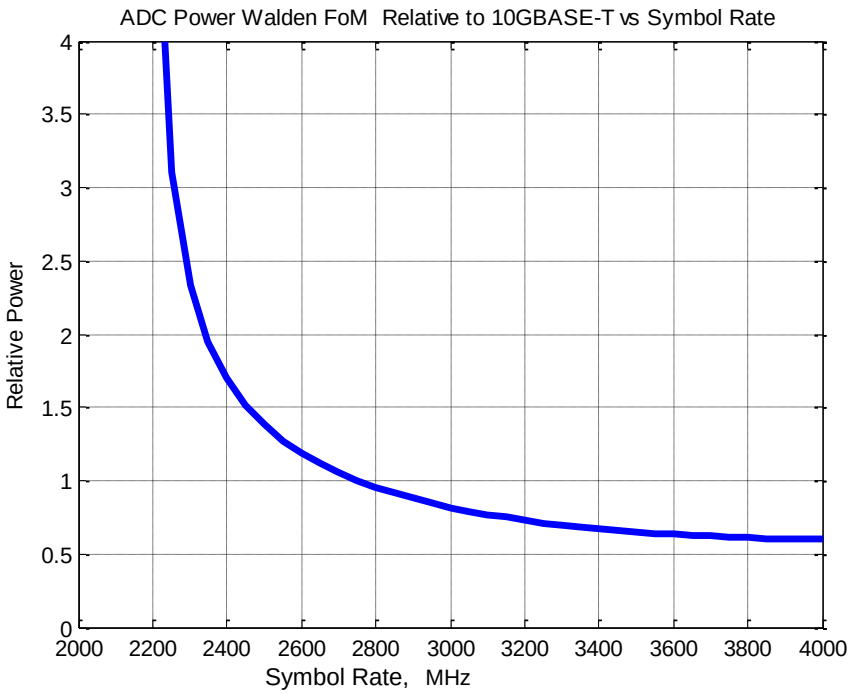
At 3200 MHz symbol rate, comparing the least and most stringent PCB channel models, the estimated ADC power varies by up to about 35%.

- **Longer trace and narrower spacing drives the worst-case analysis.**

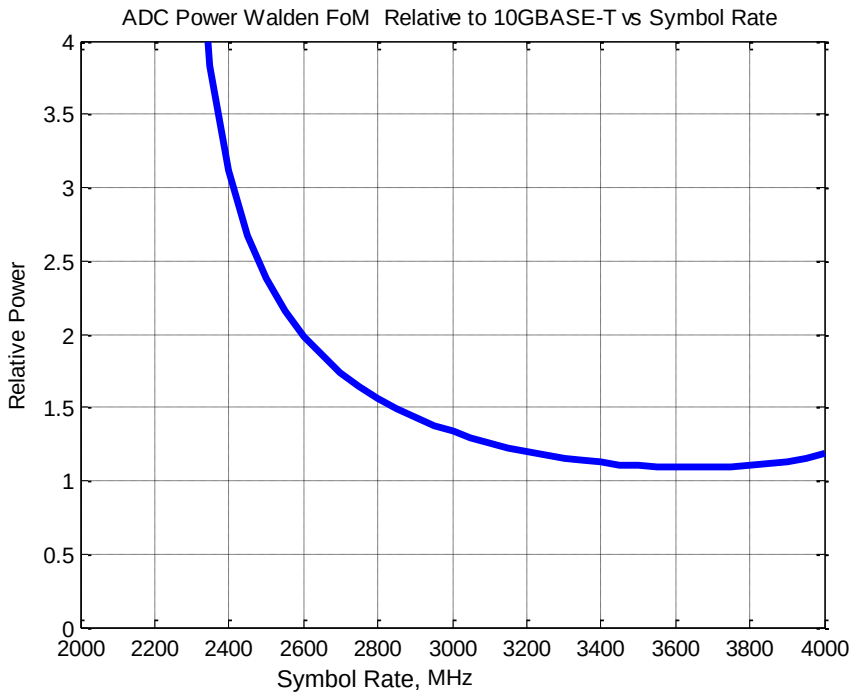
Panduit_Channel_30m_V1.s16
Pulse NGBase-T Magnetics.S4P

Analysis of 16-Port Cable Models ADC Power FoM vs Symbol Rate

wlarsen_short_channel_1-3-1.s16p



wlarsen_long_channel_3-24-3.s16p



At 3200 MHz symbol rate, comparing the short and long cable channel models, the estimated ADC power varies by up to about 64%.

- **The longer cable channel drives the worst-case analysis.**

Pulse NGBase-T Magnetics.S4P
stackup2_8in_30mils_isolation.s16p

Conclusions and Next Steps

- Initial PCB and Cable 16-port S-parameter models have been included to exercise the end-to-end PHY channel simulations.
- A 16-port model for the isolation path (ie integrated connector module) is still needed to complete this analysis.
  - Channel ad hoc committee members are actively working on creating these 16-port models from measurements.
  - A 4-port model of the magnetics only and without the effects of crosstalk was used in the simulations and results presented.
- Intermediate results show a significant ADC relative power penalty for symbol rates below 2800 MHz and above 4000 MHz (or design bandwidths below 1400 MHz and above 2000 MHz).
  - Recommend focusing symbol rate study in the range of 2800 MHz to 4000 MHz.

Thank you