IEEE 802.3br D1.0

Proposal to addressi the editor’s note in clause 9.4.5

Current editor's note

- This presentation provides alternatives to address the editor's comment in clause 99.4.5 (page 37, line 30 in D1.0).

- Text from the draft:
    - *Editor's Note (to be removed prior to publication) - If the final mFrame of a preempted frame is lost, i.e receive processing is waiting for another fragment in a preempted frame and the start of the next preemptable frame arrives, the receive processing state diagram operation will discard the new frame as well as the incomplete frame.]*

Alternative 1: Add an “exception” to following figure 99-5

Change

“Receive processing shall be performed as specified in Figure 99–5”

To

“Receive processing shall be performed as specified in Figure 99–5 except as noted in clause 99.4.5.x.”

Add new clause 99.4.5.x:

99.4.5.x Special handling of lost final mFrames

Per figure 99-5, if one or more non-final mFrame of a preempted frame have been received, the receiver will be in the WAIT FOR RESUME state (waiting to receive the next mFrame from the same preempted frame). If the final mFrame in the preempted frame is lost or has a corrupt SMD, the state machine will still be in the WAIT FOR RESUME state when the first mFrame of the next preemptable frame is received and the state machine will transition to the ASSEMBLY ERROR state, causing the pMAC to interpret both the current preempted frame and the next preemptable frame as invalid frames and both frames will be dropped by the pMAC.

Receive processing shall ensure that the pMAC will detect an error in the preempted frame where there is a missing final mFrame, Receive processing may either cause the pMAC to detect an error in the second frame (as per figure 99-5) or pass the second frame to the pMAC as a valid frame.

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Alternative 2: Split receive processing into two state machines with a fifo

Add to clause 99.4.5 (Receive processing)

The receive processing consists of a receive processing input block, a fifo, and the receive processing output block.

The receive processing input block is responsible for parsing and validating incoming mFrames and reassembling such mFrames into Frames.

The fifo provides buffering such that the input block can process a new mFrame while the output block is still forwarding data from the previous mFrame to the pMAC. The fifo should provide enough buffering such that the input block can receive new data while the output block is forwarding a Frame Check Sequence, an IPG, and a preamble to the pMAC.

The receive processing output block is responsible for passing data to the pMAC, ensuring that the pMAC will detect a FrameCheckError due to any reassembly errors, and ensuring that a there is a valid IPG in all frames sent to the pMAC

Alternative 2: Split receive processing into two state machines with a fifo (cont).

Add to clause 99.4.7.3 (Variables)

receiveFifo

A fifo array used to store data from new incoming mFrames while data from the previous mFrame is being forwarded to the pMAC. Each element of the fifo can hold either the value from an octet, the special value “EOF” (indicating that the frame has ended), or the special value DISCARD_EOF (indicating that frame should be discarded).

Add to clause 99.4.7.4 (Functions)

FIFO_DEQUEUE

Returns an Invokes an implementation dependent process that dequeues an element from the fifo and returns the dequeued data element data

FIFO_EMPTY

Returns a boolean value indicating if the receiveFifo is not storing any elements. true indicates that the receiveFifo is empty. false indicates that the receiveFifo has data that can be dequeued.

FIFO_ENQUEUE(data)

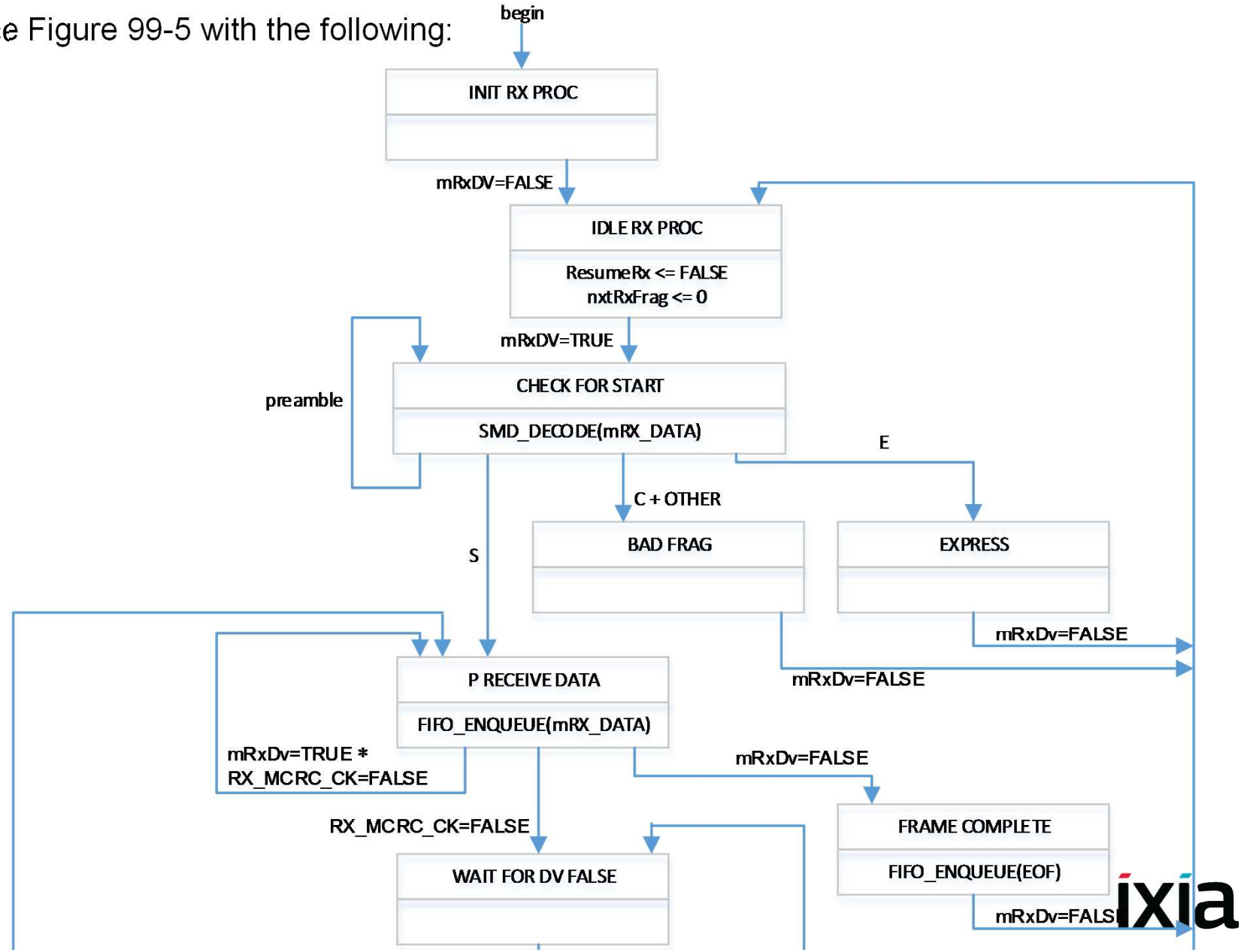
Invokes an implementation dependent process that enqueues data to the receiveFifo.

FIFO_HEAD_DATA

Returns the data at the head of the receiveFifo without dequeuing the data from the fifo.

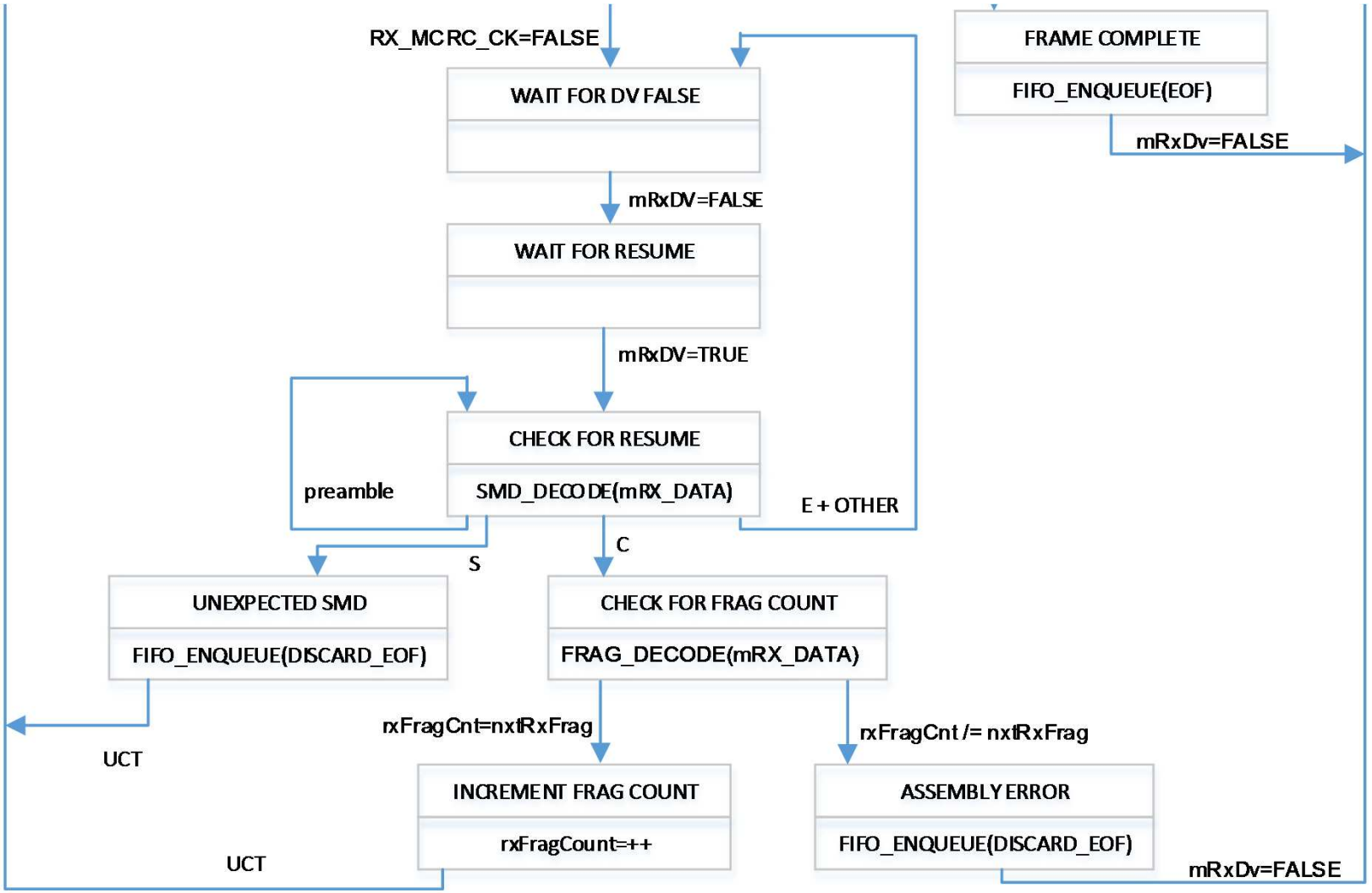
Alternative 2: Split receive processing into two state machines with a fifo (cont).

Replace Figure 99-5 with the following:



Alternative 2: Split receive processing into two state machines with a fifo (cont).

Replace Figure 99-5 with the following (continued):



Alternative 2: Split receive processing into two state machines with a fifo (cont).

Add new Figure 99-x after Figure 99-5: