# Architecture: Configurations and use cases

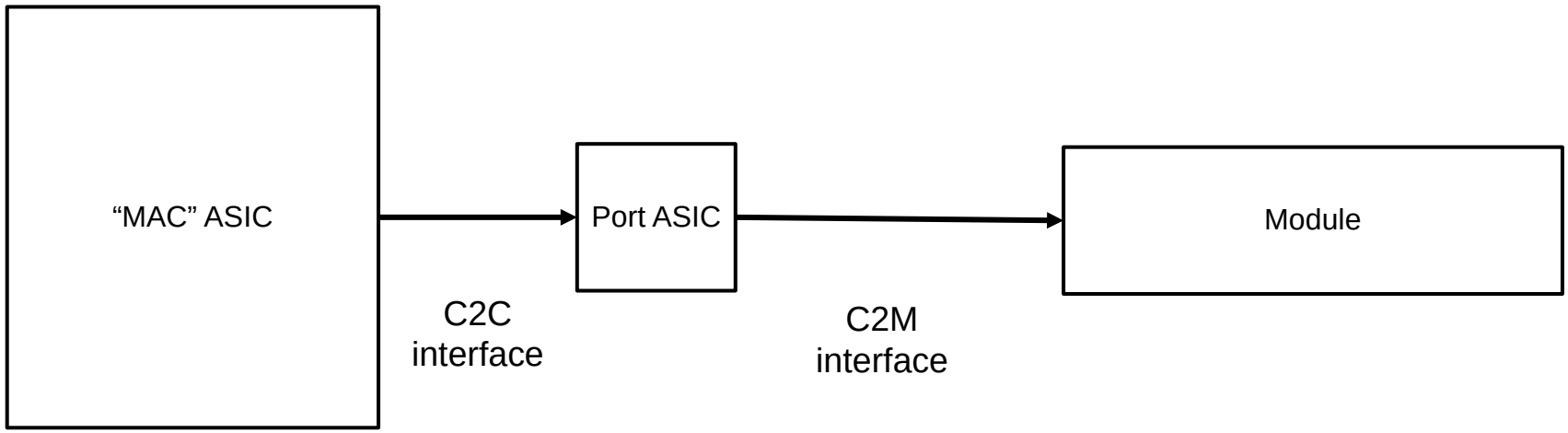
This presentation is a corollary to the architecture baseline shown in gustlin_3bs_02_0514

John D' Ambrosia & Hugh Barrass

with assistance from Pete Anslow, Mark Gustlin, Adam Healey, David Law, Gary Nichol, David Ofelt

# General picture

- Many (most) host systems will include a C2C and a C2M interface



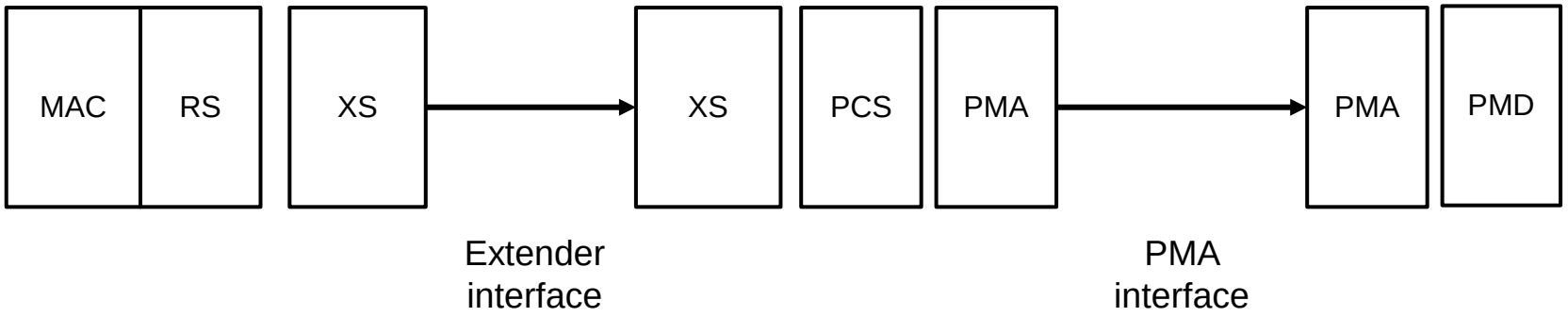

"MAC" ASIC includes MAC & a bunch of other stuff – often serves multiple ports

Port ASIC contains newer technology that could not be accommodated in current generation of "MAC" ASIC.

Module will be as simple as possible (with thermal/space challenges) – also accommodates new PHY components that weren't available when hosts system finalized.

# General architecture

- Basic components from gustlin_3bs_02_0514



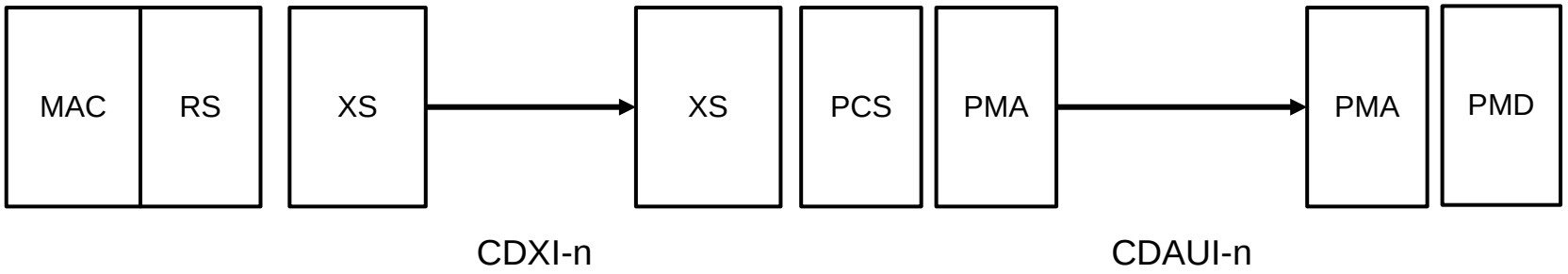

XS and extender interface is used to extend the xMII so that the raw data stream can be presented to the PCS

Extender is used in any situation where the coding or FEC requirements are different between the internal interface and the external PHY

PMA interface is used when there is no requirement to change the coding or FEC between the internal interface and the external PHY

# Naming the interfaces

- CDAUI & CDXI




**AUI – “Attachment Unit Interface” – fancy-speak for “the way you connect to a pluggy-thing”**

Generally, if a host has both an extender interface AND a PMA interface, then the PMA interface will connect to a module – therefore PMA interface is an “AUI”

Unfortunately, there will also be cases where a host has 2 extender interfaces or 2 PMA interfaces – we just have to live with that…

**CDAUI – 400G Attachment Unit Interface = physical instantiation of PMA interface**

**CDXI – 400G Extender Interface = physical instantiation of extender interface**

# Configs

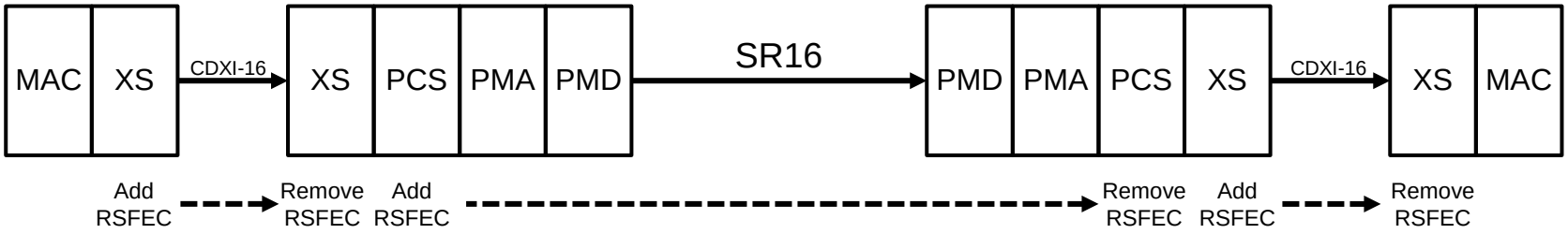
- Capturing possible current/future configurations

Mapping host configuration examples to architectural diagrams – aim to build a comprehensive library of configurations

Capture host sublayer breakdown, with various module options – with variations at both ends of a link

**Detailed proposals for coding/FEC/etc. can be measured against forward & backward compatible implementations**

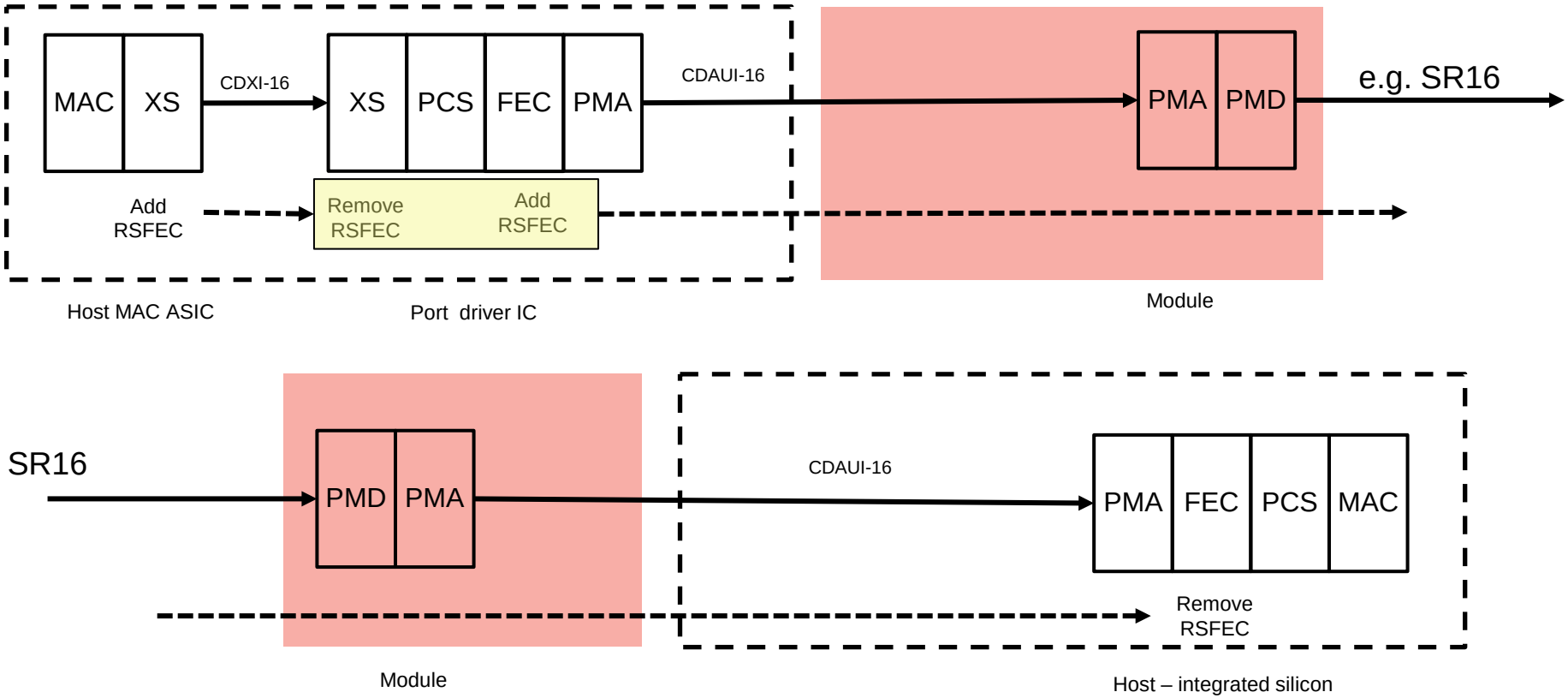
e.g. a 400GBASE-SR16 could be drawn like this…




… but this doesn't mean that we are endorsing a 400GBASE-SR16 proposal
Some of the items depicted may be the subject of future projects – some may never exist!

# Configs

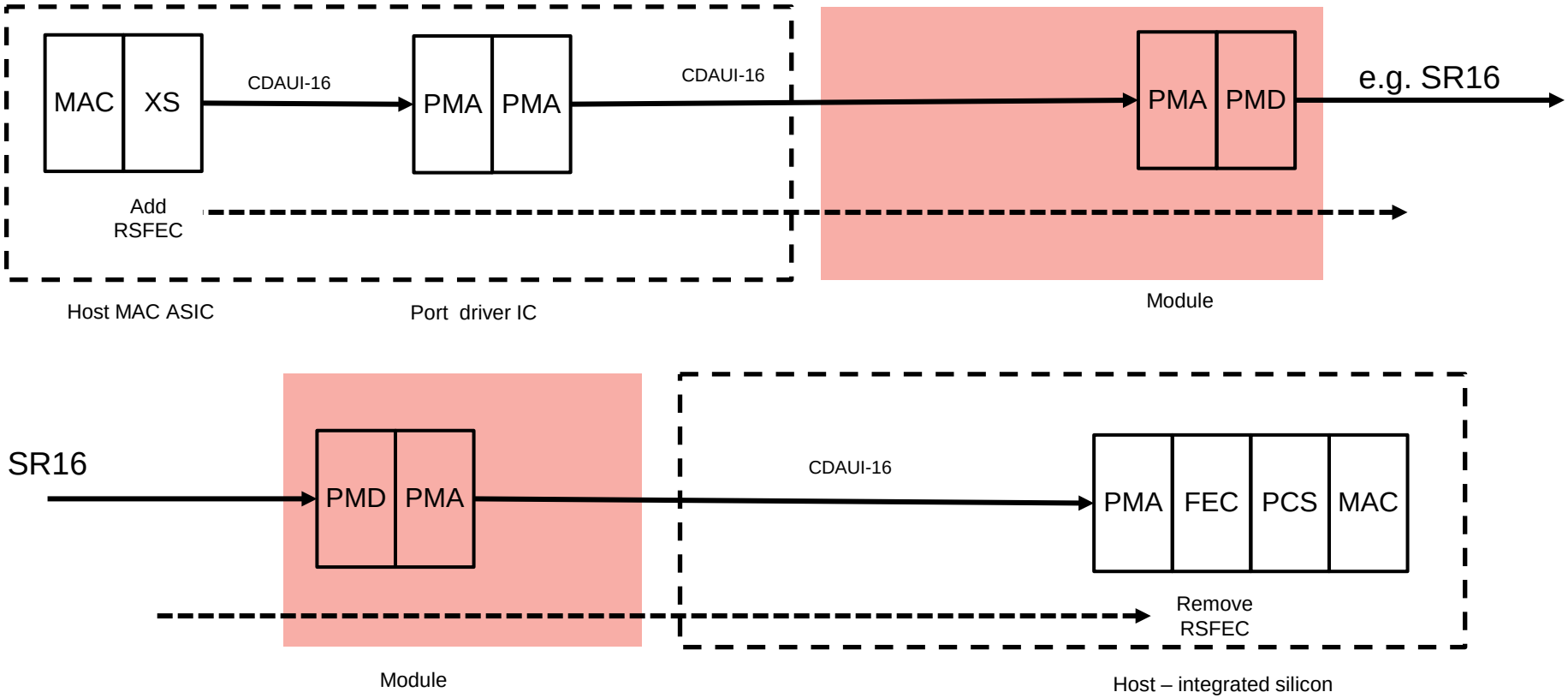
- Capturing possible current/future configurations
  - Host config #1 – 1st gen. – 16 lane module interface




Definition for 16-bit XS & SR16 PCS/FEC/PMA should be as similar as possible so that driver IC has minimal logic

# Configs

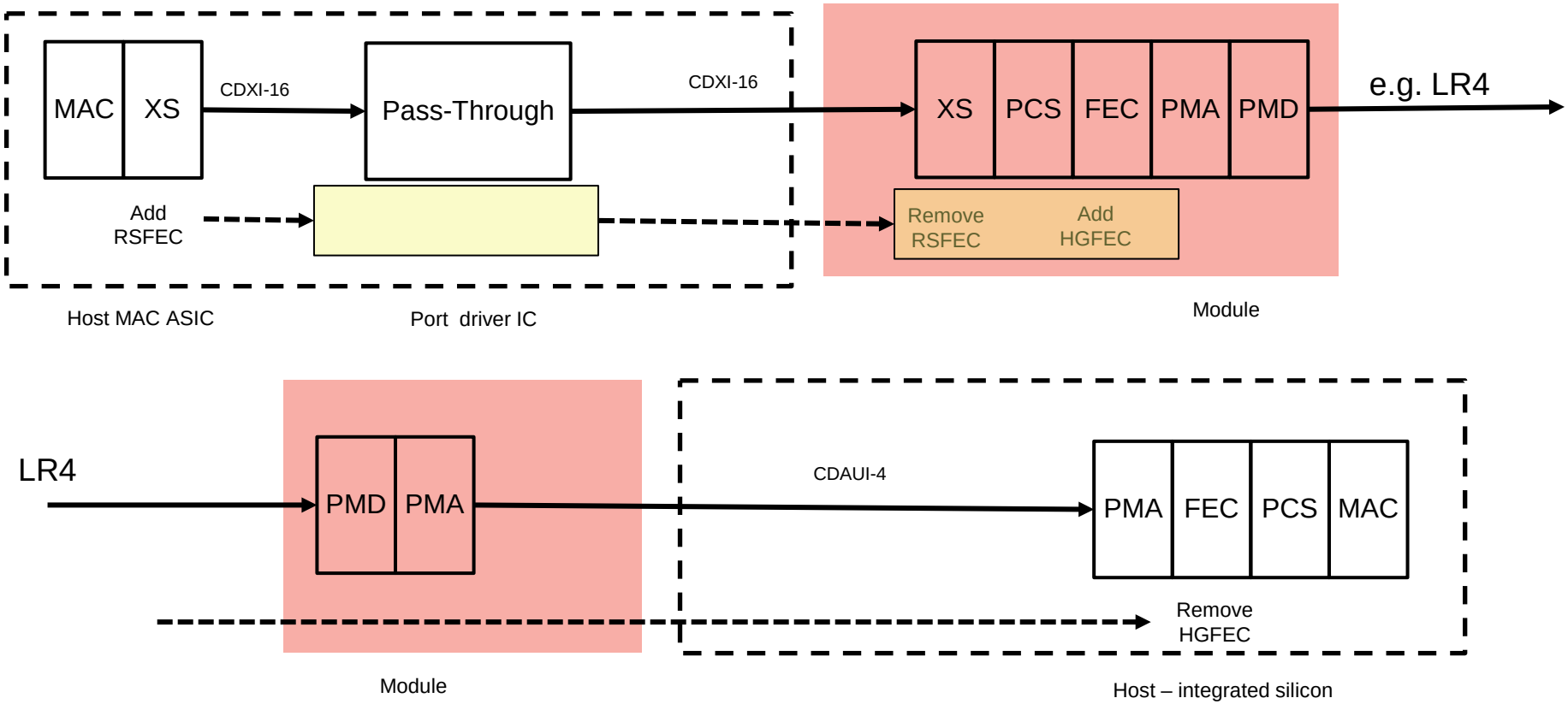
- Capturing possible current/future configurations
  - Host config #1 – 1st gen. – 16 lane module interface, alternate architectural view




The detailed architecture proposal may require both views, or may make previous view redundant

# Configs

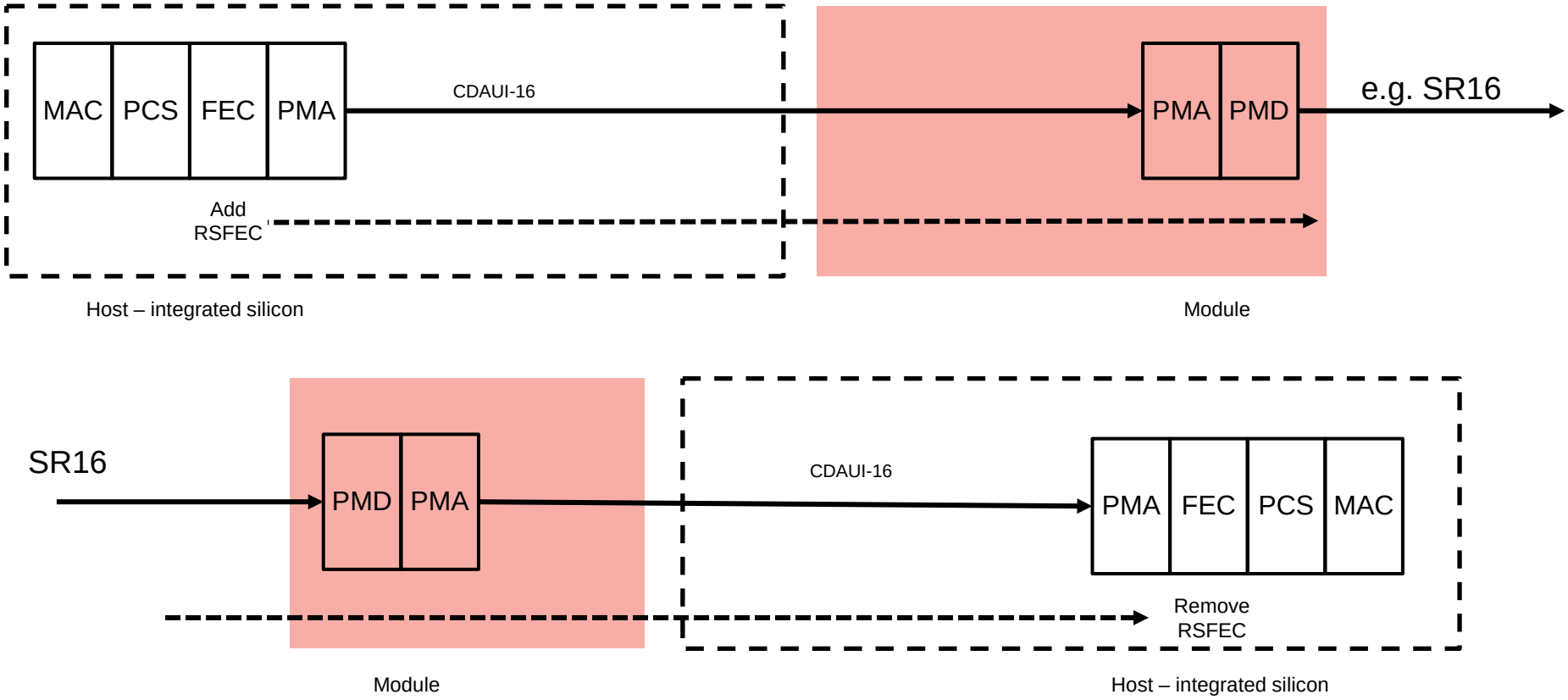
- Capturing possible current/future configurations
  - Host config #1 – 1st gen. – 16 lane module interface




Complex module to handle coding & FEC in advance of host integration
Pass through or back-to-back XS for this will depend on detailed specifications

# Configs

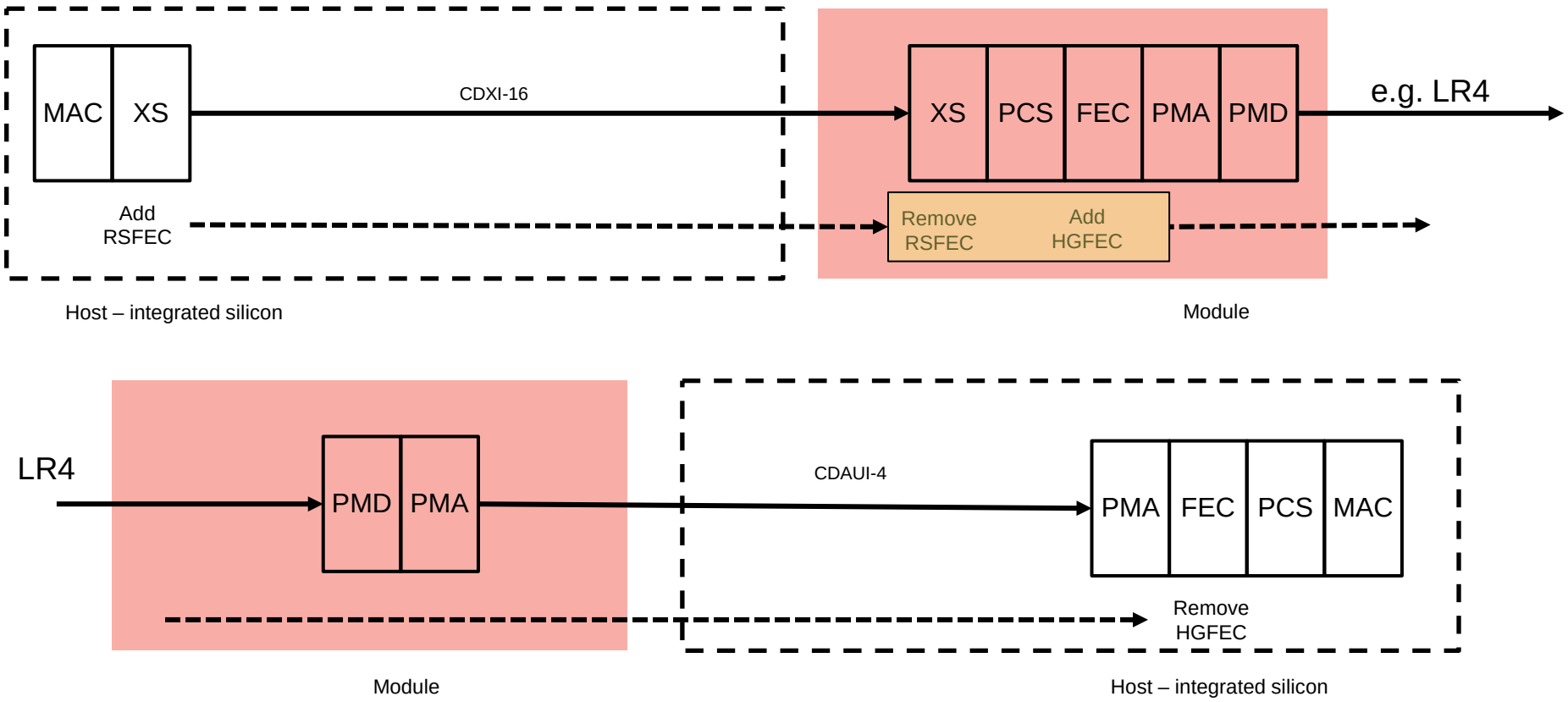
- Capturing possible current/future configurations:
  - Host config #2 – 2nd gen. – 16 lane module interface




Driver integrated with host ASIC, indistinguishable from config #1 from external view

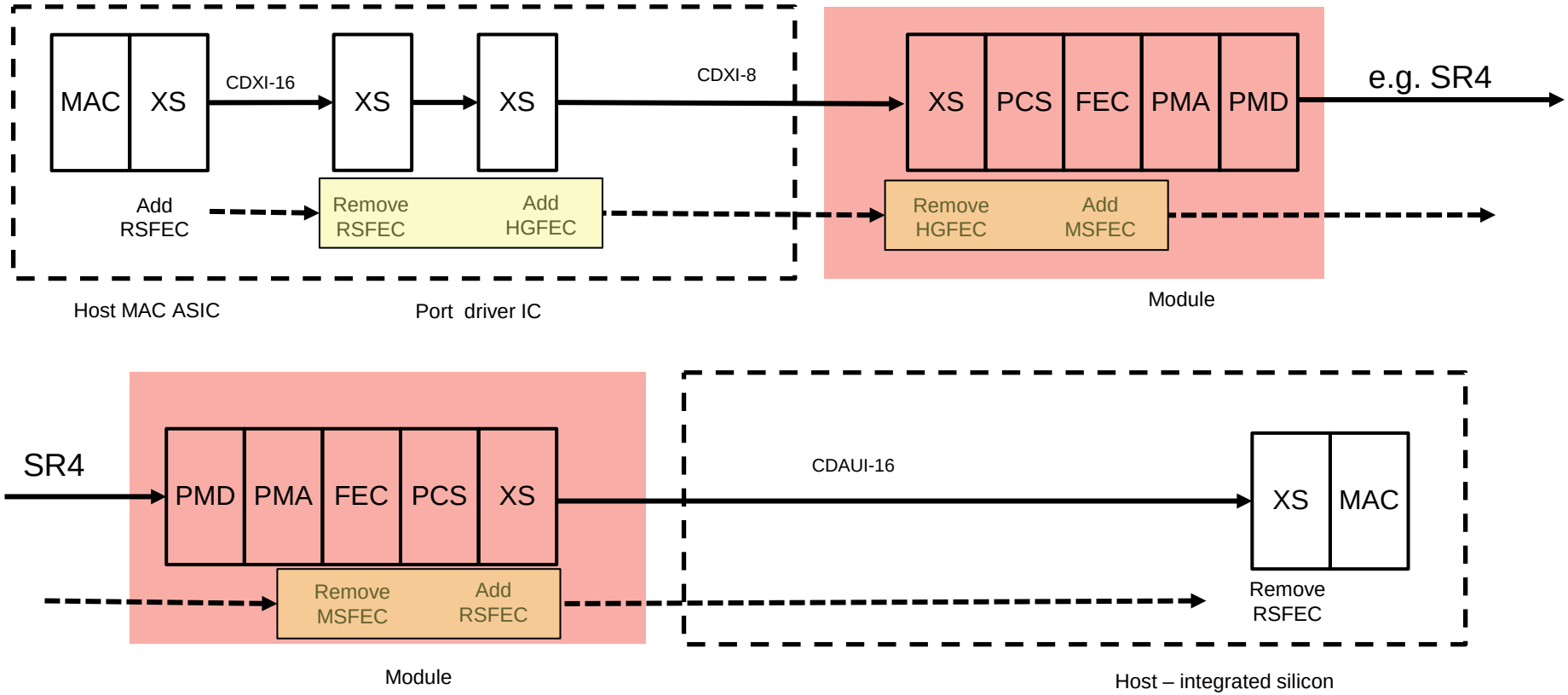
# Configs

- Capturing possible current/future configurations:
  - Host config #2 – 2nd gen. – 16 lane module interface



# Configs

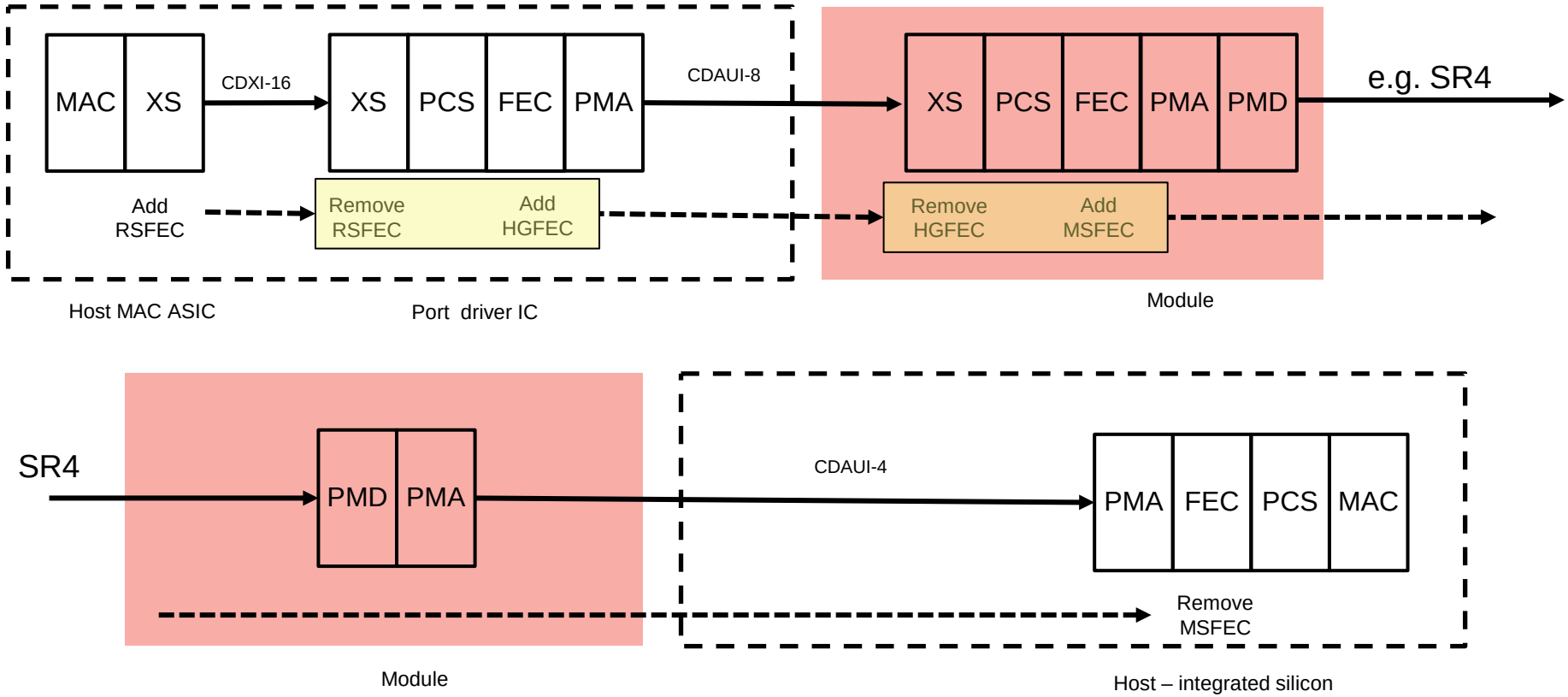
- Capturing possible current/future configurations
  - Host config #3 – 1st gen. – 8 lane module interface




More aggressive C2M interface, re-using 1st gen. host ASIC – Highly complex modulation requires MSFEC

# Configs

- Capturing possible current/future configurations
  - Host config #3 – 1st gen. – 8 lane module interface




Future link partner may eliminate recoding in module – if MSFEC also works for C2M interface