400Gb/s 500m PMD Alternatives

400Gb/s Ethernet Task Force

IEEE 802.3 Interim Meeting

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IEEE

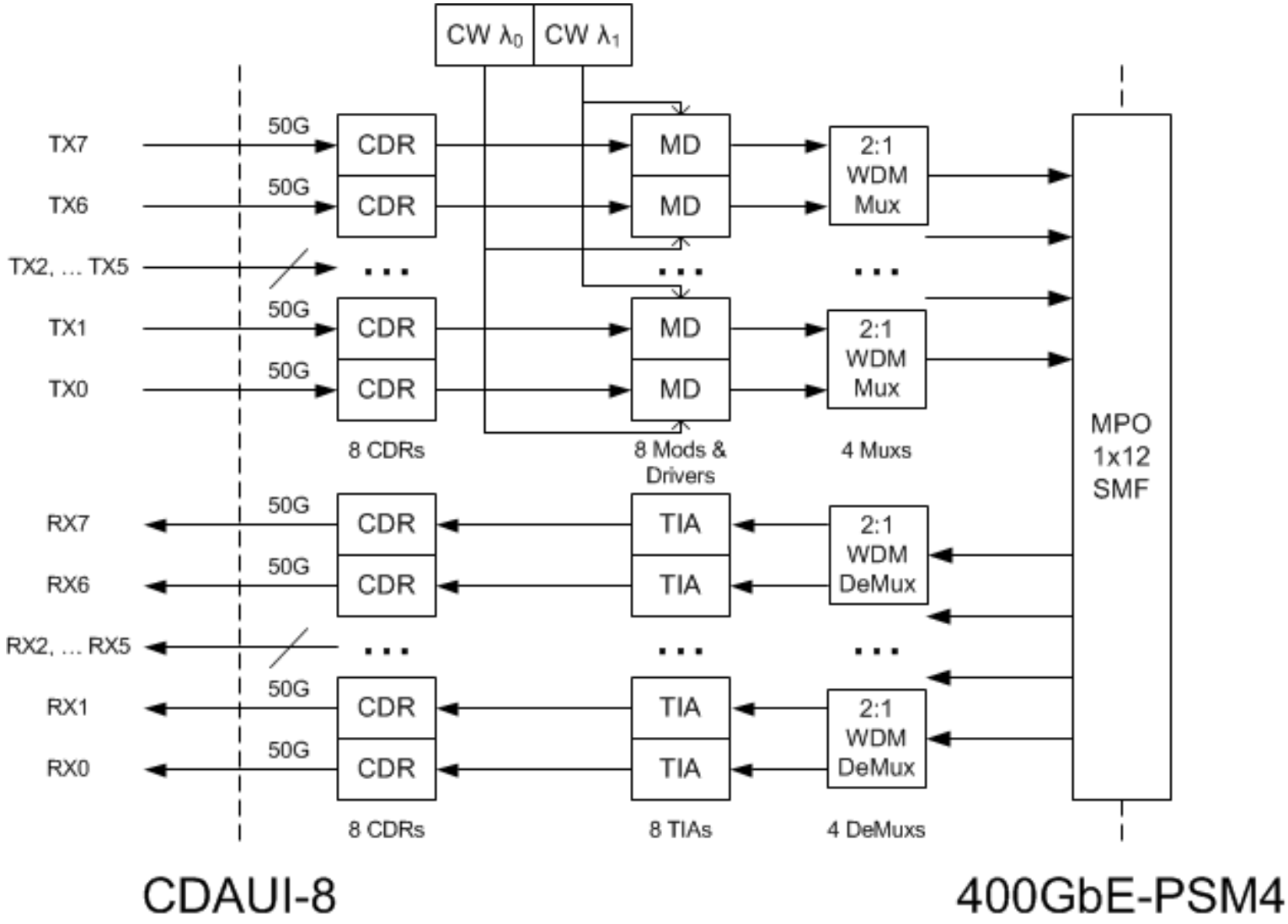
Finisar®

500m Reach Objective

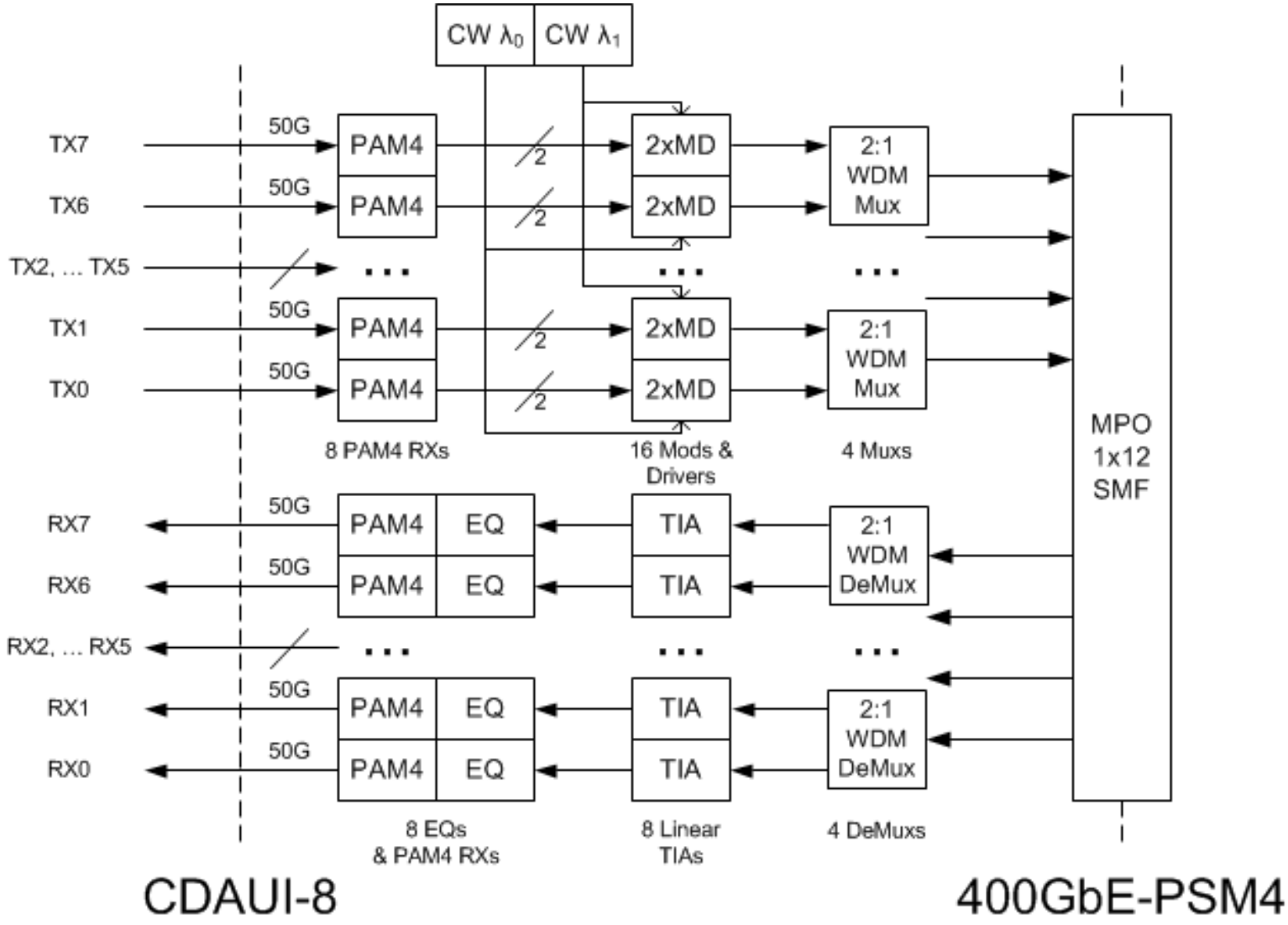
	500m	2km
TDP	~TP (1310nm)	~TP (1310nm)
Loss	~4dB	4dB (5dB preferred)
Loss Ref.	kolesar_02_0313_optx	cole_01_0911_NG100GOPTX

- Distinct 500m and 2km duplex SMF PMDs are not justified
- Distinct 500m PMD is justified if it uses different fiber type ex. parallel SMF (8f) vs. duplex SMF (2f) for 2km
- 500m objective best met by 400GbE-PSM4
  - Gen1 bit/sec cost parity with 100GbE optics
  - High density 4x 100GbE break-out

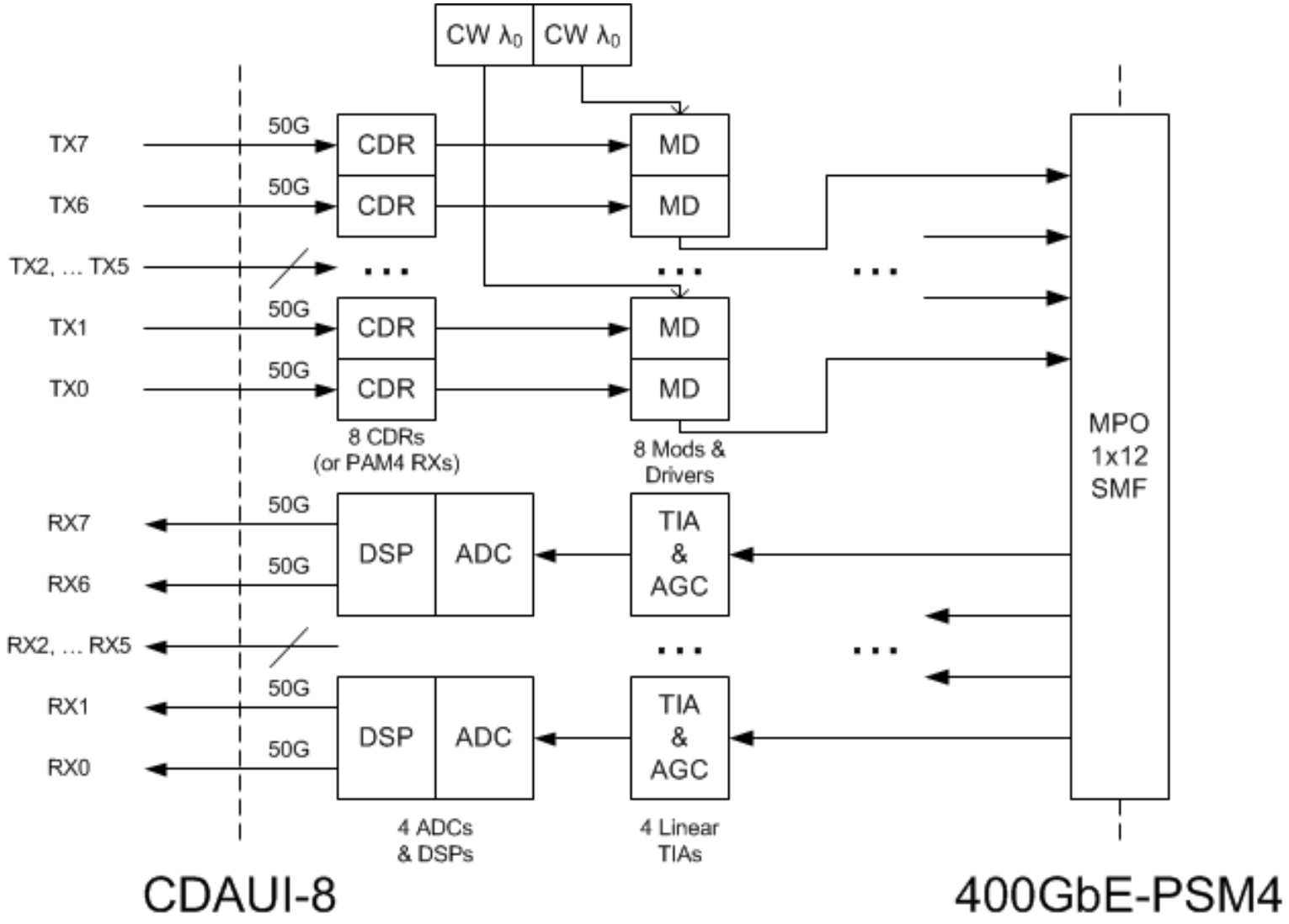
400GbE-PSM4 Alt 1: Quad 2x 50G NRZ λs



400GbE-PSM4 Alt 2: Quad 2x 50G PAM-4 λs

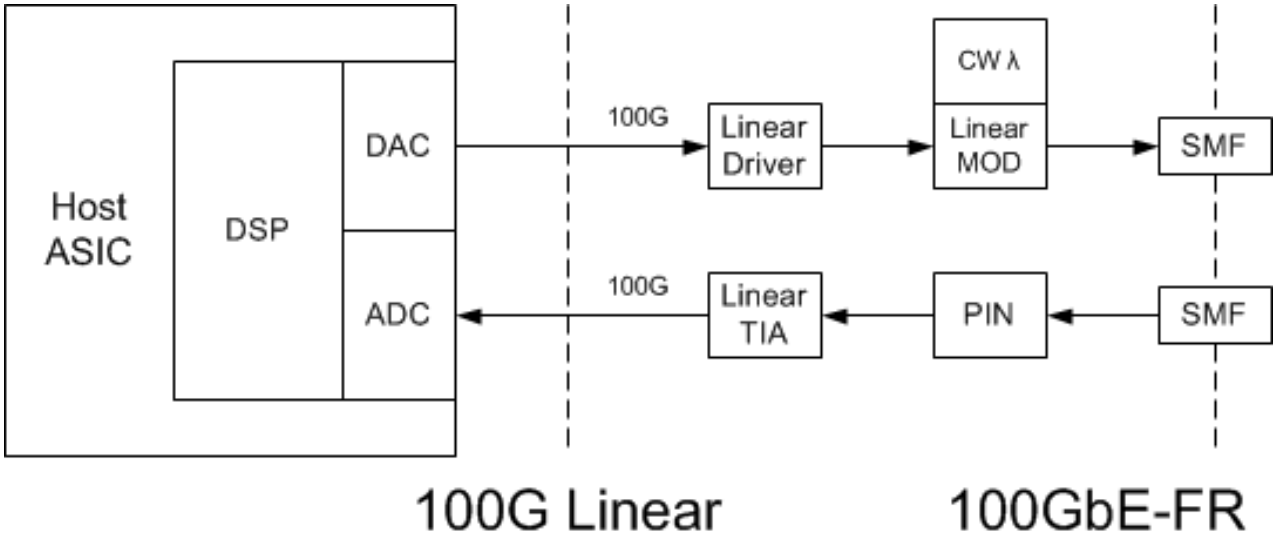


400GbE-PSM4 Alt. 3: Quad 1x 100G PAM-4 λ



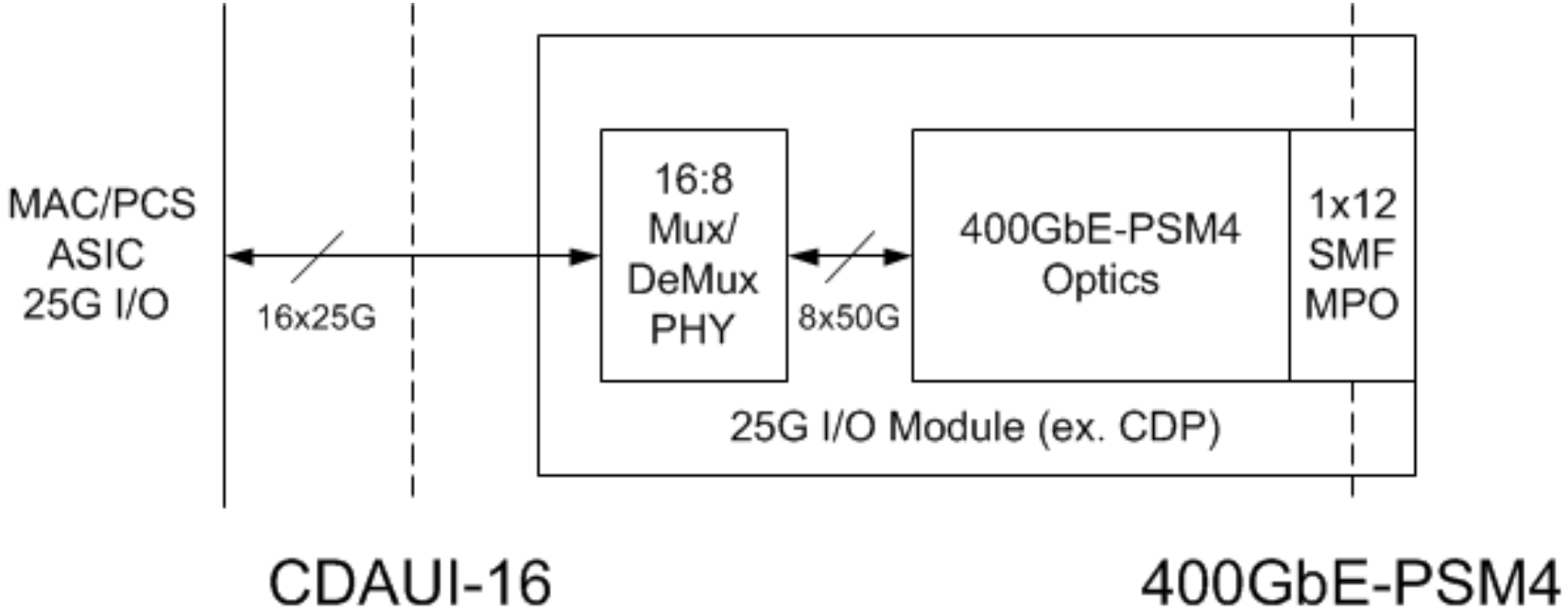
Ultimate 400GbE-PSM4 100G I/O Architecture

- Ultimate 100GbE Architecture (ex. SFP100)

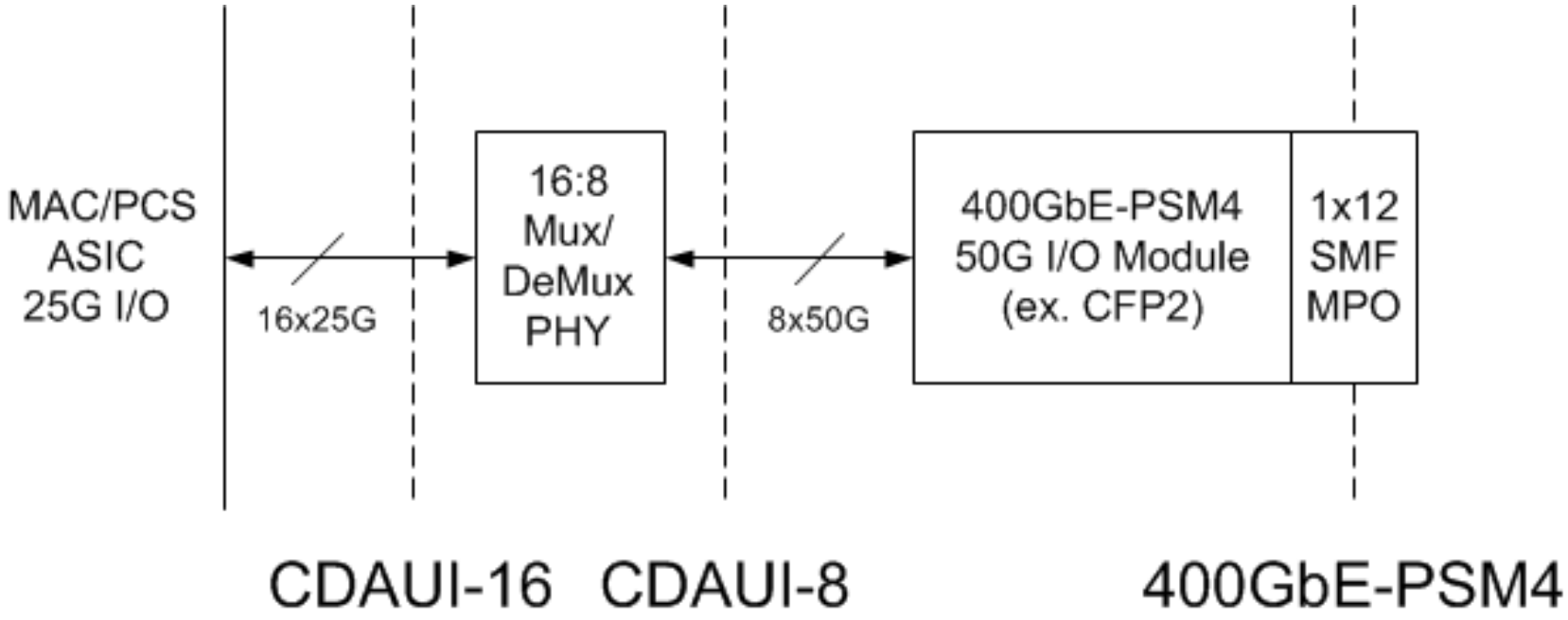


- Ultimate 400GbE-PSM4 Architecture is quad version of the above (ex. CFP4)
- Linear Interface favors more complex modulation formats like DMT or QAM over PAM
- This is many years away (>2020)

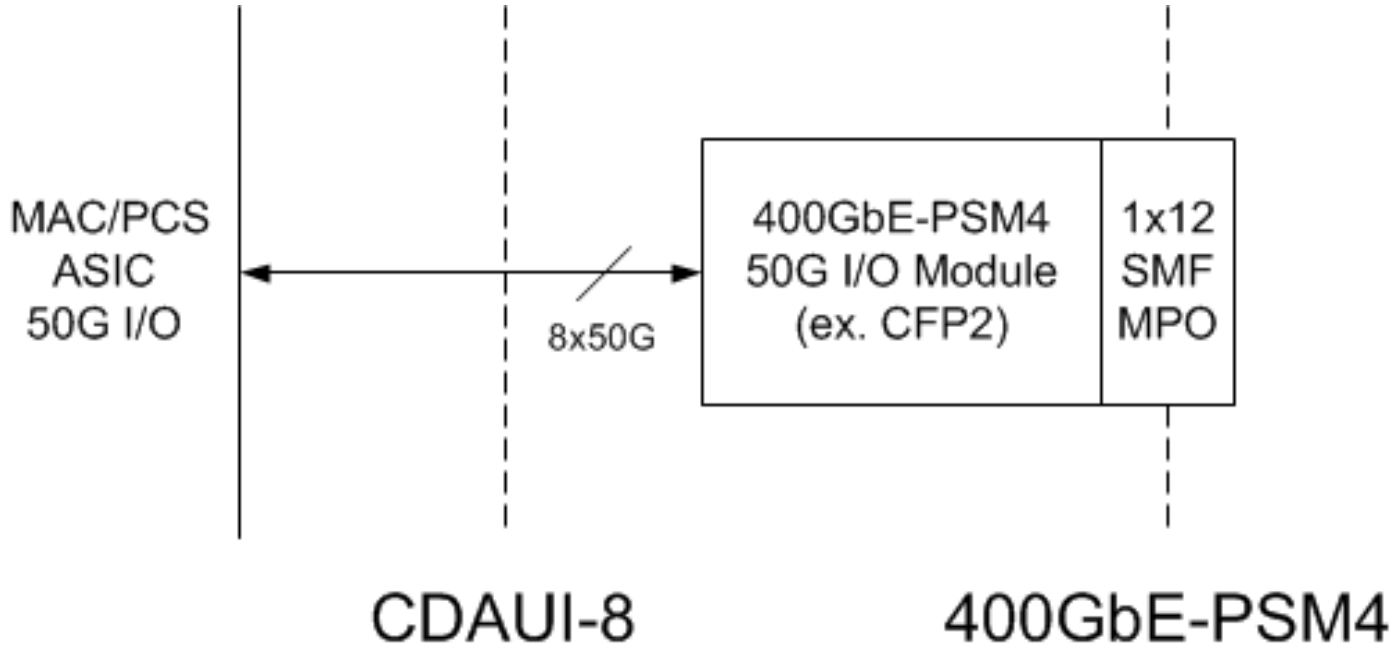
ASIC 25G I/O ⇔ Module 25G I/O



ASIC 25G I/O ⇔ Module 50G I/O



ASIC 50G I/O ⇔ Module 50G I/O



Perspective on PMD Proliferation

Myth: PMD proliferation is bad

Fact: PMD proliferation is bad if it's the other guy proliferating

Myth: Standards based, multi-vendor, multi-gen. form factor, multi-app PMD is good

Fact: Standards based, multi-vendor, multi-gen form factor, multi-app PMD is good if it's free (as in free lunch)

Ex. 1: 10x10G MSA example

- Two more PMDs
- Single vendor & single-gen form factor
- Single-app baseline 2km/2.5dB loss spec
- Unsustainable business model

Ex. 2: New IDC deployment model example

- MS comments in 802.3: single-gen, MSA PSM4 is OK

Take away for 400Gb/s: focus on today's needs

500m Reach Objective Discussion

- 400GbE-PSM4 offers 100G bit/sec cost parity for Gen1
- 400GbE-PSM4 enables high density 4x 100GbE break-out
- Long term considerations have low value in the market
- Modulation picked in this project may not be the ultimate high volume modulation
- Optimize what we know, not crystal ball future technology
- Progress must be made on 40-50Gb/s electrical I/O in the OIF CEI-56 Project to define optimal optical modulation

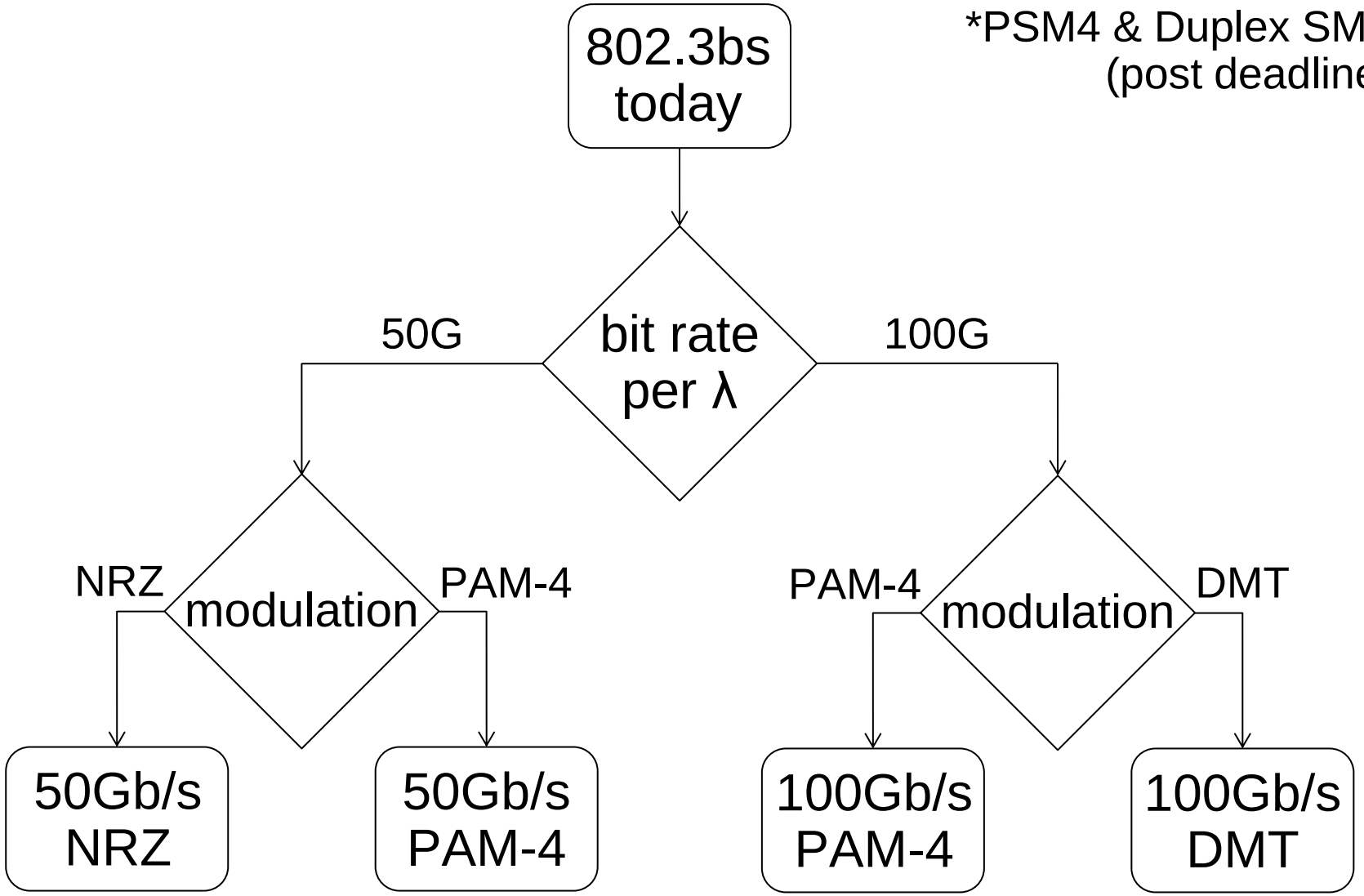
Appx.1: OIF 40-50Gb/s I/O (post deadline)

CEI-56G Project	Application	Loss dB	Max Reach mm	Need Now
Ultra Short Reach USR	Chip-to-OE (within MCM)	no proposal	10	N
Extra Short Reach XSR	Chip-to-OE (Chip-to-PHY)	5 to 10	50	Y
Very Short Reach VSR	Chip-to-Module	10 to 20	100	Y
Medium Reach MR	Chip-to-Chip	15 to 25 (@14G)	500	Y
Long Reach LR (not a project)	Backplane (Chip-to-Fabric)	25 to 50 (@ 14G)	1000	N

Specification problem: conflicting requirements between single ASIC SerDes architecture (modulation) for all apps. vs. optimized architecture for each rate and reach

Appx.2: Proposed SMF PMD* Decision Tree

*PSM4 & Duplex SMF (post deadline)



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Thank you