The 400GbE Project: An Overview

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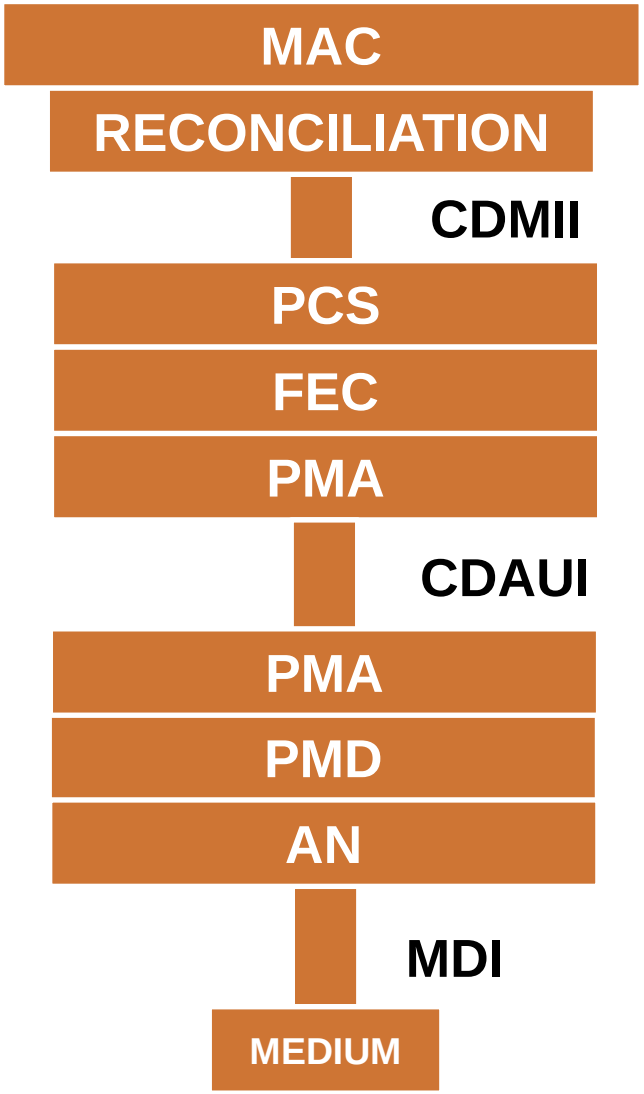
IEEE P802.3bs 400 GbE Objectives

- Support a MAC data rate of 400 Gb/s
- Support a BER of better than or equal to 10^{-13} at the MAC/PLS service interface (or the frame loss ratio equivalent)
- Support full-duplex operation only
- Preserve the Ethernet frame format utilizing the Ethernet MAC
- Preserve minimum and maximum FrameSize of current Ethernet standard
- Provide appropriate support for OTN
- Specify optional Energy Efficient Ethernet (EEE) capability for 400 Gb/s PHYs
- Support optional 400 Gb/s Attachment Unit Interfaces for chip-to-chip and chip-to-module applications
- Provide physical layer specifications which support link distances of:
  - At least 100 m over MMF
  - At least 500 m over SMF
  - At least 2 km over SMF
  - At least 10 km over SMF

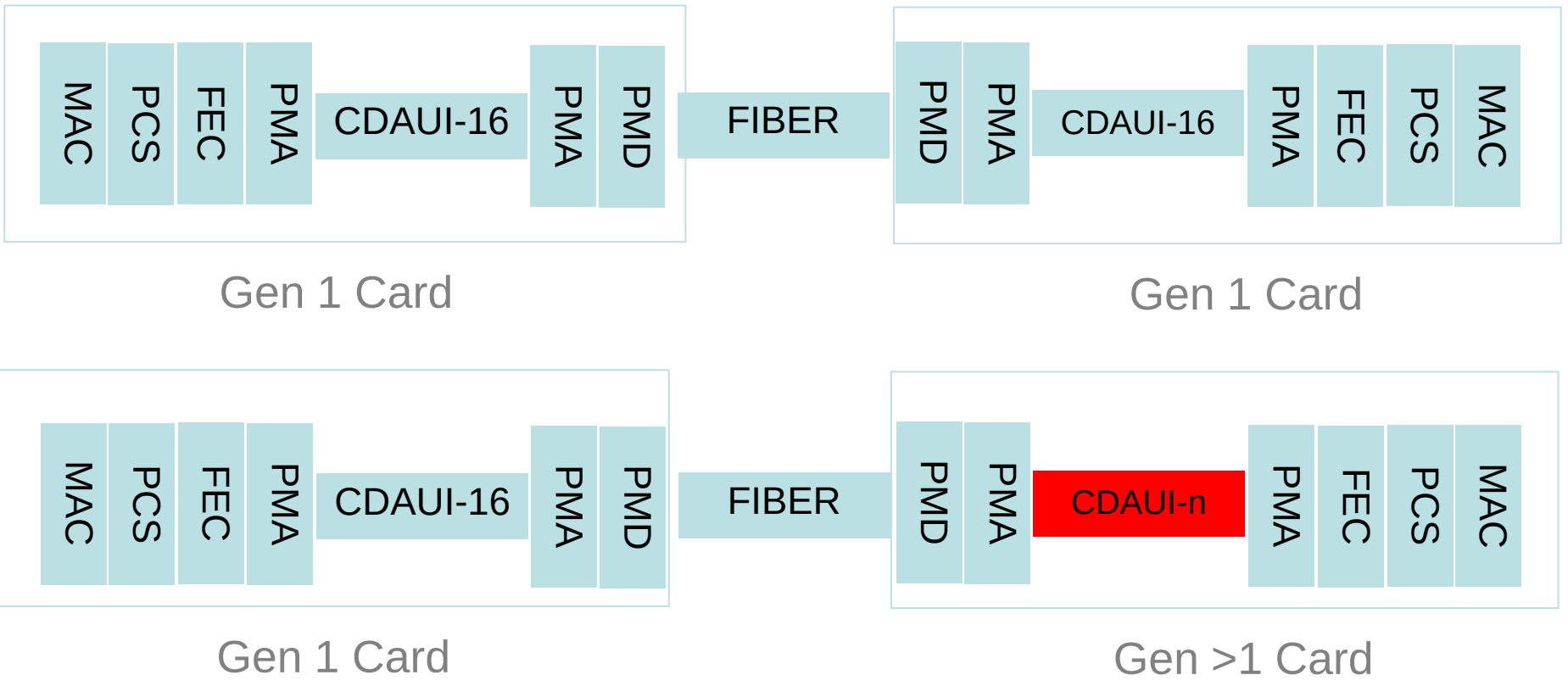
* Approved by IEEE 802.3 WG, 20-Mar-2014

Issues – Bottom Up

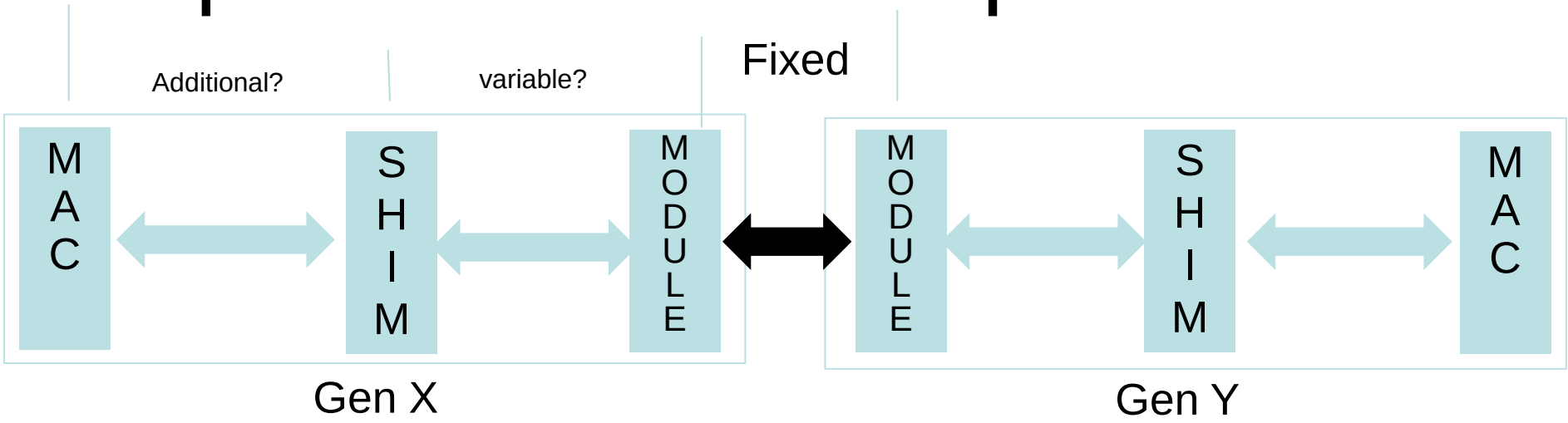


- Medium- Channel Models
- MDI?
- PMD
  - 16x25G / 8 x50G / 4x100G? (Modulation, Parallelization)
  - Breakout?
- CDAUI / PMA
  - PMA Functionality
  - 802.3ba architecture? Between 2 PMA sublayers?
  - Channel / Connector for module?
  - Signaling characteristics
  - FEC?
    - Per electrical interface? FEC for the entire link? CDAUI: Above / below PCS?
  - Number / placement within layer structure
- FEC (see next slides)
  - Type?
  - Budgeting?
  - Multi-generation considerations
- PCS
  - Similar 802.3ba PCS Structure?
  - Bit versus Block encoding?
  - Embedded FEC Specific to PHY?
- CDMII
  - Extender Sublayer?

FEC: Multi-Generation Considerations



Thinking Generically From an Implementation Perspective



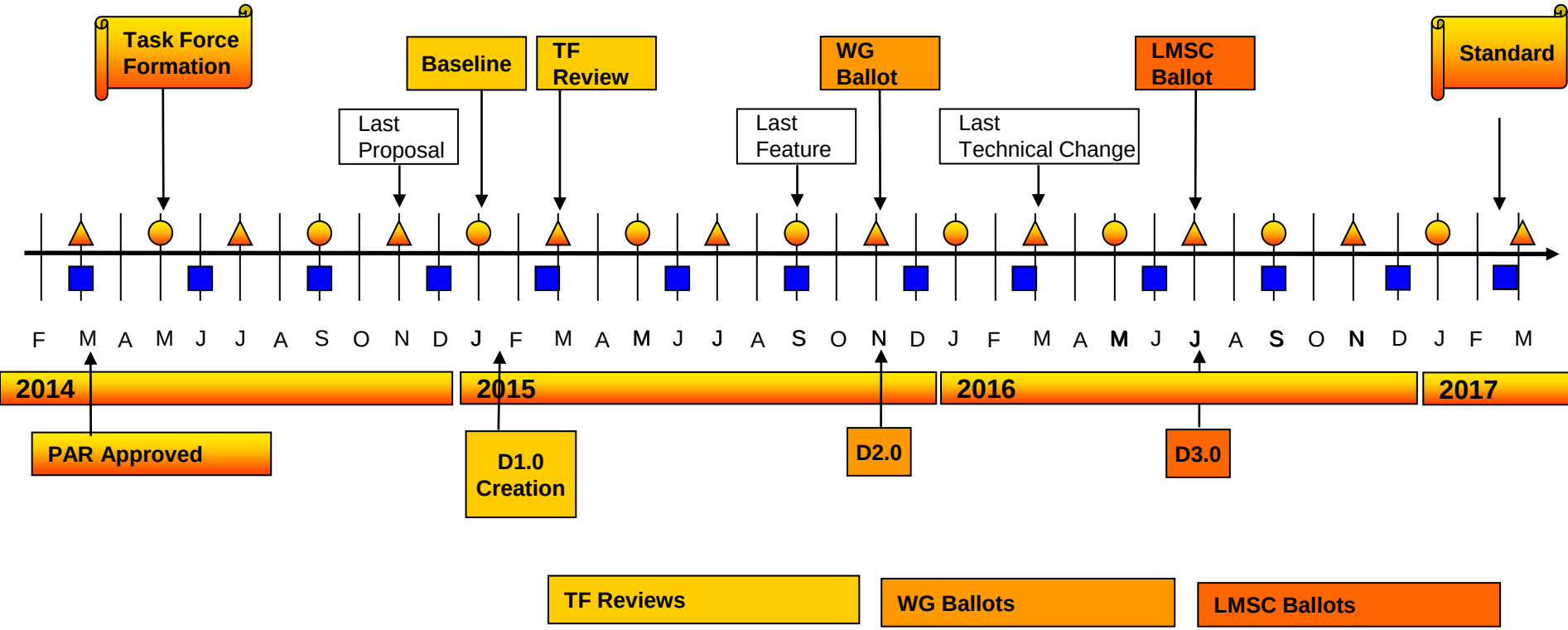
Assume retiming at module electrical interface?
Assume FEC (or chance of) in module?
“SHIM” – retiming & FEC?
“SHIM” – may or may not be there
Concerns

- FEC Zones boundaries – where are they?
- Specifying clearly so budget can’t be stolen if a “total” approach is used
- How do we determine a total budget with fixed zones for variable implementations and generations

Organization of Project Work

Logic Functions	Electrical Interfaces	Optical PMDs
▪ Amendments to MAC, RS, and MAC PHY interfaces ▪ RS and CDGMII ▪ Extender Sublayer (CDXS)? ▪ PCS functions ▪ PMA functions ▪ OTN Compatibility ▪ EEE (LLDP)	▪ Extender Sublayer (CDXI)? ▪ Chip-to-chip ▪ Chip-to-module ▪ Channels characteristics, including connector for chip-to-module	▪ 400GBASE-Sxx (100m) ▪ 400GBASE-xxx (500m) ▪ 400GBASE-Fxx (2km) ▪ 400GBASE-Lxx (10km) ▪ MDI(s?) ▪ Media characteristics
FEC ARCHITECTURE AND BUDGET	▪ FEC related to electrical interfaces?	▪ FEC related to PMD functions?
▪ Management related to Logic functions (Clauses 30, 45, etc.)	▪ Management related to electrical interfaces (Clauses 30, 45, etc.)	▪ Management related to PMD functions (Clauses 30, 45, etc.)

Timeline for Discussion (Not Approved)



Proposed Key Dates (Not Approved)

Description	Date
Last Proposal	Nov 2014
Complete Baseline Selection (Generate D1.0 out of this mtg)	Jan 2015
Start Task Force Review	Mar 2015
Last Feature	Sep 2015
Request WG Ballot	Nov 2015
Last Technical Change	Mar 2016
Request Sponsor Ballot	Jul 2016
Standard Ratification	Feb 2017