# Investigation of 56Gbps PAM4 based bi-directional architecture for 400GbE

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# Outline

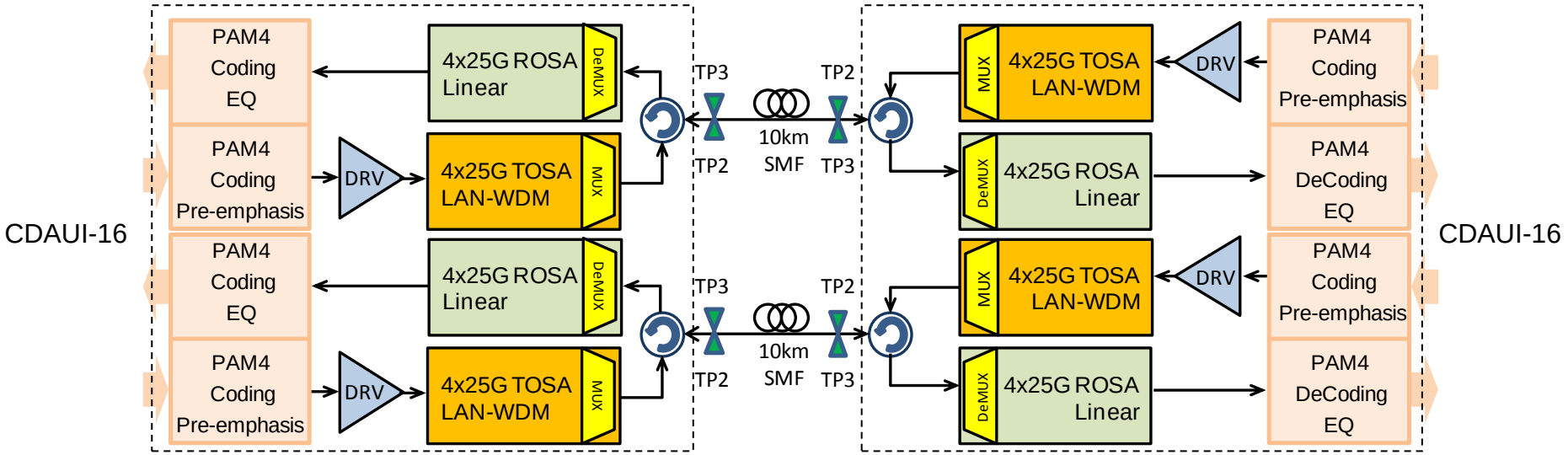
- Background information
- 400GBASE-BLR4 investigation for 10 km PMD
- Characteristics of 400GBASE-BLR4
- TF, EF and BMP of 400GBASE-BLR4

# Background Information

- This presentation will provide a bi-directional 4x56Gbps PAM4 (400GBASE-BLR4) configuration and further investigation results to support the technical feasibility and other criteria of 10 km objective.
- For 10 km SMF PMD, consider the time-to-market for 400GE transceivers, reuse 100GE components (25G-class optical and electrical device) will be a promising way.
- For operator networks, **2 km duplex SMF** and certainly **10 km duplex SMF** are the first priority.
  - Initial market demand can tolerate 10km SMF in 2km applications so prioritize 10km first.

# PAM4 based bidirectional architecture for 10 km SMF PMD

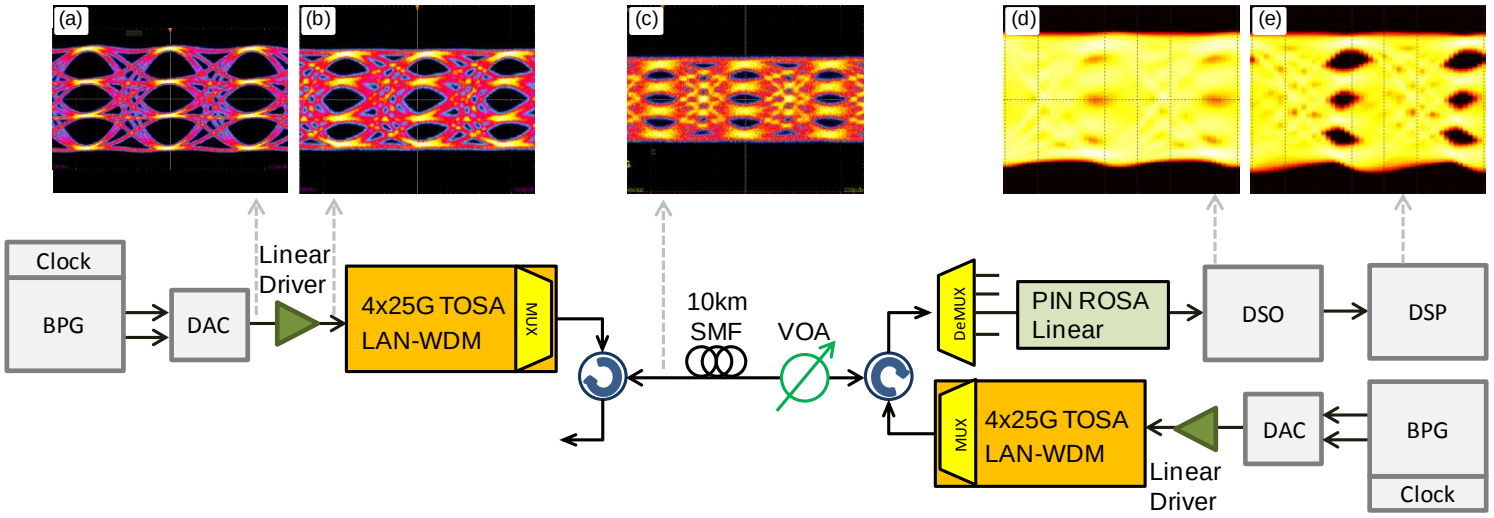
Bi-directional 4x56Gbps PAM4 Solution




- Bi-direction scheme has been investigated with two sets of LAN-WDM devices, no extra wavelengths are required beyond existing 100GBASE-LR4.
  - Allows re-use of existing LR4 filters/muxes.
- The 25Gbps optical and electrical devices required in this solution are currently available.
- The PAM4 Coding/Decoding, equalization as well as FEC are required.

# Experimental Demonstration of Bi-Di 4x56G PAM4 for 10 km

## Experimental setup of Bi-Di 4x56Gbps PAM4 scheme




**Transmitter:**

TOSA: 4x25Gbps EML, 20GHz BW, 6.5dB ER

Driver: 25Gbps linear driver, 20GHz BW

Circulator: O-band, <1dB insertion loss

DAC: SHF 611B

**Receiver:**

ROSA: 25Gbps PIN ROSA

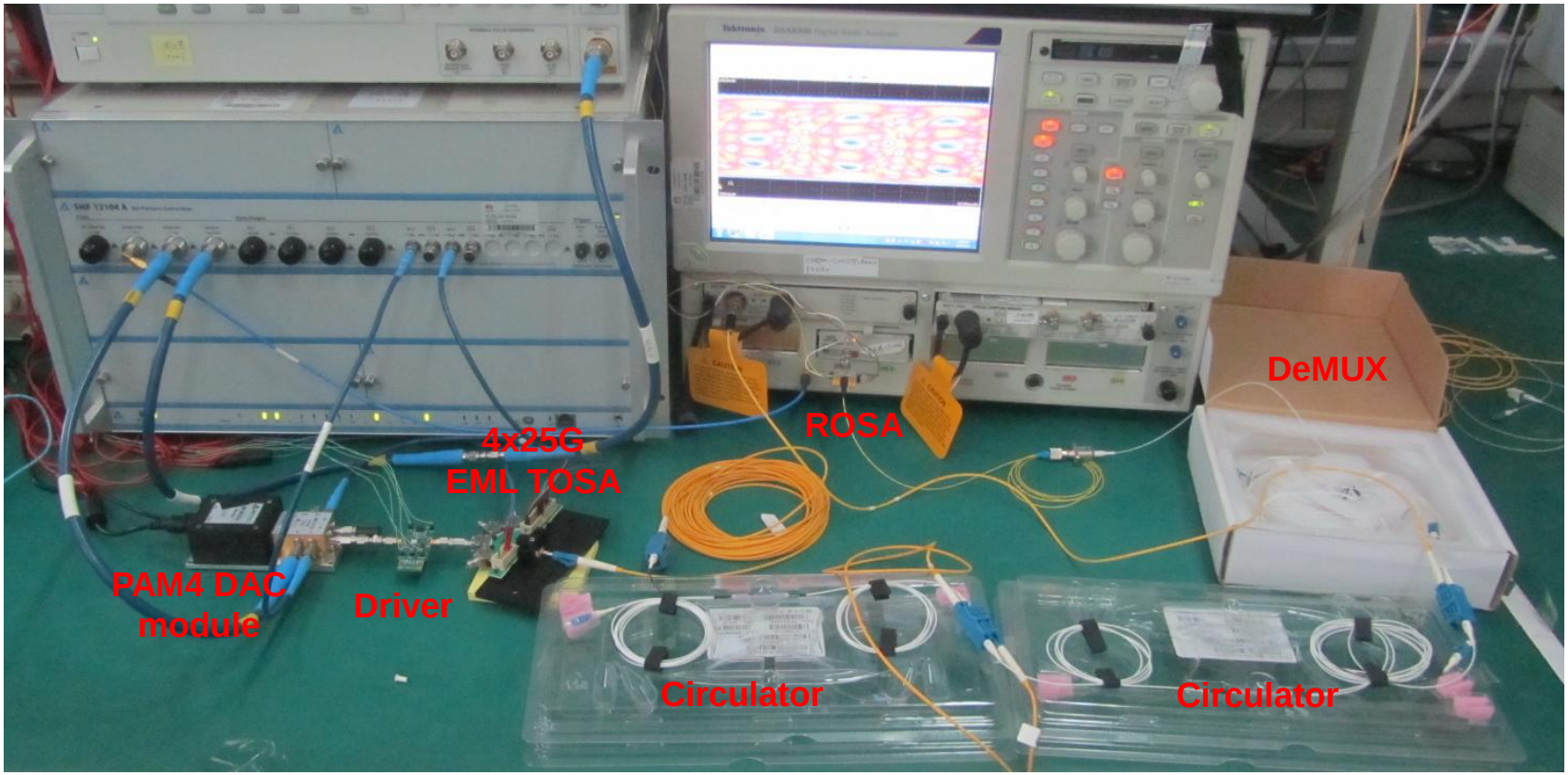
Circulator: O-band, <1dB insertion loss

DeMUX: LAN-WDM, <1.5dB insertion loss

Equalization: FFE (off-line)

# Experimental Demonstration of Bi-Di 4x56G PAM4 for 10 km

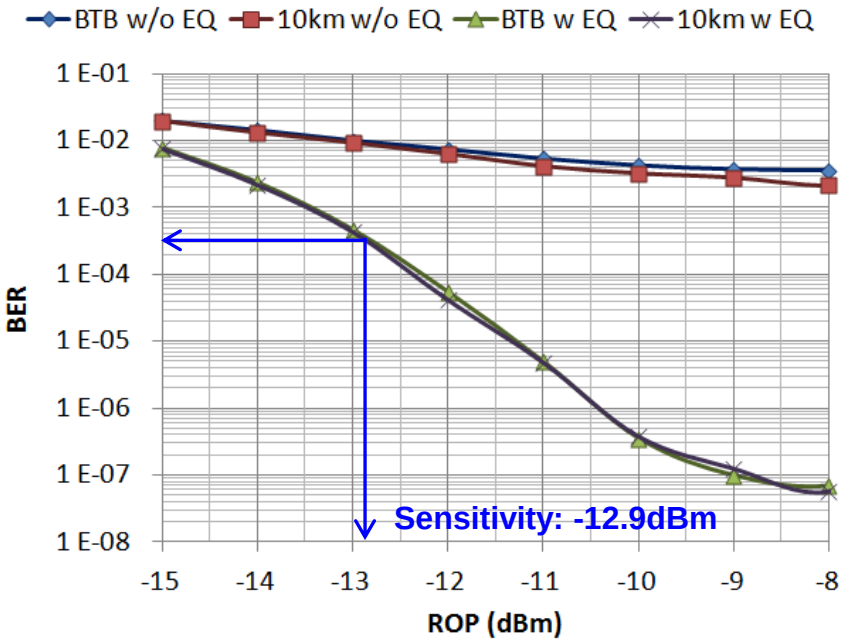
## Experimental setup

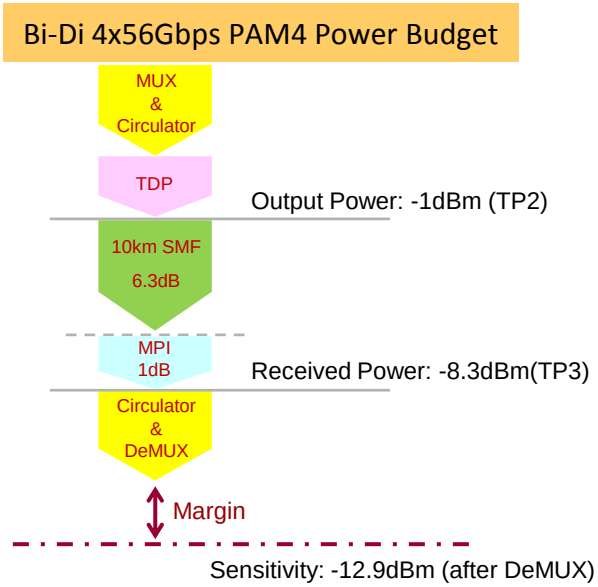



- The experiment was carried out by the discrete devices and offline DSP.

# Experimental Demonstration of Bi-Di 4x56G PAM4 for 10 km

## BER test results and power allocation

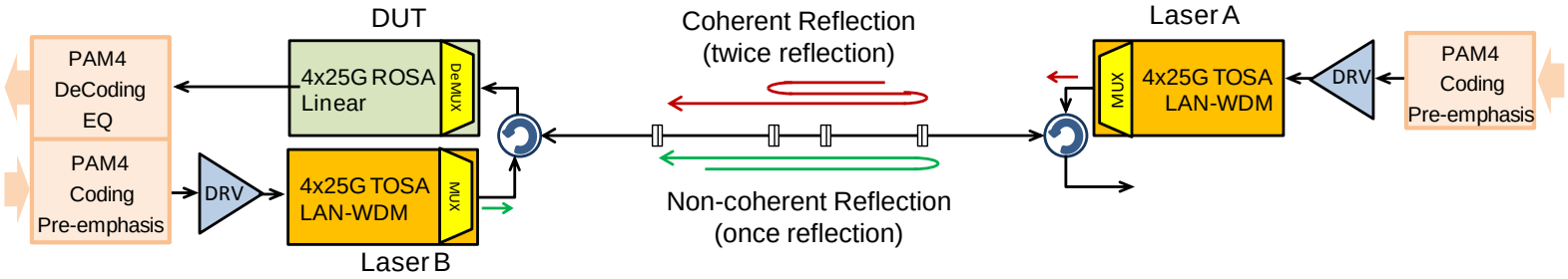


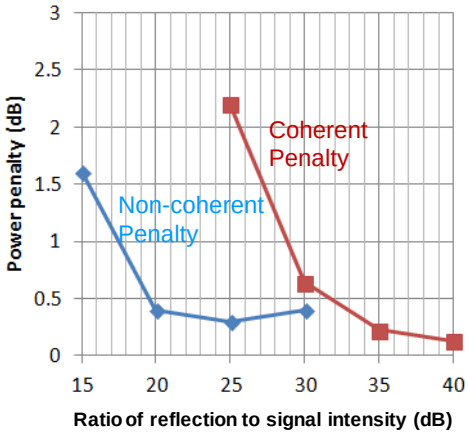

- Bi-directional 56Gbps PAM4 experiment has been carried out over 10 km SMF off-line.
- -12.9dBm sensitivity (@3E-4 BER) have been achieved with FFE/DFE equalization after optical DeMUX (including TDP).
- The RS FEC (100GBASE-KP4) is needed to satisfy BER requirement of 1e-13.
- The power budget may include the channel insertion loss, TDP and the penalty of MPI.

# Experimental Demonstration of Bi-Di 4x56G PAM4 for 10 km

## Multi-Path Interference Analysis




Here MPI is defined as the ratio of coherent and non-coherent reflection to signal intensity, and the penalty is listed as below.




4 Connectors Penalty

| Connector RL (dB) | Non-coherent Penalty (dB) | Coherent Penalty (dB) | Total Penalty (dB) |
|---|---|---|---|
| 26 | 0.4 | 0.1 | 0.5 |
| 30 | 0.3 | <0.1 | <0.4 |
| 35 | 0.3 | <0.1 | <0.4 |

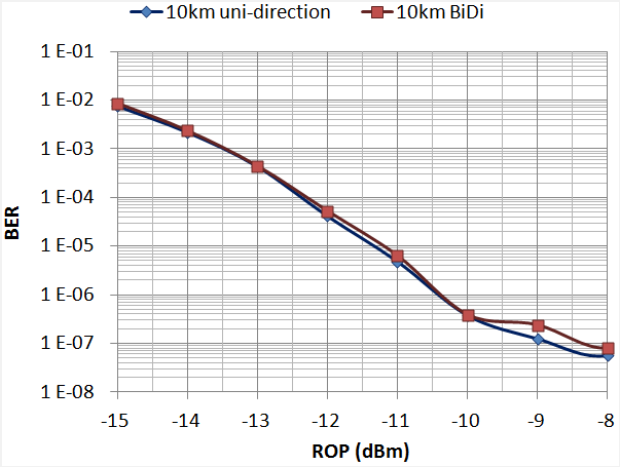
6 Connectors Penalty

| Connector RL (dB) | Non-coherent Penalty (dB) | Coherent Penalty (dB) | Total Penalty (dB) |
|---|---|---|---|
| 26 | 0.8 | 0.1 | 0.9 |
| 30 | 0.35 | <0.1 | <0.45 |
| 35 | 0.35 | <0.1 | <0.45 |

Evaluated with same wavelength and same output power.

The penalty of MPI should be considered and it may be compensated by DSP solution.

## Laboratory Test




No obvious penalty can be observed when connector return loss is more than 40dB.

# Characteristics of 400GBASE-BLR4

| | Description | 400GBASE-BLR4 | Unit |
|---|---|---|---|
| **Transmitter** | Signaling rate, each lane (range) | 28±100ppm(TBD) | GBd |
| | Lane wavelengths (range) | 1294.53 to 1296.59<br>1299.02 to 1301.09<br>1303.54 to 1305.63<br>1308.09 to 1310.19 | nm |
| | Optical Modulation Amplitude (OMA), each lane (max) | 4.5 | dBm |
| | Optical Modulation Amplitude (OMA), each lane (min) | -0.3(TBD) | dBm |
| | Launch power in OMA minus TDP, each lane (min) | -1 | dBm |
| | Transmitter and dispersion penalty (TDP), each lane (max) | 2 (TBD) | dB |
| | Extinction ratio (min) | 6(TBD) | dB |
| | RIN(TBD)OMA (max) | -143(TBD) | dB/Hz |
| | SNR | 25 (TBD) | dB |
| **Receiver** | **Description** | **400GBASE-BLR4** | **Unit** |
| | Receiver reflectance (max) | -35 (TBD) | dB |
| | Receiver sensitivity (OMA), each lane (max) | -8.3 (TBD) | dBm |
| **Link Power** | **Description** | **400GBASE-BLR4** | **Unit** |
| | Power budget (for maximum TDP) | 9.3 (TBD) | dB |
| | Operating distance | 10 | km |
| | Channel insertion loss | 6.3(TBD) | dB |
| | Allocation for penalties (for maximum TDP) | 2 (TBD) | dB |
| | MPI | 1 (TBD) | dB |

# Cost & Power Consumption Evaluation

Relative Cost Estimation

| Solutions | 4x25Gbps NRZ | Bi-Di 4x56Gbps PAM4 | Notes |
|---|---|---|---|
| Relative Cost of TOSA | 1.0 | 1.9 | EML required will be 2x and can be integrated further. |
| Relative Cost of ROSA | 1.0 | 2.8 | PIN and TIA required will be twice and the TIA is needed to be changed to 25Gbps linear one. |
| Relative Cost of IC | 1.0 | 2.6 | IC here includes the 25GBd linear driver and 56Gbps PAM4 to 2x28Gbps converter. |
| Relative Total Cost | 1.0 | 2.3 | The relative total cost including TOSA, ROSA and IC. |

Power Consumption Evaluation

| Devices | 4x25Gbps NRZ | Bi-Di 4x56Gbps PAM4 | Notes |
|---|---|---|---|
| TOSA/ROSA | 3 W | 6 W | TOSA/ROSA power consumption should be twice of that in CFP4, and it can be integrated further as a BOSA. |
| Driver | 1 W | 2 W | Driver power is twice of that in CFP4 with linear version. |
| Gearbox/CDR/DSP | 1 W | 6 W | The PAM4 PHY chip may be ADC based with 8 channel and estimated based upon existing 25Gbps 28nm PAM4 PHY chips. |
| Other | 0.5 W | 1 W | Including the DC source and controller circuit. |
| Total | 5.5 W | 15 W | The total power is less than 24W and can be optimized to 12W. |

- Bi-directional 4x56Gbps PAM4 solution achieves technical complexity (time-to-market) balance with low cost.
- The total power consumption can meet the power requirement of CFP and can be optimized further to CFP2.

# Summary

- Leveraging current 100GBASE-LR4 components (25G-class optical and electrical device) and based upon the BJ's FEC (KP4), Bi-Di 4x56G PAM4 configuration is a cost-effective time-to-market solution for 10 km SMF.
- The approach uses 25GBd devices with mature technology nodes and more readily available industry supply chain.
- From the test results, the technical feasibility is demonstrated using current commercial components, 400GBASE-BLR4 is a promising method for 10km SMF objective, it is a reasonable time-to-market solution.
- The solution for reflection penalty needs to be further investigated.

# Thank you