Technical Feasibility Study of 56Gb/s and 112Gb/s PAM-4 Transmission

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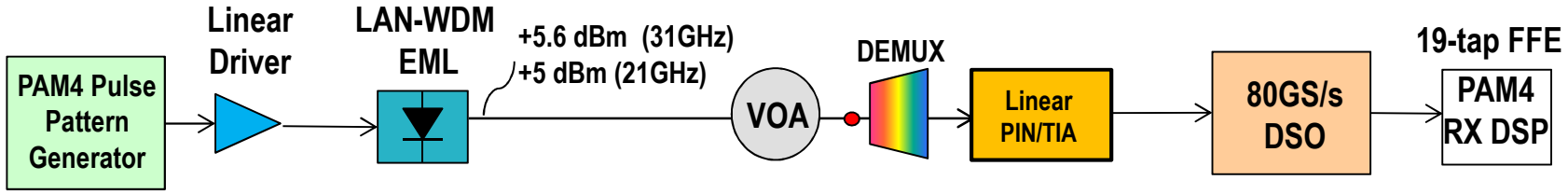
Objectives

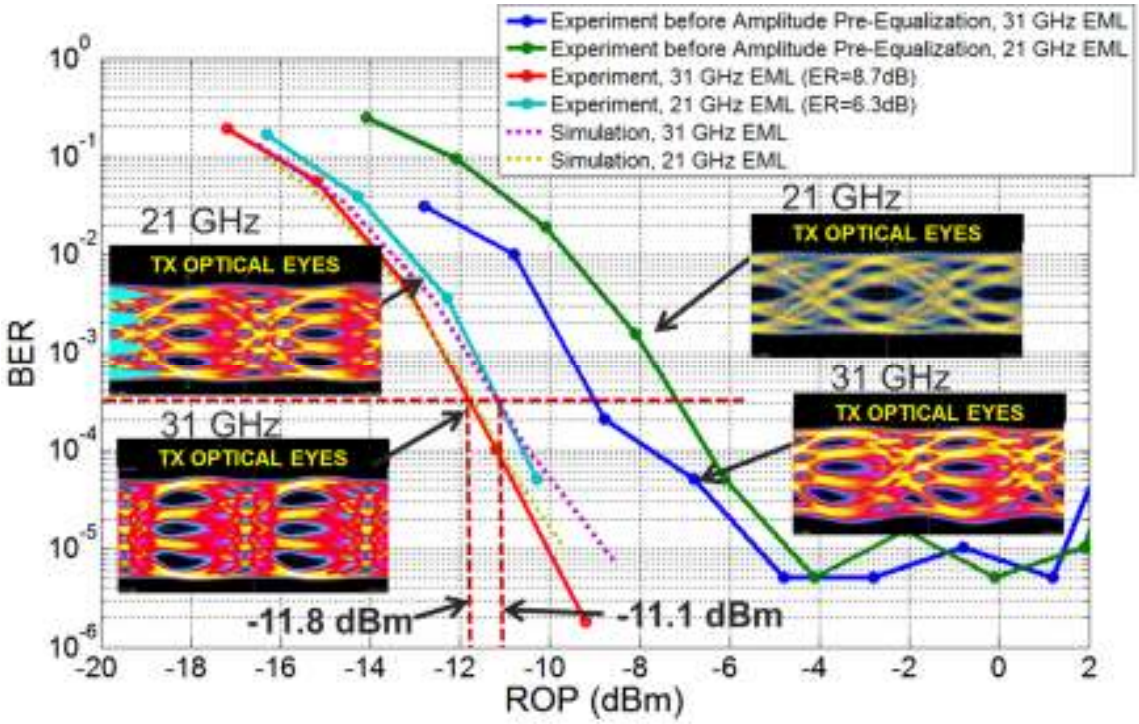
- Investigate the requirement of a DAC for an optimized 56Gb/s PAM-4 transmission performance
- Build a simulation model which can match with 56Gb/s experimental results, and predict 112 Gb/s PAM-4 performance
- Investigate the impact of SOA on 56Gb/s PAM-4 link power budget and its implication on 112Gb/s PAM-4

Review of EML-based 56Gb/s PAM-4 Experiments

Reference	Link distance	Link budget w/o WDM (=(a)-(b))	EML output power (a)	Received optical power @ 3e-4 (b)	Extinc-tion ratio	2-bit DAC BW	Driver Amp BW	EML BW	RX 3-dB BW	Error Detection and Equalizer
Schell_01_0712_optx	10 km	--	--	--	5.7dB	--	--	--	--	--
Xu_400_01a_0114	10 km	17.3dB	+6dBm	-11.3 dBm	9dB	13GHz	18GHz	17GHz	20GHz	Error Analyzer DFE (No. taps=1)
Man_3bs_01_0514	10 km	12.9dB	+0dBm	-12.9 dBm	6.5~ 7dB	19GHz	20GHz	21GHz	20GHz	160 Gsps DSO (analog BW=63GHz), FFE (No. taps=31)
Bhoja_3ba_01_0514	10km	14dB	+4dBm	-10dBm	>6dB	19GHz	25GHz	21GHz	28GHz	80GS/s DSO (analog BW=30GHz), FFE (No. taps=10)

56Gb/s PAM-4:
Use Pulse Pattern Generator with adjustable voltages





56Gb/s PAM-4 Simulation Parameters		
Parameter	Value	Unit
Bit rate	56	Gb/s
SNR before EML	21	dB
EML BW (1st-order Bessel)	21 or 31	GHz
Linear driver amp BW (1st-order Bessel)	32	GHz
ER	6.3 or 8.7	dB
Wavelength	1310	nm
RIN	-145	dB/Hz
Receiver input spectral noise density	25	pA/√Hz
PD + TIA BW (1st-order Bessel)	22	GHz
Number of FFE taps	19	
ADC bandwidth (5th-order Bessel)	25	GHz

- Pre-equalize three eye amplitudes can improve BER significantly
- 31GHz vs 21GHz EML: Receiver sensitivity improvement ~ 0.7 dB, mainly due to ER difference
- Simulation and experimental results match well

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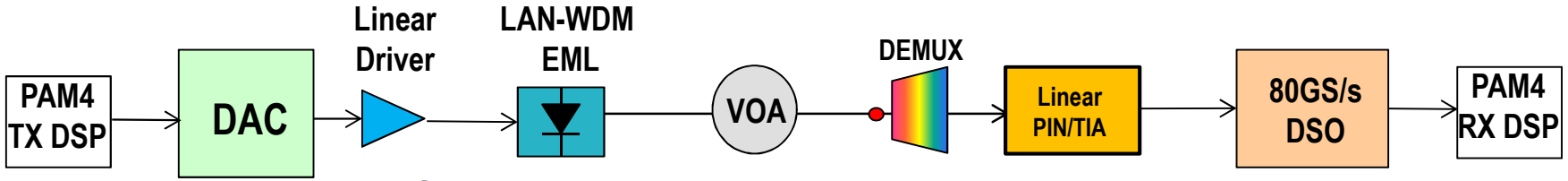
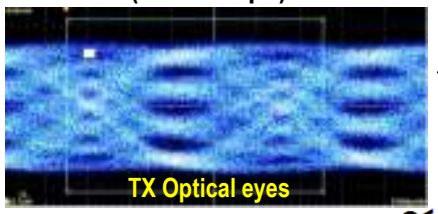
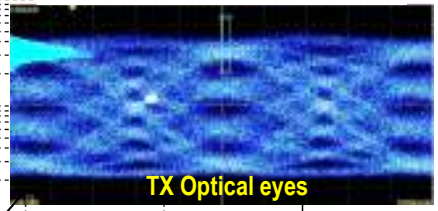
56Gb/s PAM-4:
Use 13GHz & 65Gs/s DAC (ENOB~ 4.5bits)



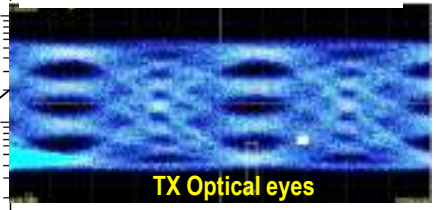
31 GHz, ER: 7.3 dB
(Rx: 19 taps)



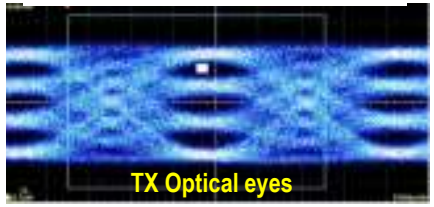
21 GHz, ER: 5.7 dB
(Rx: 19 taps)



21 GHz, ER: 5.4 dB
(Tx: 5 taps, Rx: 19 taps)

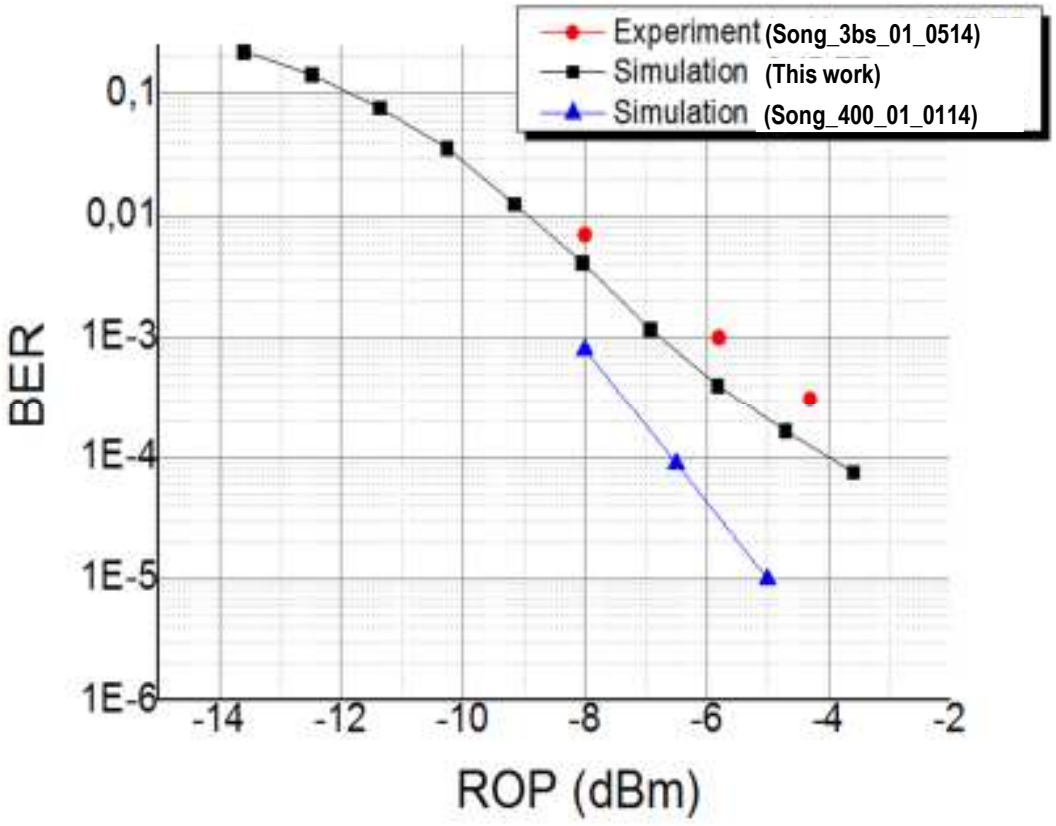


31 GHz, ER: 6.5 dB
(Tx: 5 taps, Rx: 19 taps)



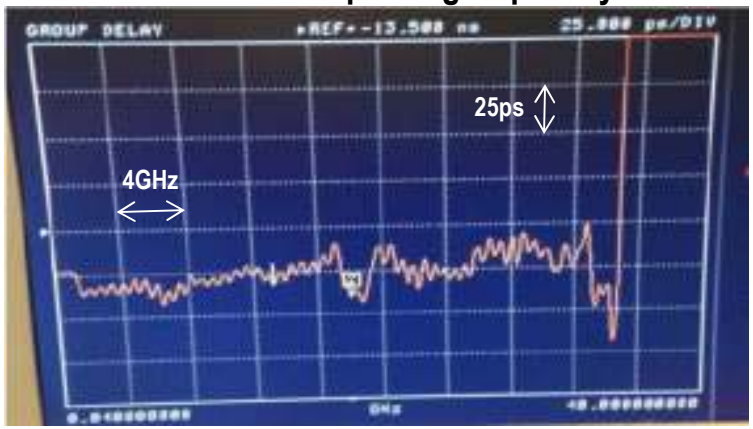
- (RX only FFE) has a worse RX sensitivity than that of (TX + RX FFE) by <0.9dB
- (Limited DAC-bandwidth + (TX+RX FFE)) has a worse RX sensitivity than that of (PPG + RX FFE)
- ER degraded by TX pre-emphasis

112 Gb/s PAM-4: Simulation Results



112 Gb/s PAM-4 Simulation Parameters		
Parameter	Value	Unit
Bit rate	112	Gb/s
SNR before EML	21	dB
EML BW (1st-order Bessel)	32	GHz
Linear driver amp BW (1st-order Bessel)	32	GHz
ER	6	dB
Wavelength	1310	nm
RIN	-145	dB/Hz
SSMF distance	2	km
Receiver input spectral noise density	40	pA/√Hz
PD + TIA BW (1st-order Bessel)	32	GHz
Number of FFE taps	11	
ADC bandwidth (5th-order Bessel)	33	GHz

Measured 31GHz EML superior group delay variation



- **Receiver sensitivity comparable to 100Gb/s DMT @ BER=1e-3**
- **Effect of group delay still need to be investigated**

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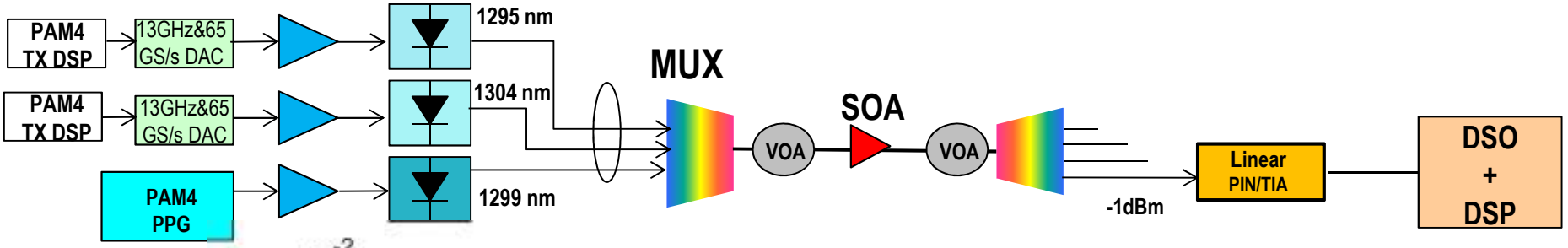
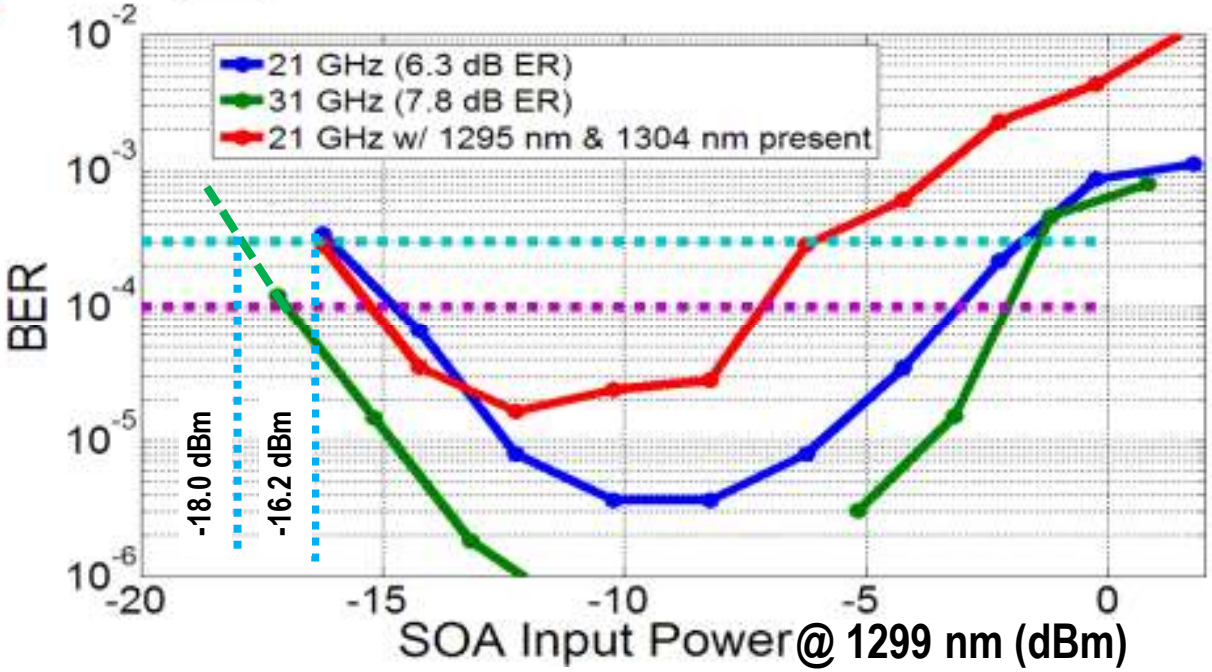
56Gb/s PAM-4 RX sensitivity improvement via SOA





- For 56Gb/s PAM-4, an extra link power budget of 6.6 to 7.7 dB can be achieved, albeit a smaller dynamic range than the case without SOA
- Potential of 112Gb/s PAM-4 RX sensitivity improvement using an SOA
- Same SOA cannot be used to improve the RX sensitivity of a DMT system w/o extra DSP power

Summary

- A 2-bit DAC generating PAM-4 PPG eye quality and with voltage-adjustability on both data streams is preferred to a bandwidth-limited DAC with more effective number of bits
- RX-only FFE should be sufficient
- A PAM-4 chip may have reduced ADC bandwidth and ENOBs in comparing to a DSO, and their effects on link performance require more investigations
- The potential of using SOA to improve the RX sensitivity for 112Gb/s PAM-4 will be investigated