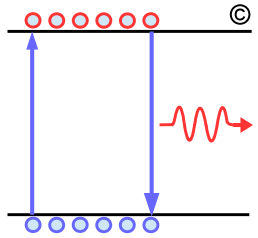


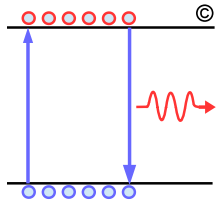
Path to Consensus on 400 GbE PMDs

Ali Ghiasi
Ghiasi Quantum LLC

IEEE 802.3bs Task Force

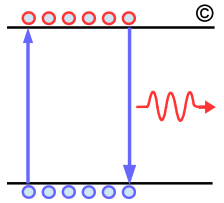
July 2014

Current 802.3bs Objective Per Dallas Meeting



- **Provide physical layer specifications which support link distances of at least 100 m over MMF**
- **Provide physical layer specifications which support link distances of at least 500 m over SMF**
- **Provide physical layer specifications which support link distances of 2 km on SMF**
- **Provide physical layer specifications which support link distances of at least 10 km over SMF**
- **Key questions where consensus need to be developed are:**
  - Do we define in .bs more efficient PMDs?
  - Do we define higher bit rate narrower CDAUI in .bs?

Straw Polls Results from Norfolk

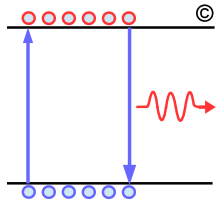


- **There is strong support to define 50 Gb/s short reach electrical interface to get more BW from big ASICs and narrow the module**

Straw Poll #	**2**	
Title	IEEE 802.3bs should target the initial 400GbE electrical chip-to-chip interface to be based on bit-rate per lane of:	
Result	a) 25G	64
	b) 40G	0
	c) 50G	31
	d) 100G	0

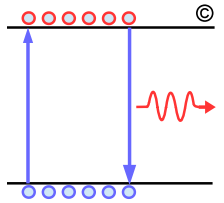
Straw Poll #	**3**	
Title	IEEE 802.3bs should target the initial 400GbE electrical chip-to-module interface to be based on bit-rate per lane of:	
Result	a) 25G	49
	b) 40G	0
	c) 50G	16
	d) 25 & 50G	24

PMD Evolution Options

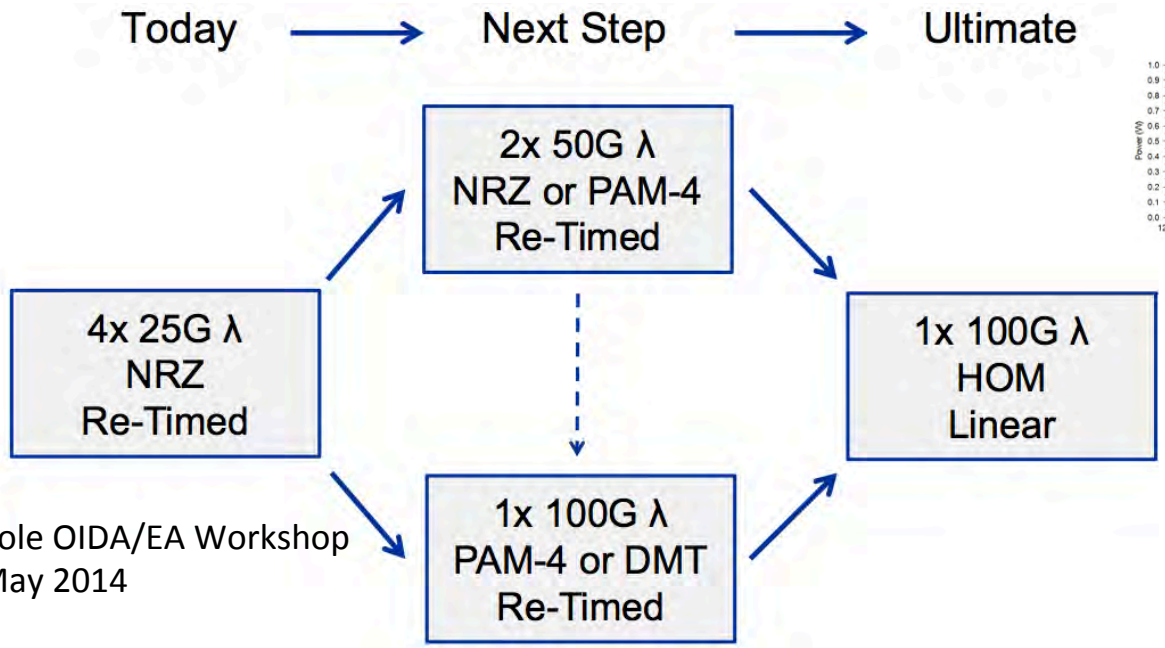


- **Current Gen 16x25G – Signaling NRZ**
  - Advantage: mature technology and reuse
  - Dis-advantages: SR16/PSM16 high cost associated with 32 fibers and CDAUI-16 makes the module too wide, LR16 is high cost effectively a Metro WDM, with migration to CDAUI-8 these PMDs require inverse-mux in the module
- **Next Gen 8x50G – Signaling (NRZ, PAM4, or DMT)**
  - Advantage: Common 50 Gb/s signaling and host based moderate gain FEC ~ 6 dB is sufficient for CDAUI-8, SR8, PSM8, FR8, and LR8 increases supply base, and lowers the cost
  - Disadvantage: Narrower interface eventually would deliver lower cost
- **Ultimate Gen 4x100G – Signaling (PAM4 or DMT)**
  - Advantage: With 4 lasers eventually lower cost could be achieved
  - Disadvantage: Project will take longer, high gain FEC >9 dB would be required, higher BW component such as as MZM/EA needed, VCSEL/DFB-DML may not have sufficient power/BW, and/or more complex DSP required.

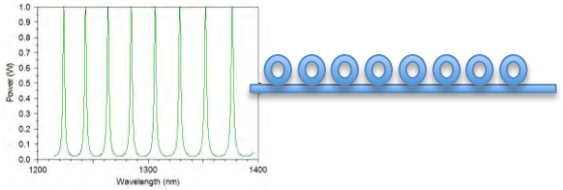
What Should We Aim for?



- **Aiming too low means PMDs defined now would require inverse mux in 2 years and a new PMD!**
- **Standard body should not try to aim for ultimate solution with limited data and under aggressive schedule = just getting it wrong**
- **Standards should be defining next Gen PMDs = just getting it right**

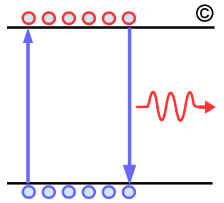


Cole OIDA/EA Workshop
May 2014



Ultimate solution could be an 8λ comb laser with ring Resonator. Ring resonator Have the promise to deliver Highest density, lowest power, and cost optical devices but Somewhat slow ~20 GBd!

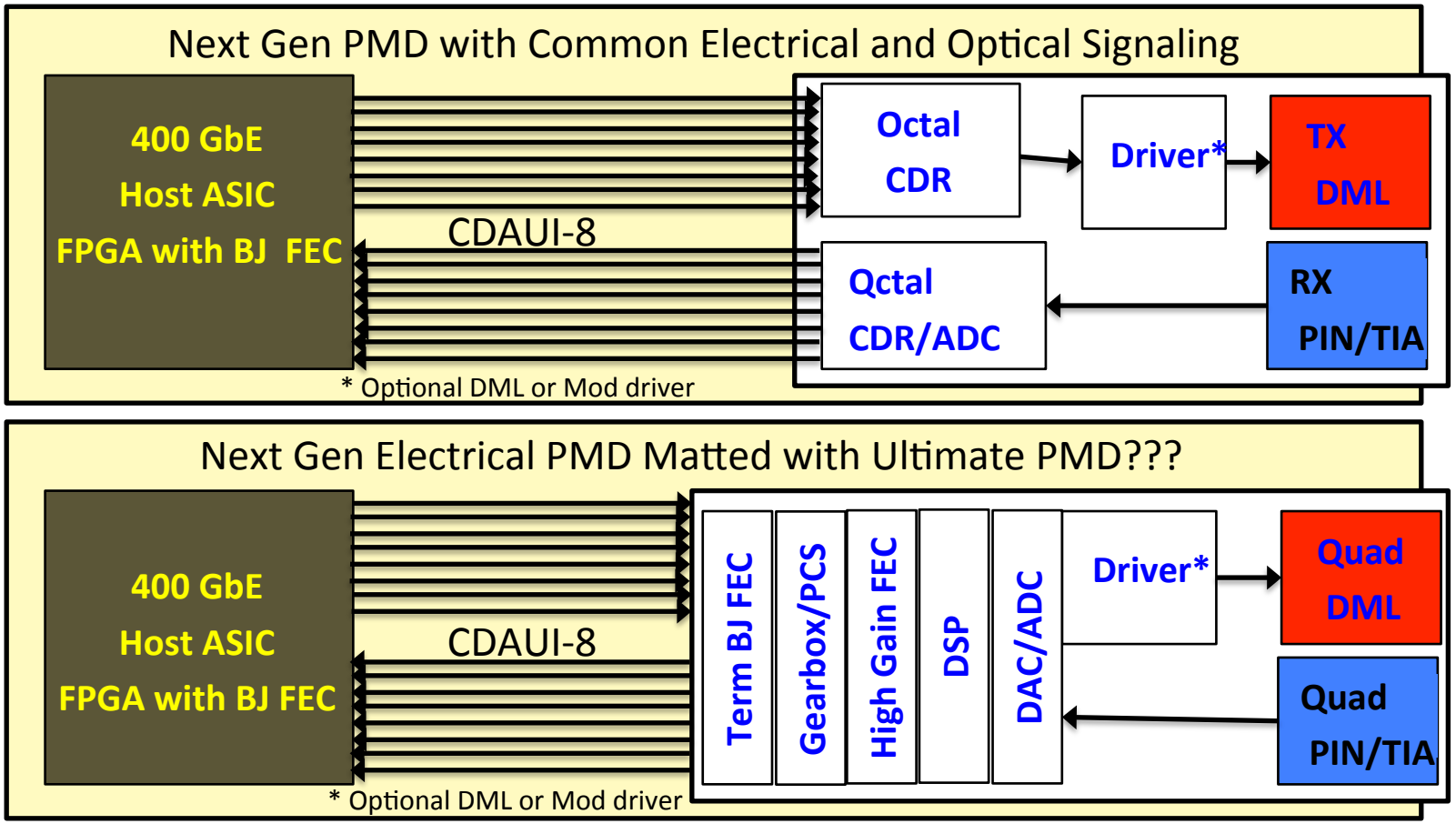
Toward Consensus



- **Trying to standardize 16x25G, 8x50G, and 4x100G all in one project is an enormous undertaking for the BS task force, for component/OEMs to develop the products, and for end user to manage all the deployment and interoperability issues**
- **Here is scenario how 400 GbE could turn into quagmire**
  - SR16 is based on 16x25 Gb/s with BJ FEC
  - PSM8 is based on 8x50 Gb/s with BJ or moderate gain FEC
  - FR4 based on 4x100 Gb/s with high gain FEC
  - LR4 based on 4x100 Gb/s with high gain FEC
- **It is an enormous undertaking to develop 3 different SerDes possibly based on 3 different signaling with 3 different FECs**
- **The industry and IEEE need to focus on the next generation PMDs based on 8x50G for economy of scale, lower cost and for more efficient 400 GbE Interface**
  - Aiming too low and only defining SR16/PSM16 is a disservice to industry
  - Aiming for ultimate solution = making decision based on speculation!

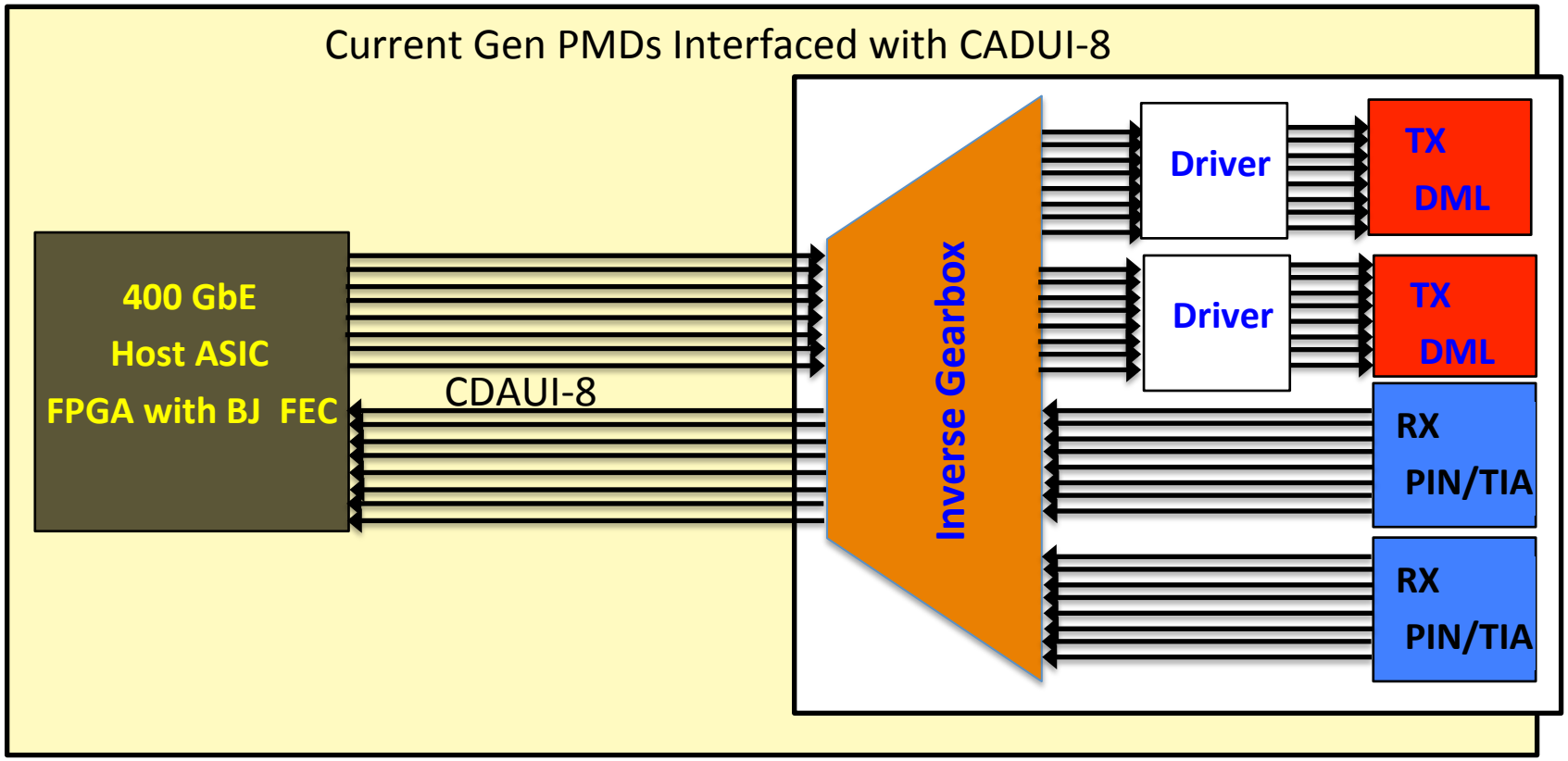
400 GbE PMD Architecture

- **8x50G could create ubiquitous interface similar to todays' 100Gbase-SR4/LR4**
  - Developing 2nd Gen PMD now require more complex DSP, higher gain FEC, high cost, and the solution likely will be sub-optimum than waiting ~ 3 years to develop 100 Gb/s/lane in the next project based on factual research!

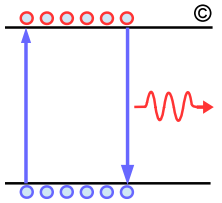


400 GbE PMD Architecture

- **Fortunately in 802.3ae we only defined 16 lanes electrical XSBI which was short lived**
  - Unless VCSELs or PSM can not operate at 50 Gb/s, architecture below need to be avoided at all cost!
  - 100 GbE breakout is not a valid argument to push SR18/PSM16 when 100 GbE PMDs are moving toward narrower lane width!



Natural Evolution of 400 GbE PMDs Cont.



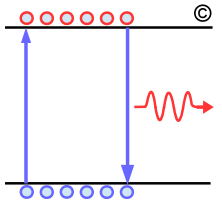
- **In 802.3bs we need to focus on common 50 Gb/s signaling and a common FEC for all optical PMDs**
  - CDAUI-16 could be useful for early adopter but expect to short live just as in the case of XSBI
  - Based on the result of straw poll the task force should define CDAUI-8 and next Gen PMDs
  - Based on the result of Norfolk straw poll OIF is accelerating 56G-VSR/MR project so 802.3bs can use it as starting baseline for CDAUI-8
  - Many questions surround the ultimate Gen PMDs which indicate we have no solid data as ultimate solution could be 8λ comb laser with ring resonators!

PMD	Current (25 Gb/s/lane)	Next Gen (50 Gb/s/lane)#	Ultimate Gen (100 Gb/s/lane)#
CDAUI	CADUI-16	CADUI-8	CADUI-4/8???
100 m MMF	SR-8	SR-8	SR-8+WDM*???
500 m SMF	PSM-8, WDM-8	PSM-8, WDM-8	PSM-4/8 or WDM-4/8???
2 km SMF	WDM-8	WDM-8	WDM-4/8???
10 km SMF	WDM-8	WDM-8	WDM-4/8???

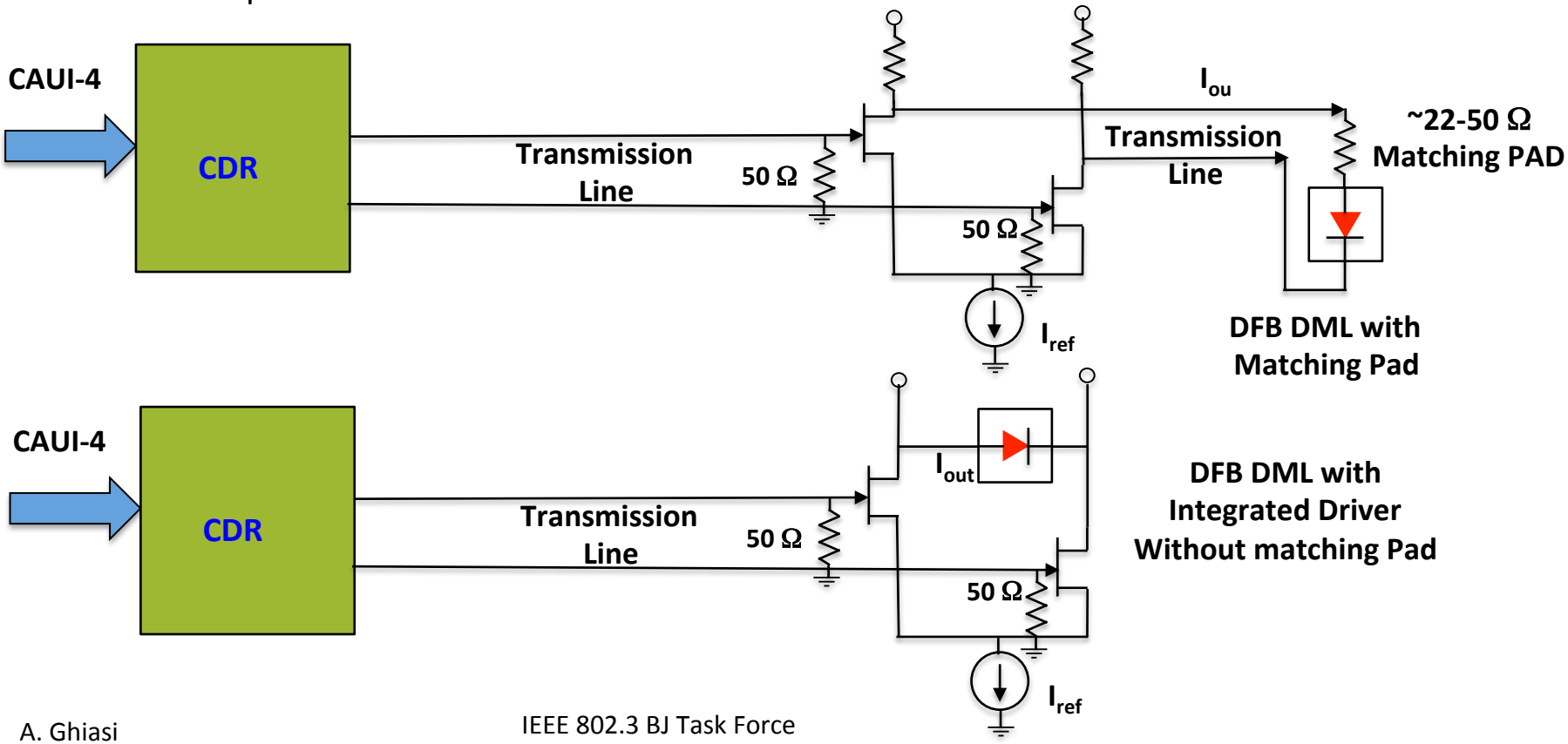
 # Some form of HOM (Higher order modulation is an option)

*** WDM in case of MMF could mean 100+ nm spacing and in case of SMF could mean 100's GHz spacing**

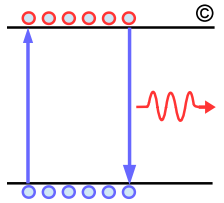
NRZ Driving the Optics



- **If the matching pad was 35 Ω then 70% of power wasted in the pad but giving RL of just 6.3 dB!**
  - Integrated driver can reduce PD and improve RL if the round trip delay is <1/(Baudrate*10)
  - Input stage to LD driver is limiting where amplitude rippled are clipped and signal is sharpened



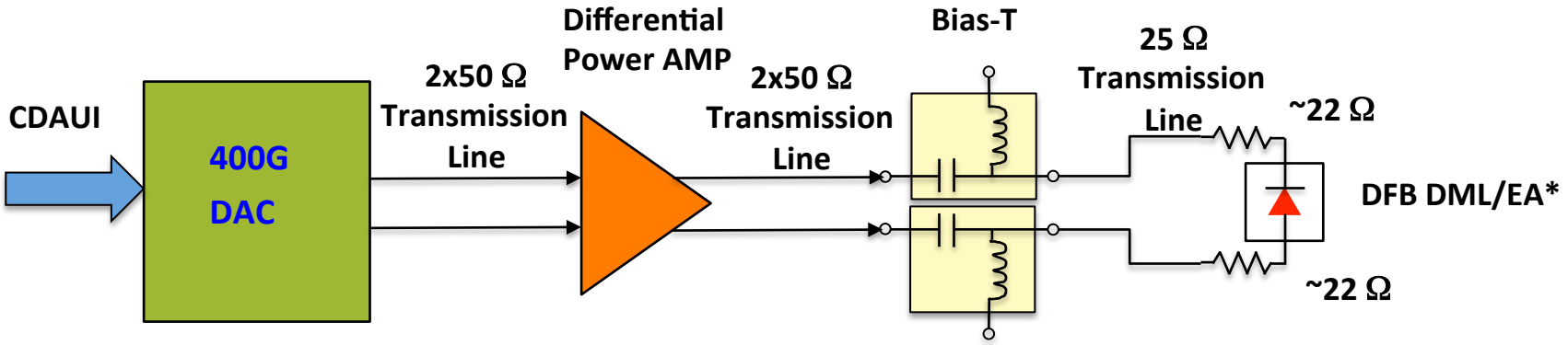
Challenges of HOM Driving Optics



- **The single biggest drawback of moving from NRZ to HOM (Higher Order Modulation) brings is the complexity associated with driving the optics**
- **A large SOC like DAC is not a candidate for integration into a TOSA**
  - Forces the interface between the DAC, TOSA, and intermediary power AMP all to be 50 Ω transmission lines which increases power
  - HOM may require better match than 6.3 dB illustrated on previous page to something more like 12-16 dB
- **On the receiver side linear TIA has some added complexity but the issue is more manageable**
- **Moving from NRZ to HOM adds significant complexity and power to the driving optics**
  - Driving the optics become even more complex with HOM and should be one of the key consideration in selecting an HOM
  - Next will examine complexity of driving HOM optics.

HOM Transmitter Option-I

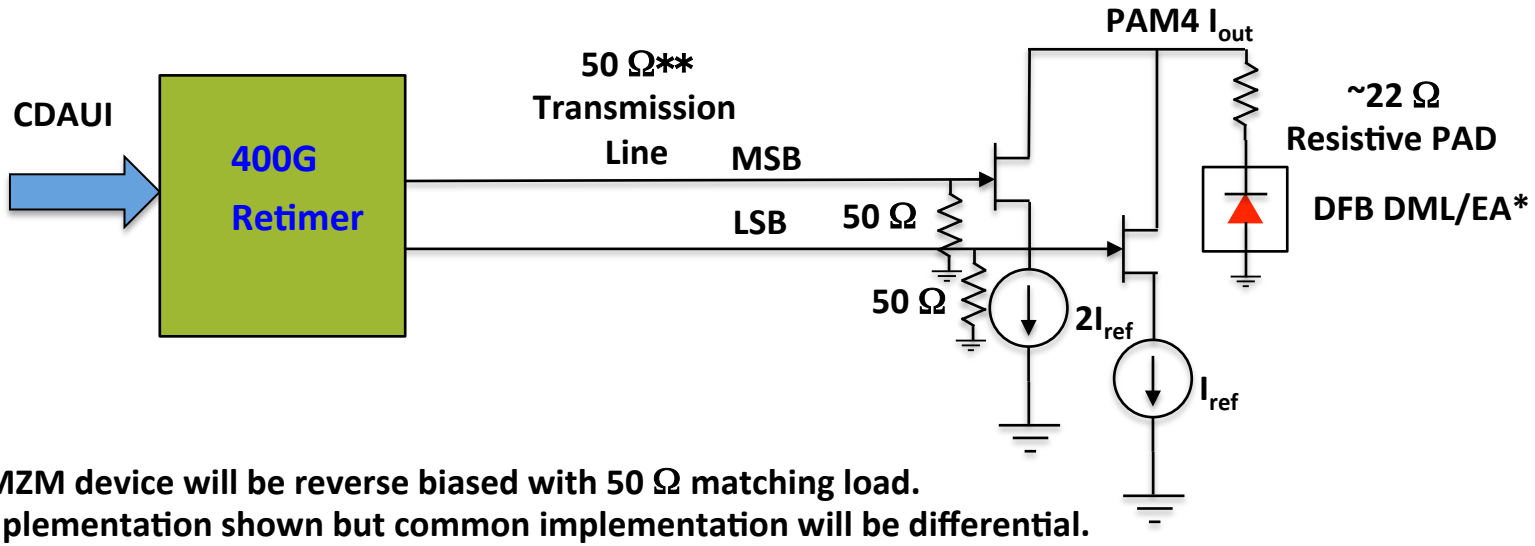
- **Classic implementation DAC driving power AMP**
  - 7-8 bits DAC in case of DMT
  - 5-6 bits DAC in case of PAM-4
  - High cost, high power, and require bulky Bias-T
  - 50 Ω transmission line and resistive matching burns significant power



*** In case of EA or MZM device will be reverse biased with 50 Ω matching load.**

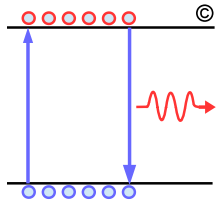
HOM Transmitter Option-II

- **Directly drive the optics with 2 bit DAC**
  - DMT can not take advantage
  - Excellent approach for PAM4
  - Potentially lower power, cost, bulky Bias-T could be eliminated
  - If the round trip delay between driver and optics <1/(Baudrate*10) then optics is treated as a lumped load with resistive pad eliminated resulting in significant power saving!

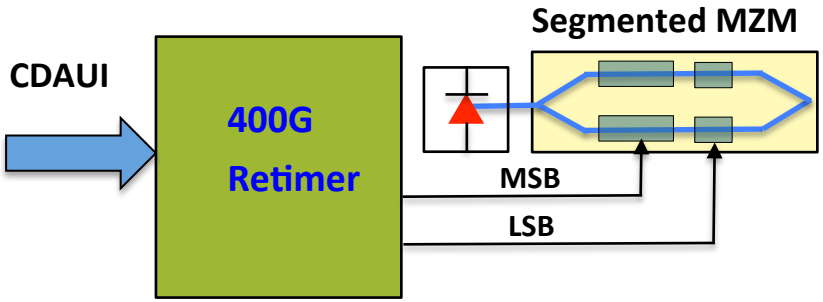


*** In case of EA or MZM device will be reverse biased with 50 Ω matching load.**
**** Single ended implementation shown but common implementation will be differential.**

HOM Transmitter Option-III



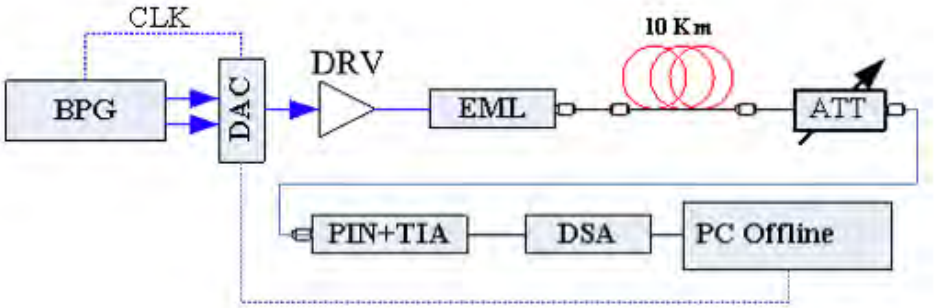
- **Segmented MZM acting as 2 bits DAC**
  - DMT can not take advantage
  - Excellent approach for PAM4
  - Potentially lowest power, cost, and bulky Bias-T eliminated
  - With 50Ω transmission lines eliminated and associated resistive matching there is potential for significant power saving
    - But require advance 2.5D packaging such as TSV or Cu Pillars
    - Not an option for VCSELs or DMLs



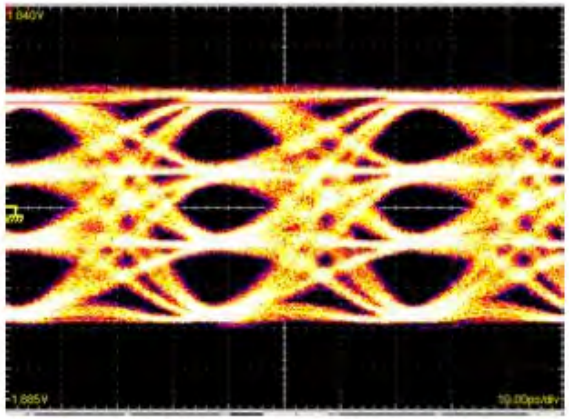
*** In case of EA or MZM device will be reverse biased with 50 Ω matching load.**

Feasibility of PAM4 Driven by 2 Bit Mux

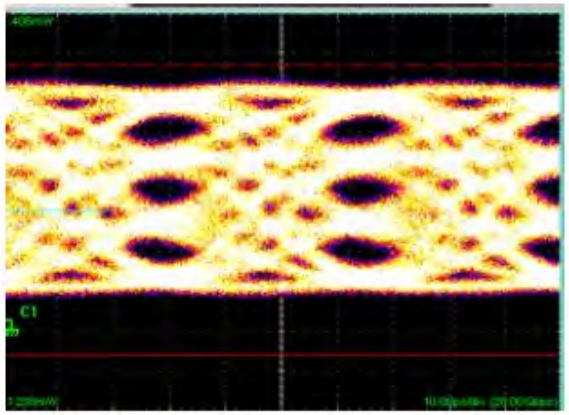
- **Example PAM4 modulation driven with 2 bit Mux at 50 Gb/s**



Experimental Setup



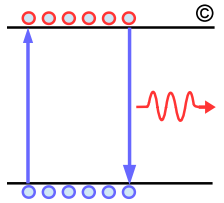
Eye diagram after driver



Eye diagram after EML

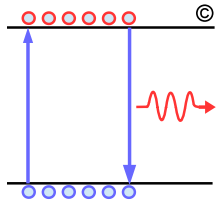
Refer: way_3bs_01a_0514

PAM4 Receiver Options



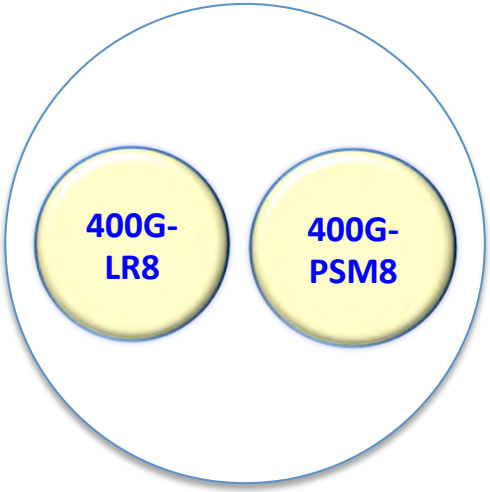
- **CTLE – Simple and low power**
  - Analog receiver
  - Can provide 10-15 dB of peaking
  - Main application moderate loss VSR/SR Cu channel
- **CTLE+DFE – Due to PAM DFE complexity likely only 1 tap DFE will be implemented**
  - ADC receiver (CTLE implemented in frontend analog VGA)
  - May not be as optimum EQ for optical channel
  - Main applications lossy FR4 backplanes
- **CTLE+FFE – Good performance and complexity**
  - ADC receiver (CTLE implemented in frontend analog VGA)
  - Better EQ for optical channels
  - Optionally 1+D (DFE like pre-coder) can be added to the TX.

Our Mantra "Common Signaling"

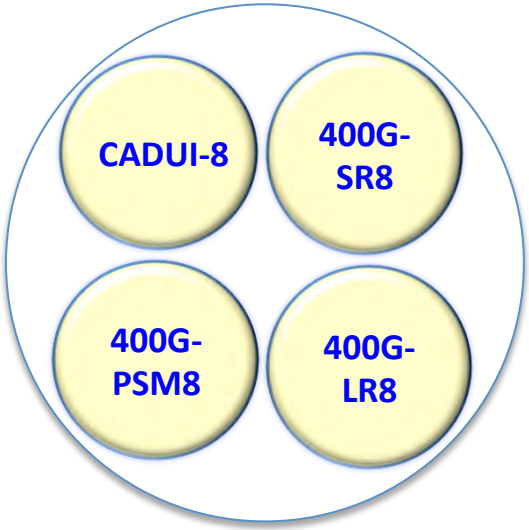


- **PAM4 at 50 Gb/s is suitable to be the common signaling for all PMDs in 802.3bs**
  - NRZ does not provide sufficient reach for 400G-SR8 and CDAUI-8
  - PAM4 at 100 Gb/s not an ecosystem solution and feasibility of 400G-SR4 is questionable
  - DMT does not offer light weight interface to address chip-chip/chip-module CDAUI-4 applications

NRZ 50 Gb/s



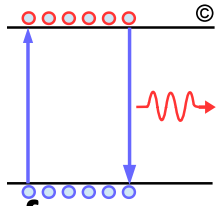
PAM4 50 Gb/s



PAM4 100 Gb/s

DMT 100 Gb/s

Summary



- **In 802.3bs need to focus on a set of PMDs meeting objective of the task force**
  - OIF is now actively developing 56G-VSR (CDAUI-8), 802.3bs should leverage this effort instead of relying on cumbersome CDAUI-16 as the only option
- **802.3bs objective for PMD reaches of 100 m, 500 m, 2 km, and 10 km can be address several ways**
  - Based on current Gen technology such as SR16/PSM16/FR16/LR16
    - All implementation based on CADUI-8 require costly inverse Gearbox in the module
    - Cable cost and/or number of source makes the solution impractical
  - Next Gen based on 50 Gb/s/lane does require some level of development
    - But it could deliver a solution that can address all PMDs SR8/PSM8/FR8/LR8 and CDAUI-8
  - Next-next "Ultimate" Gen 100 Gb/s require significant amount of development
    - It will take longer to develop and will require more costly optics such as MZM and EA
    - Devices such as DFB-DML, VCSELs, and ring resonators likely won't have the BW
    - May end up with multiple HOM SerDes and FEC
    - IEEE 802 will end making decision based on speculation than fundamental research
- **Our mantra should be "Common Signaling – Common FEC"**
  - 50 Gb/s PAM4 can offer common signaling for Cu and all optical PMDs
  - 100 Gb/s PAM4 not an option for 100 Gb/s SR4 or CDAUI-4
  - DMT overly complex for CDAUI links and require DAC with high power AMP to even drive a simple VSR link!