400GbE MII Baseline Proposal

IEEE P802.3bs 400 Gb/s Ethernet Task Force

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Mark Gustlin – Xilinx

Supporters

- John D’Ambrosia – Dell
- Arthur Marris – Cadence
- Dave Ofelt – Juniper
- Steve Trowbridge - ALU

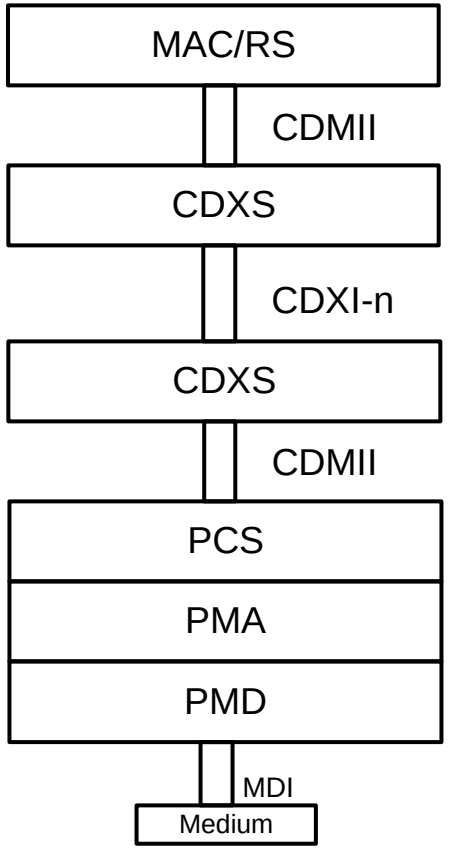
Proposed 400GbE Architecture

- The protocol stack diagram shows one possible implementation
- The CDMII connects the MAC/RS sublayer to the Extender sublayer or the PCS

CDMII is the 400 Gb/s Media Independent Interface

CDXS is the 400 Gb/s extender sublayer

CDXI is the interface between two extender sublayers



CDMII Interface

- Why define it?
  - Electrically it won't be directly instantiated, but in the proposed 400GbE architecture it can be extended with an extender sublayer (CDXS) and interface (CDXI-n)
  - Some will want it for RTL to RTL connections within devices
- Define it as a logical Interface only
  - Unless it is extended, then there is a physical instantiation via an extender sublayer

What is it?

- Base it directly on clause 81
- Same signal structure as shown below, just run faster, or in parallel

81.1.6 XLGMII/CGMII structure

The XLGMII/CGMII is composed of independent transmit and receive paths. Each direction uses 64 data signals (TXD<63:0> and RXD<63:0>), 8 control signals (TXC<7:0> and RXC<7:0>), and a clock (TX_CLK and RX_CLK). Figure 81–2 depicts a schematic view of the RS inputs and outputs.

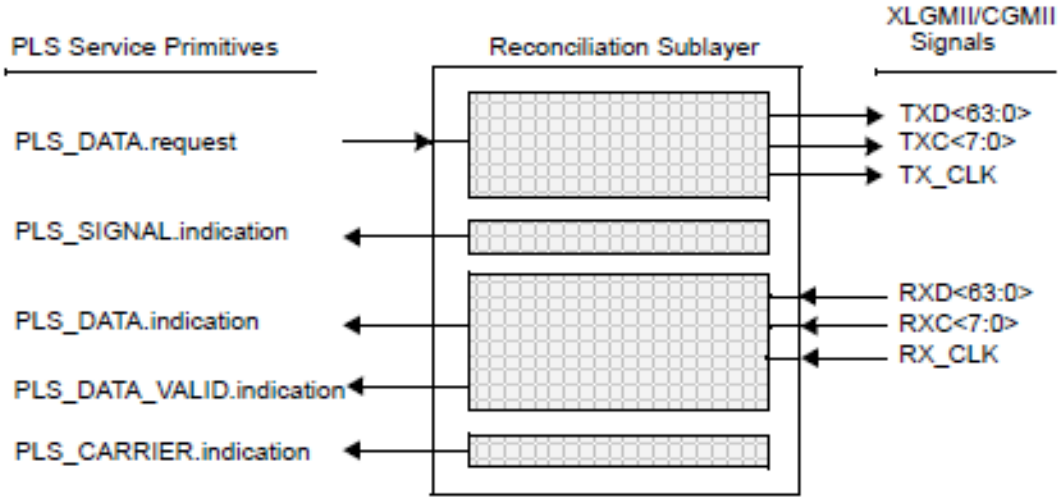


Figure 81–2—Reconciliation Sublayer (RS) inputs and outputs

Extender Sublayer (CDXS)

- The CDXS is the proposed extender sublayer to extend the CDMII
  - A typical instantiation is a high speed parallel SerDes interface
- It is optional, only used if the PCS does not cover both the electrical and optical interface needs
- The CDXS can contain PCS, FEC, and PMA functionality

Thanks!