FOM Bit Mux, Architecture, Challenge and Solution

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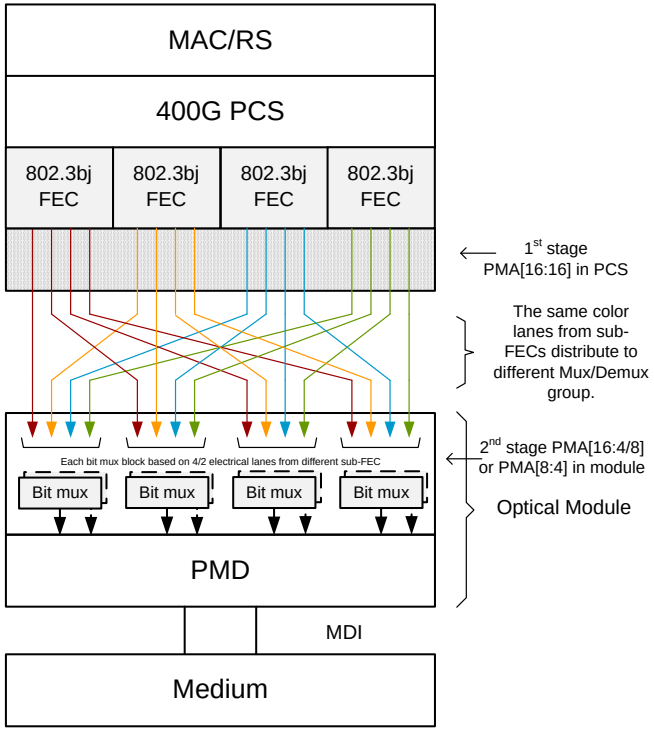
Background

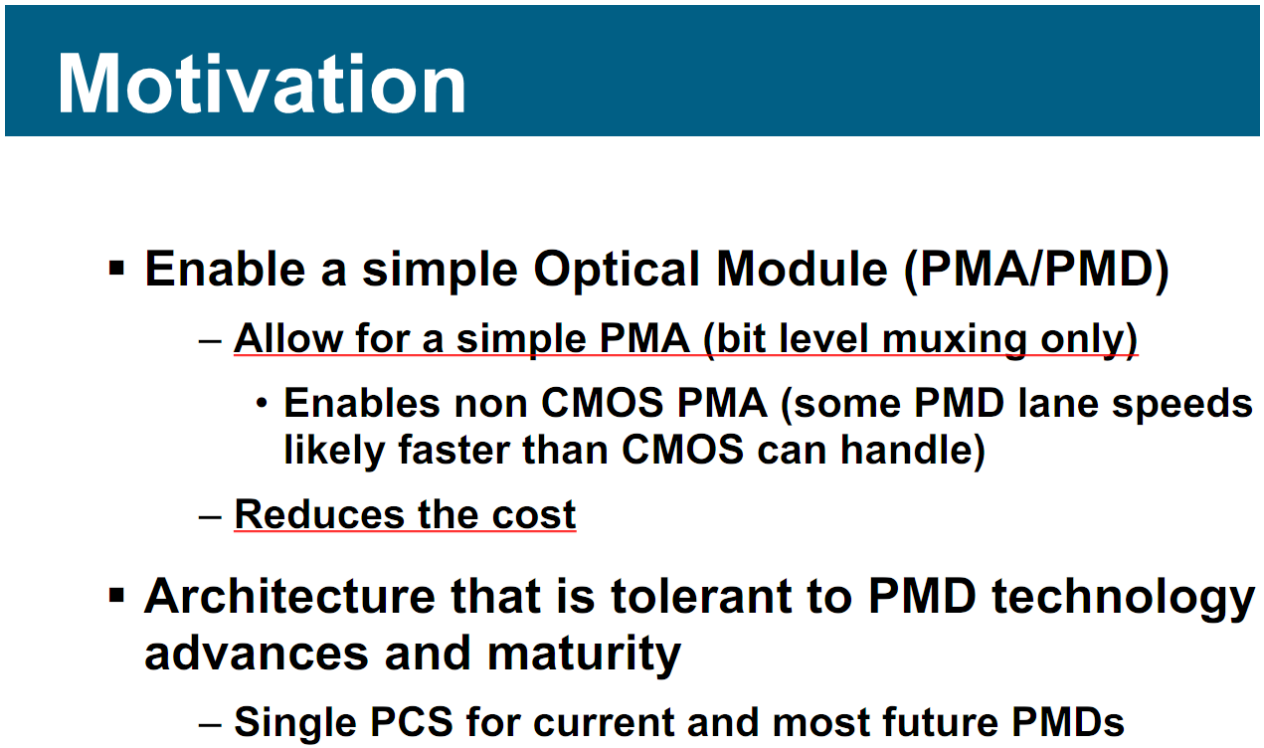
- FOM (FEC Orthogonal Multiplexing) bit-multiplexing method was presented in January meeting 2014 (wang_400_01a_0114.pdf).
- Bit mux in optical module will make it simple implement and reuse in OTN to enable broad market potential.



- How to do CDAUI-n interoperation with FOM bit-multiplexing was investigated in May Meeting(wang_x_3bs_01_0514.pdf).
- FEC performance of FOM/Non-FOM bit/symbol-multiplexing was calculated for RS(528,514) in May Meeting (wang_t_3bs_01_0514.pdf). Further calculation of FEC performance for all multiplexing method with RS(528,514) & RS(544,514) will be presented in July meeting.

Bit Multiplexing in 802.3ba 100GbE

- In 100GbE, MLD proposal address bit multiplexing requirement to enable protocol agnostic optical module by gustlin_0107.



- Bit multiplexing in optical module will shorten verification & test time.

Why FOM Bit Multiplexing in 400GbE

- Error propagation is most possibly introduced in 400GbE link, such as CDAUI-n and PAMn receiver equalizer.

Introduction

If a DFE is assumed to be part of the receiver for CAUI-4 chip-to-chip (C2C), then the probability of burst errors is much greater than for receivers that do not employ DFE. The likely presence of burst errors would call in to question the mean time to false packet acceptance (MTTFPA) performance of a link using CAUI-4.

Because of this, the reference receiver assumed for CAUI-4 C2C in P802.3bm D1.1 employs a CTLE but no DFE.

However, there has been discussion within the P802.3bm Task Force and the CAUI-4 Ad Hoc suggesting that the restriction in performance due to assuming a CTLE only reference receiver severely restricts the broad market potential of the CAUI-4 C2C solution.

This presentation attempts to analyse the impact of a DFE in the CAUI-4 C2C receiver on the MTTFPA performance.

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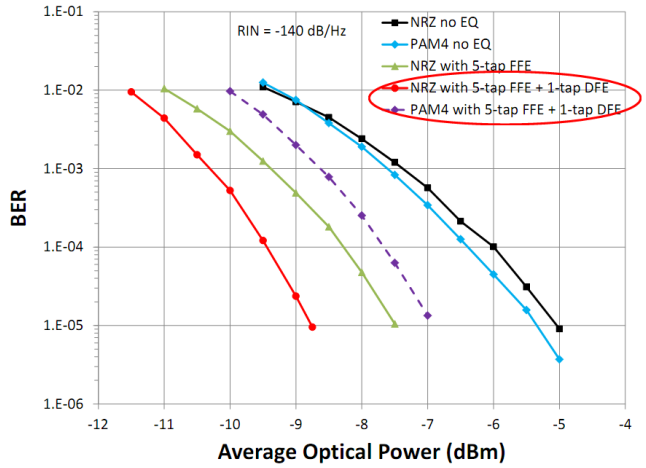
56 Gb/s Monte-Carlo Simulation Results



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- FOM bit-multiplexing/de-multiplexing is a general method to spread burst error into multi sub-BJ FEC instances for improving FEC performance.

Scalability of Bit Multiplexing in PAM4 Electrical Modulator with 2:1 Gearbox

Review of EML-based 56Gb/s PAM-4 Experiments

Reference	Link distance	Link budget w/o WDM (=(a)-(b))	EML output power (a)	Received optical power @ 3e-4 (b)	Extinc-tion ratio	2-bit DAC BW	Driver Amp BW	EML BW	RX 3-dB BW	Error Detection and Equalizer
Schell_01_0712_optx	10 km	--	--	--	5.7dB	--	--	--	--	--
Xu_400_01a_0114	10 km	17.3dB	+6dBm	-11.3 dBm	9dB	13GHz	18GHz	17GHz	20GHz	Error Analyzer DFE (No. taps=1)
Man_3bs_01_0514	10 km	12.9dB	+0dBm	-12.9 dBm	6.5~7dB	19GHz	20GHz	21GHz	20GHz	160 Gsps DSO (analog BW=63GHz), FFE (No. taps=31)
Bhoja_3ba_01_0514	10km	14dB	+4dBm	-10dBm	>6dB	19GHz	25GHz	21GHz	28GHz	80GS/s DSO (analog BW=30GHz), FFE (No. taps=10)

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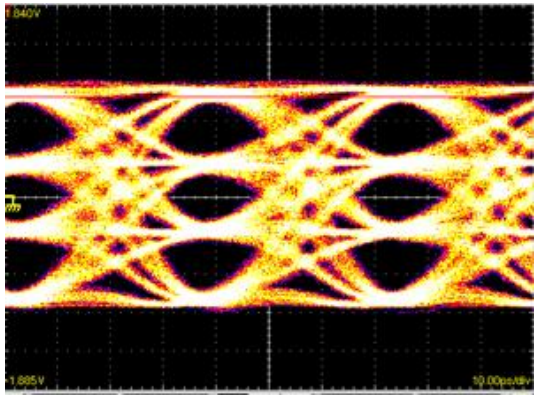
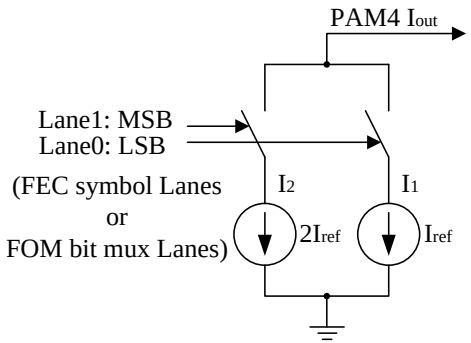


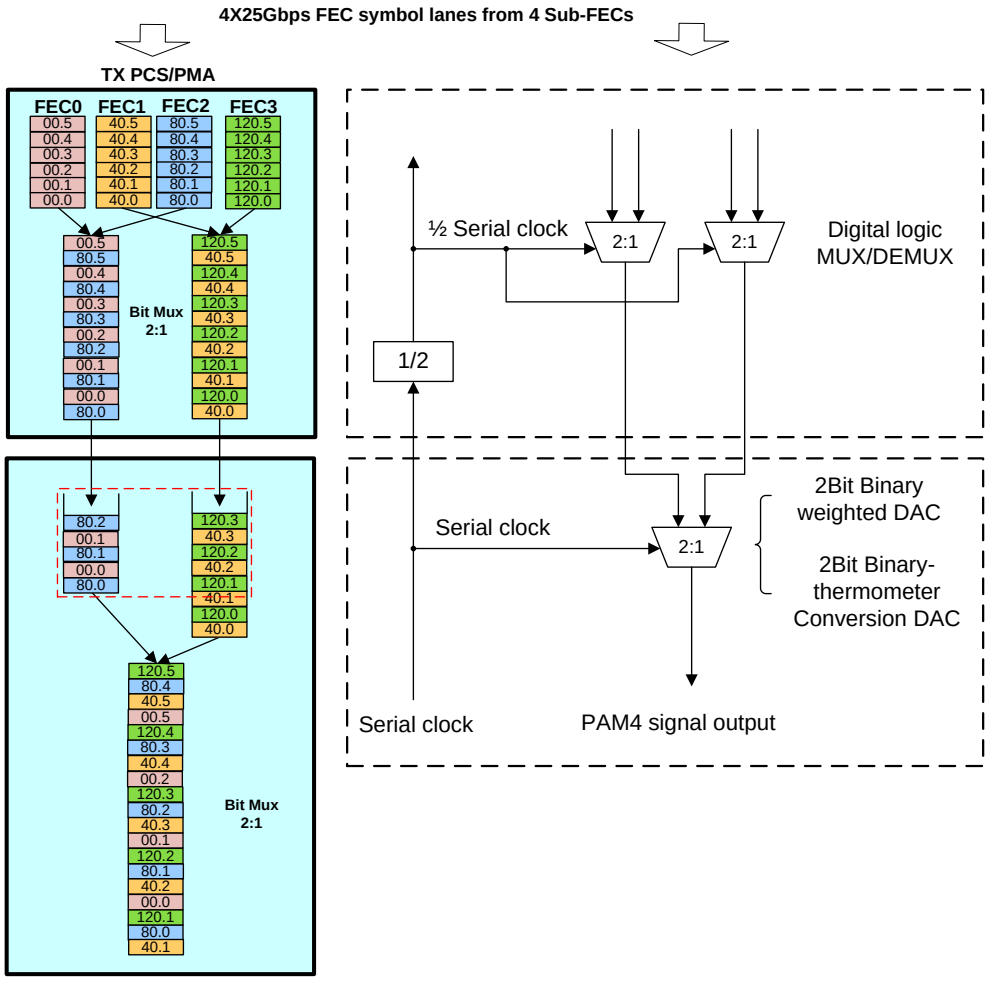
2Bit Binary Weighted DAC:



- Most common PAM4 signal modulator implementation with 2:1 gearbox is based on 2bit binary weighted DAC.

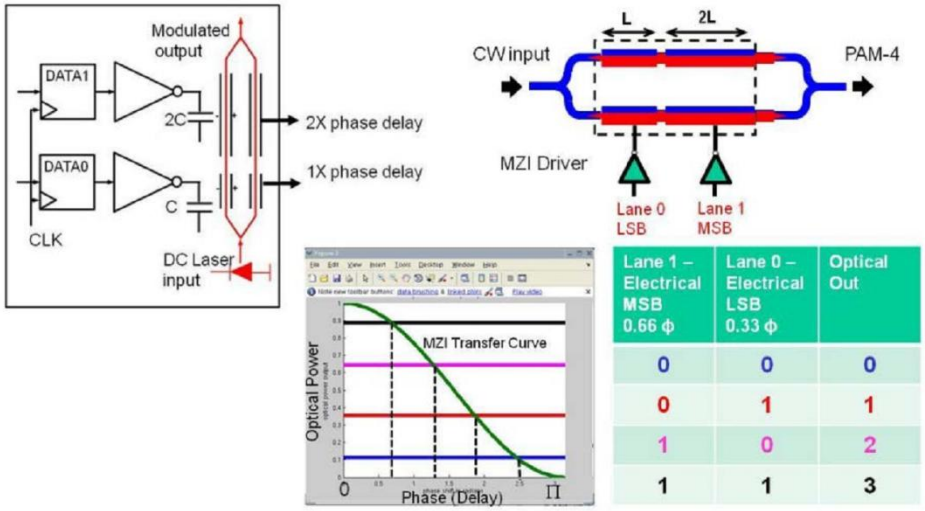
Scalability of Bit Multiplexing in PAM4 Electrical Modulator with 4:1 Gearbox

- How to generate PAM4 signal with 4:1, for example from 4X25Gbps NRZ to 1X50GBaud PAM4 signal?
  - Cascade two 2:1 Mux/DeMux for 4:1 mux;
  - 1st stage 2:1 mux is in digital logic implementation;
  - 2nd stage 2:1 with same 2bit binary weighted DAC or binary-thermometer DAC as in 2:1 gearbox;



Scalability of Bit Multiplexing in PAM4 Optical Modulator

- In theoretical view, segment MZM is essentially a bit mux implementation in optical area.
- 2bit binary weighted DAC/binary-thermometer DAC is most likely an electrical area bit multiplexing.
- FOM bit-multiplexing in PMA proposal is friendly with these general implementations
- Symbol-multiplexing has more complexity adapting to these PAM4 electrical/optical modulators.



Lane 1 – Electrical MSB 0.66 ϕ	Lane 0 – Electrical LSB 0.33 ϕ	Optical Out
0	0	0
0	1	1
1	0	2
1	1	3

Segmented MZI + Simple Digital Driver > DAC function for PAM

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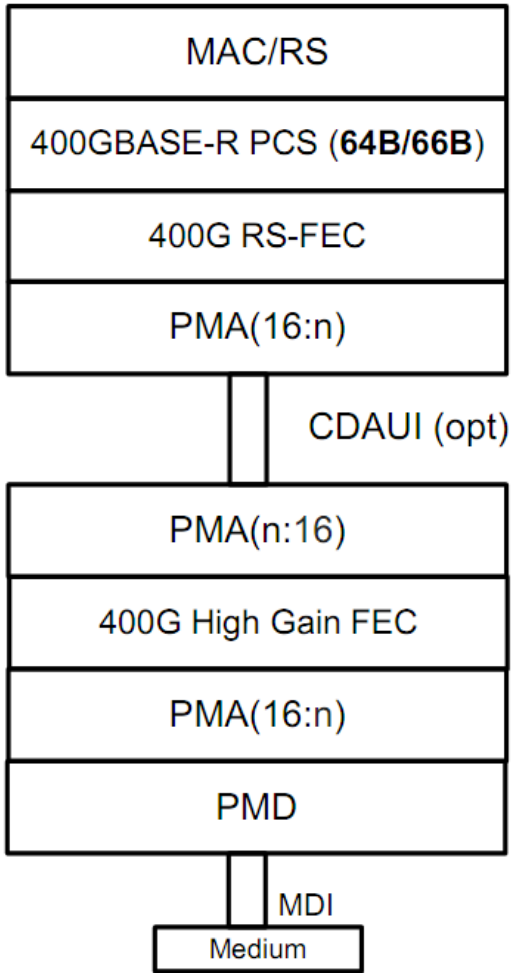
How to support High Gain FEC?



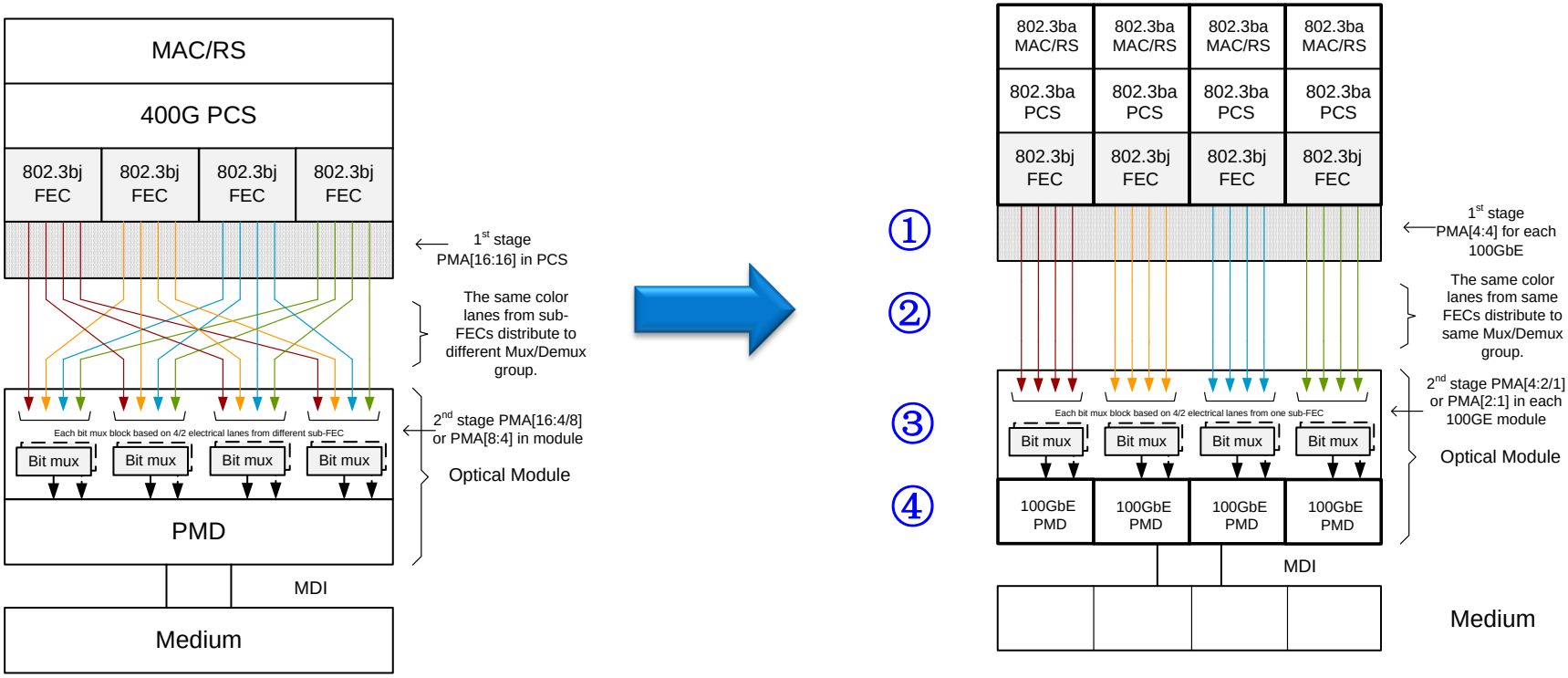
- As discussed In November 2013 Dallas meeting (gustlin_400_01_1113), High Gain FEC in the architecture can be integrated by:
  - Option 1: add the FEC on top of what is already there, no additional transcoding is needed
  - Option 2: strip off the current FEC and then add a stronger FEC to the PCS encoded data.
- With the FOM Bit-Mux proposal and Option1, it is easy to add high gain FEC on top of the FEC encoded data and implement protocol agnostic optical module.
  - If the mandatory generic RS-FEC is RS(528, 514) with transcoding, 0% overclocking in CDAUI interface, there is no need to bypass this generic FEC if High Gain FEC is deployed.
- FOM Bit-Mux proposal also supports option 2, where it just can not realize protocol agnostic optical modules anymore. Further iteration FEC for additional gain can be enabled after generic FEC decoding.

FOM Bit Mux Architecture

- Advantage:
  - Benefit from FOUR sub-BJ FEC, FOM bit mux can reach same FEC performance as 802.3 BJ.
  - Simple implementation for support CDAUI-16/8/4 interoperation if BJ RS-FEC can cover all the physical link; It can also adaptive with additional HG FEC in module.
  - Adaptive to burst error scenarios and even random error only system with one unified architecture.
  - Compatible to PMDs with segment MZM or simple DAC for PAMn signal.
- Challenge:
  - How to support breakout? Although breakout is not an objective of 400GbE.
  - Constraint in SerDes layout design on TX side of CDAUI interface;
  - Wavelength or parallel fiber identification is required in width translation when rate of electrical lanes is larger than optical lanes, even this is uncommon.

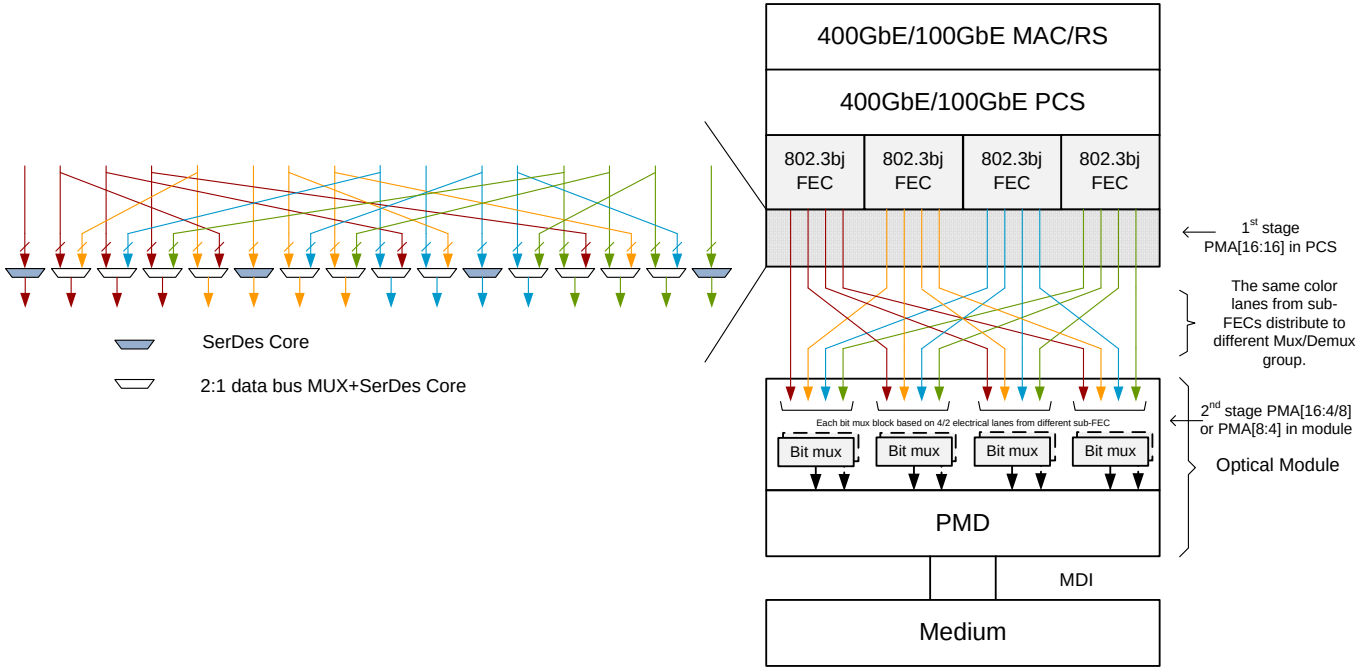
How to Breakout 1X400GbE into 4X100GbE?

- Breakout should be implemented in the following four sub-layer.
  - ① In host ASIC side, for lower silicon cost purpose;
  - ② One unified CDAUI interface layout for both implementation;
  - ③ Share one gearbox solution for 1X400GbE/4X100GbE;
  - ④ PMD breakout for reuse;



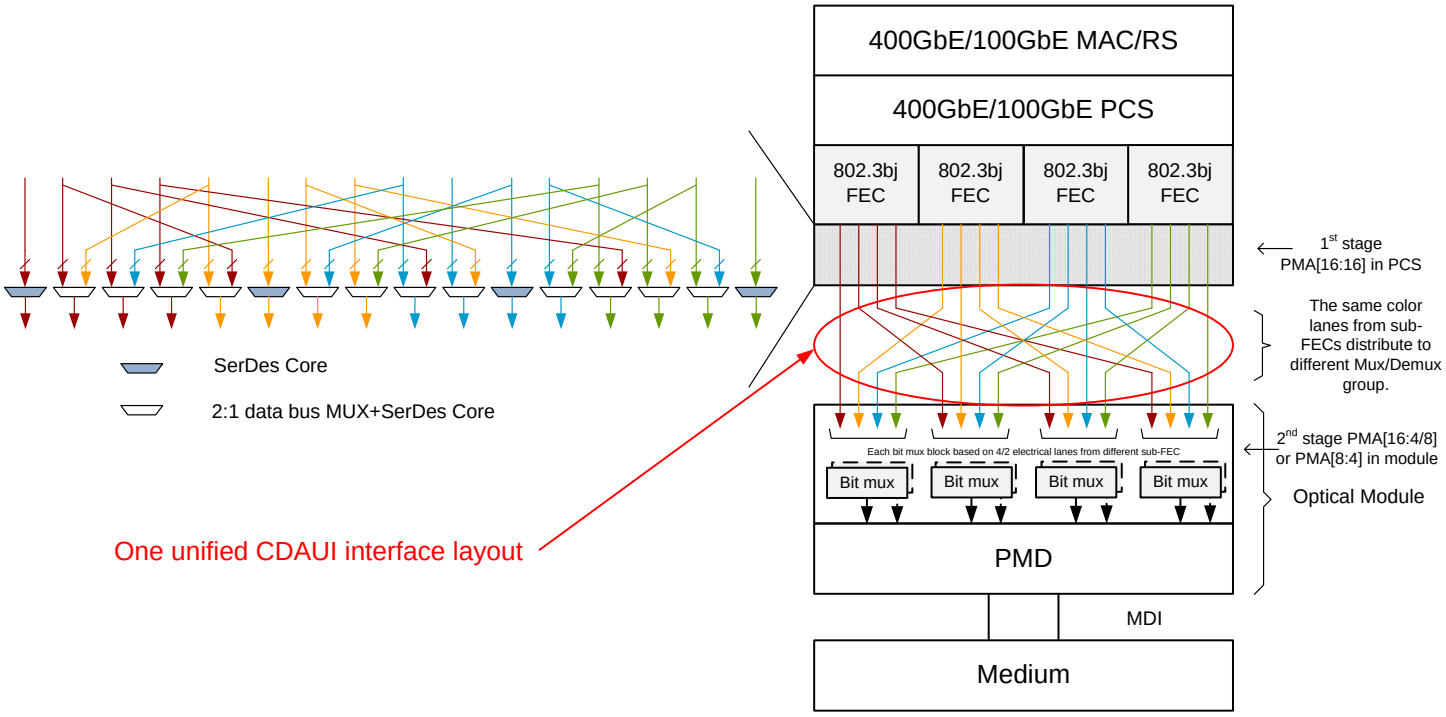
①: Dual Mode PMA in Host ASIC

- PMA Design in ASIC can use additional data bus with 2:1 Mux/Demux to support 1x400/4x100GbE breakout by SerDes re-configuration.
- Logic area cost for dual mode 2:1 Mux/DeMux before every SerDes is low.
- Take 160bit@161MHz as example, ~320LUT for each SerDes pair in FPGA.



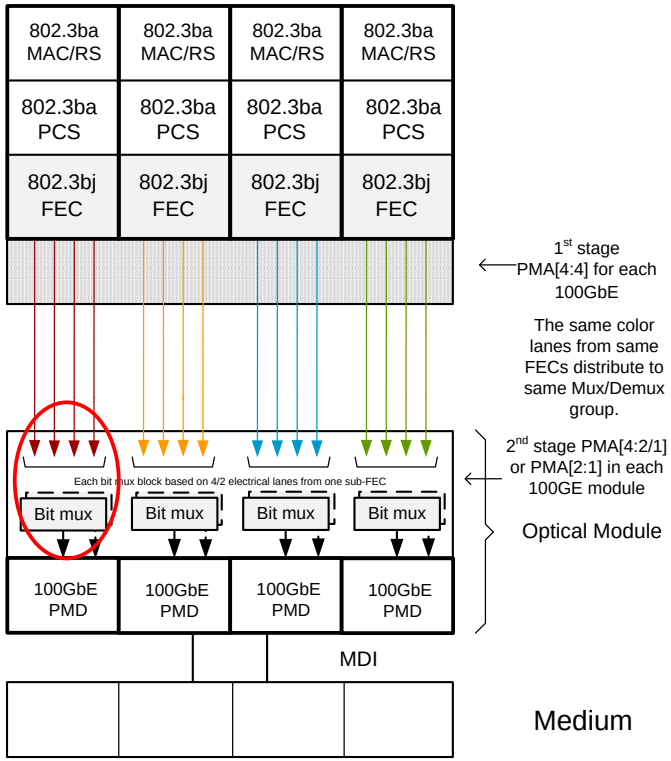
②: CDAUI interface layout

- No hardware layout changes for supporting breakout into 4X100GbE with dual mode PMA;
- For 1X400GbE/4X100GbE hardware layout implementation, it is one unified route design in TX side as FOM bit mux. Breakout will requires additional route constrain in RX side.



③: How to do Mux/DeMux in ¼ slice PMA of 400GbE after breakout?

- As RS FEC is mandatory in 802.3bj/bm, but how to do Mux/Demux in gearbox is undefined?
  - Option 1: General solution with Non-FOM symbol Multiplexing. No supporting bit multiplexing!
  - Option 2: FOM bit mux
    - Use 4X25Gbps RS FEC. This will un-compatible with 802.3bj/bm architecture and introduce additional latency.
    - Bit multiplexing between contiguous codeword of each 802.3 bj/bm RS FEC. This will lead to additional 100ns latency and complexity.
  - Option 3: Non-FOM bit Mux
    - Assuming low burst error probability
    - May have worse performance than FOM bit mux. However, 100GbE requires 1/10 BER objective as in 400GbE. (1e-12 vs. 1e-13)

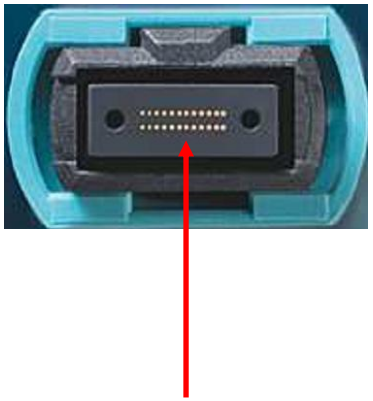


- This Mux/DeMux feature probably will be further defined in future 100GbE standard with new PMD.

④: Breakout in PMD

- Breakout in Optical module is more easy with parallel fiber comparing to duplex one-pair fiber solution.
- Port serial number should be pre-defined from high level system management view, for example MPO-4XLC fiber.

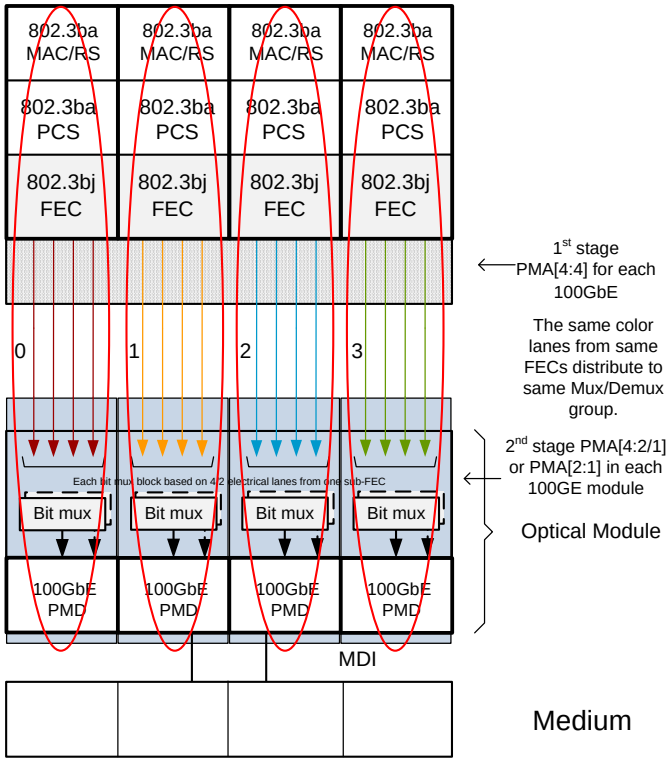
Port 0	Port 1	Port 2	Port 3	Interoperation issue as port serial number difference
Port 1	Port 3	Port 2	Port 0	



Port serial number vs. ferrule position

④: Breakout in PMD(Cont'd)

- Breakout function needs to know which one is Port 0 or 1/2/3, for example to shut down/bring up and connect to the correct peer destination.
- From system view, high level management software wants to know which sub-port is connect to the desired peer destination. The port identification(number #n) should be same in:
  - Management view in system software;
  - CDAUI interface lanes number/sequence;
  - Physical lanes parameter, for example wavelength for WDM PMDs and ferrule position for parallel ribbon.
- This requirement in CDAUI TX route layout also exists for FOM bit mux.



Summary

- PMA architecture is bridge between 400GbE logic layer and PMDs. Tradeoff is needed in system flexibility from standard architecture and implementation.
- FOM bit mux is an unified and robust architecture which is adaptive to burst error scenarios and even random error only system.
- FOM bit mux is more friendly with simple PMD proposal, such as segment MZM and general DAC for PAMn signal.
- Breaking out 1X400GbE into 4X100GE gives same TX route layout constrain as FOM bit mux.
- Several options are discussed on how to do multiplexing within each ¼ 400GbE PMA for breakout. This issue is related to future 100GbE standard with new PMD.

Further Work

- Detailed analysis the cost comparison of complexity/power/area for bit/symbol mux scheme in PMA/PMDs;
- Investigate gray coding/precoding with FOM bit mux architecture and error correct capability.
- Investigate burst error model of various PMDs in 400GbE;
- MTTFPA analysis;

Thank you