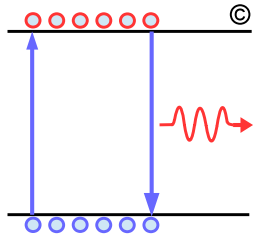


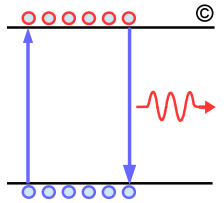
# Path to Consensus on 400 GbE PMDs

**Ali Ghiasi**
**Ghiasi Quantum LLC**

**IEEE 802.3bs Task Force**

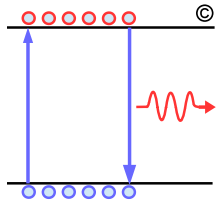
**Sept 2014**

# Current 802.3bs Objective Per Dallas Meeting



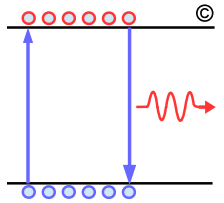
- **Provide physical layer specifications which support link distances of at least 100 m over MMF**
- **Provide physical layer specifications which support link distances of at least 500 m over SMF**
- **Provide physical layer specifications which support link distances of 2 km on SMF**
- **Provide physical layer specifications which support link distances of at least 10 km over SMF**
- **Key questions where consensus need to be developed are:**
  - Do we define in .bs more efficient PMDs?
  - Do we define higher bit rate narrower CDAUI in .bs?

# PMD Evolution Options

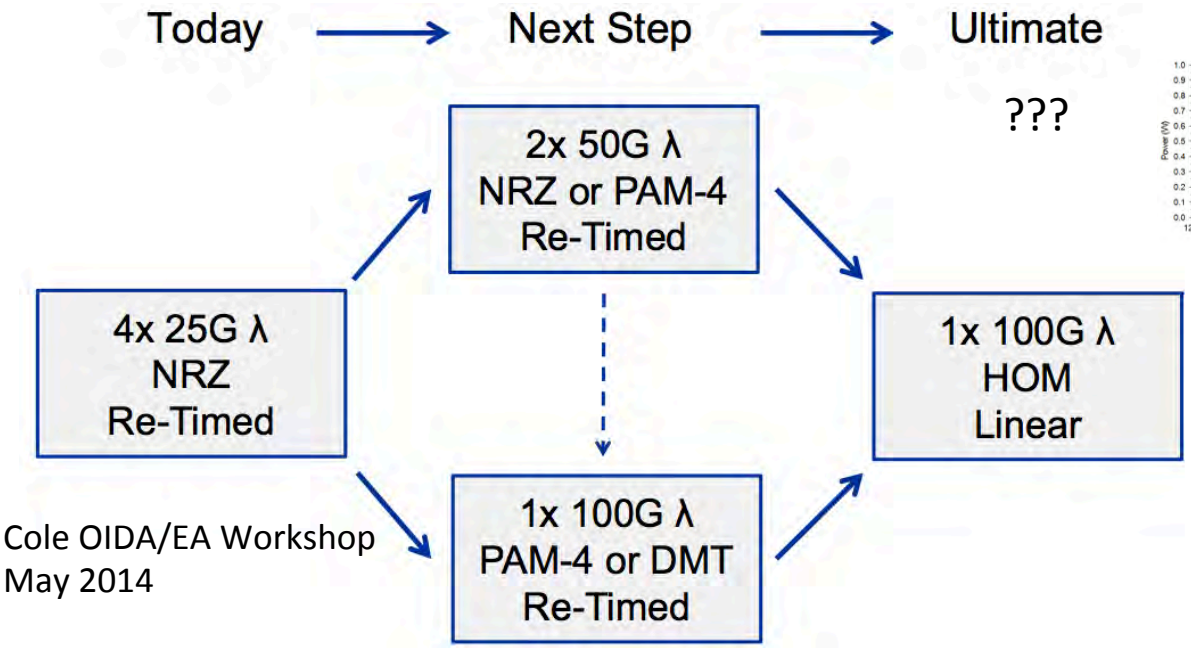


- **Current Gen 16x25G – Signaling NRZ**
  - Advantage: mature technology and reuse
  - Dis-advantages: SR16/PSM16 high cost associated with 32 fibers and CDAUI-16 makes the module too wide, LR16 is high cost effectively a Metro WDM, with migration to CDAUI-8 these PMDs require inverse-mux in the module
- **Next Gen 8x50G – Signaling (NRZ, PAM4, or DMT)**
  - Advantage: Common 50 Gb/s signaling and host based moderate gain FEC ~ 6 dB is sufficient for CDAUI-8, SR8, PSM8, FR8, and LR8 increases supply base, and lowers the cost
  - Disadvantage: Narrower interface eventually would deliver lower cost
- **Ultimate Gen 4x100G – Signaling (PAM4 or DMT)**
  - Advantage: With 4 lasers eventually lower cost could be achieved
  - Disadvantage: Project will take longer, high gain FEC >9 dB would be required, higher BW component such as as MZM/EA needed, VCSEL/DFB-DML may not have sufficient power/BW, Ring Resonator may not have sufficient BW, solution defined based limited knowledge will be sub-optimal, and/or more complex DSP required.

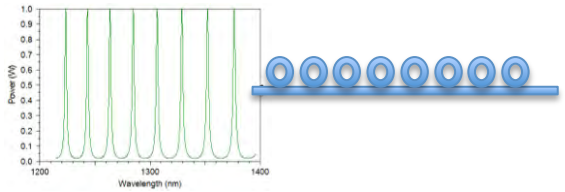
# What Should We Aim for?



- **Aiming for ultimate solution only raises the risk for getting it wrong**
  - As illustrated ultimate solution could be 8l comb laser with ring resonators
  - 100Gb/s PAM4 implementation have been based on high cost-power EML and MZM
  - Defining a PMD based on EML/MZM could remove the option of DML forever!



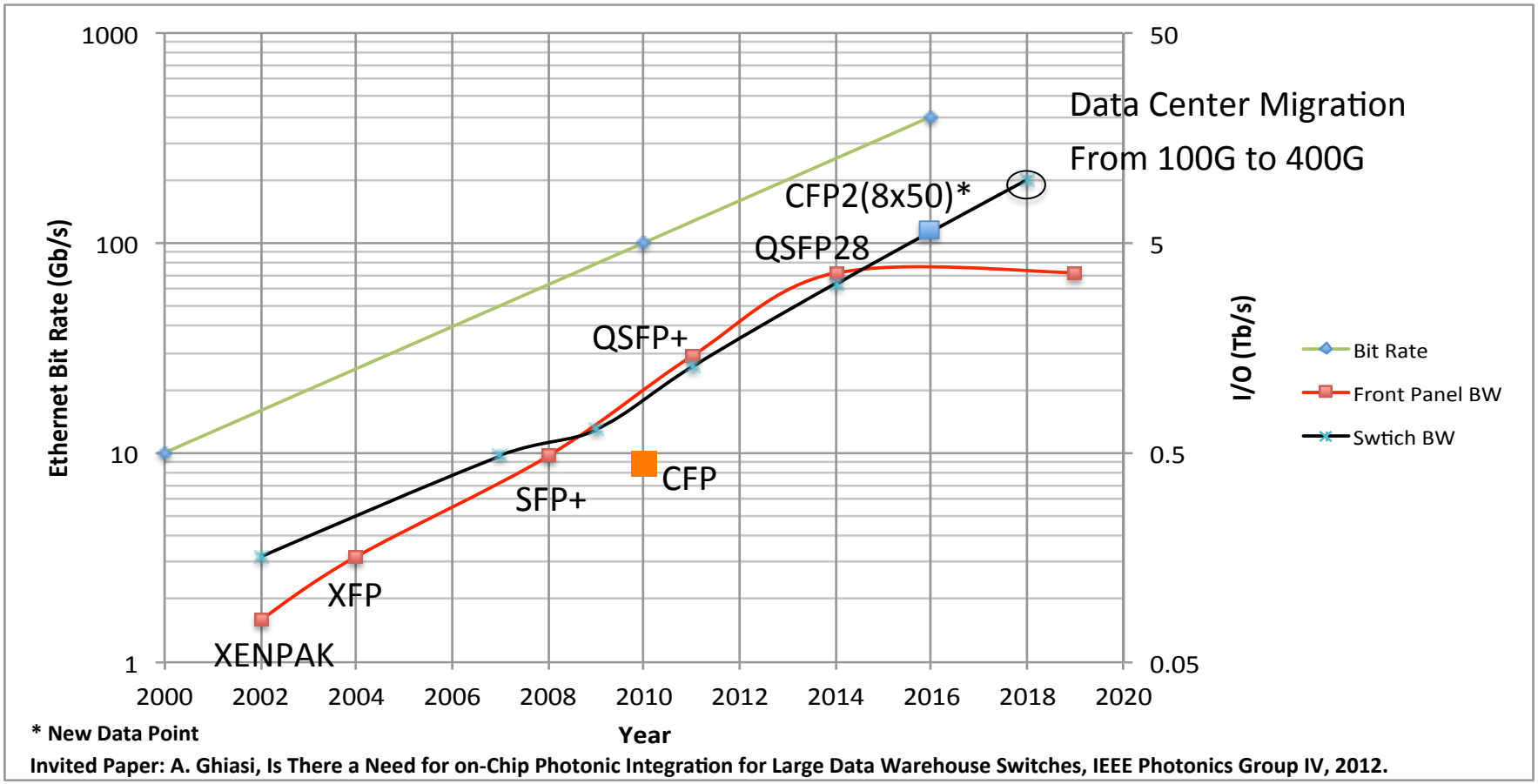

Cole OIDA/EA Workshop
May 2014



**Ultimate solution could be an 8λ comb laser with ring Resonator. Ring resonator Have the promise to deliver Highest density, lowest power, and cost optical devices but Somewhat slow ~20 GBd!**

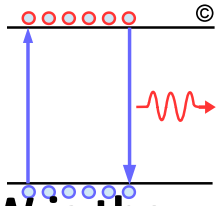
# Ethernet Speed and Switch BW Growth

- **The 2016/2018 data point was superimposed on the original graph**
  - In the 2016 time frame 50G signaling is needed
  - 400G 1-2 km data center optimized SMF PMD is needed in 2018 with availability of 10+ Tb/s switches




Invited Paper: A. Ghiasi, Is There a Need for on-Chip Photonic Integration for Large Data Warehouse Switches, IEEE Photonics Group IV, 2012.

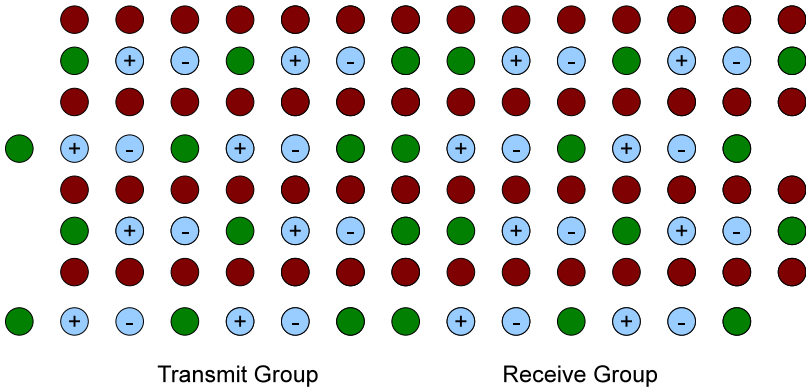
# Do We Need 50G I/O on the ASIC

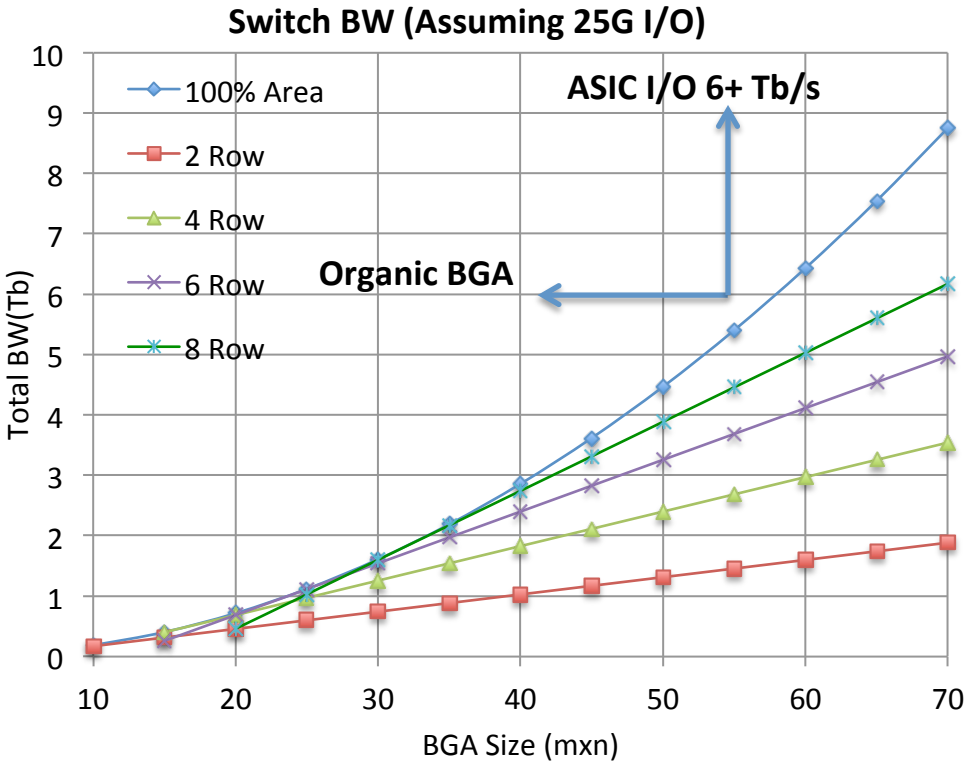


- **For a given package where R is number of high speed rows and BW is the BW density for given ball field assuming 25G I/O, then total BW is calculated as (assuming 25Gb/s I/O) ***

$$Total\ BW = 2 \times R \times \left( (m+n) \times 2 - R \times 8 \right) \times BW$$

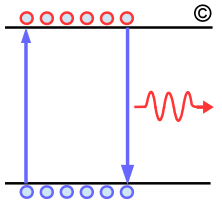
**A Suitable 25G I/O Ball Map**



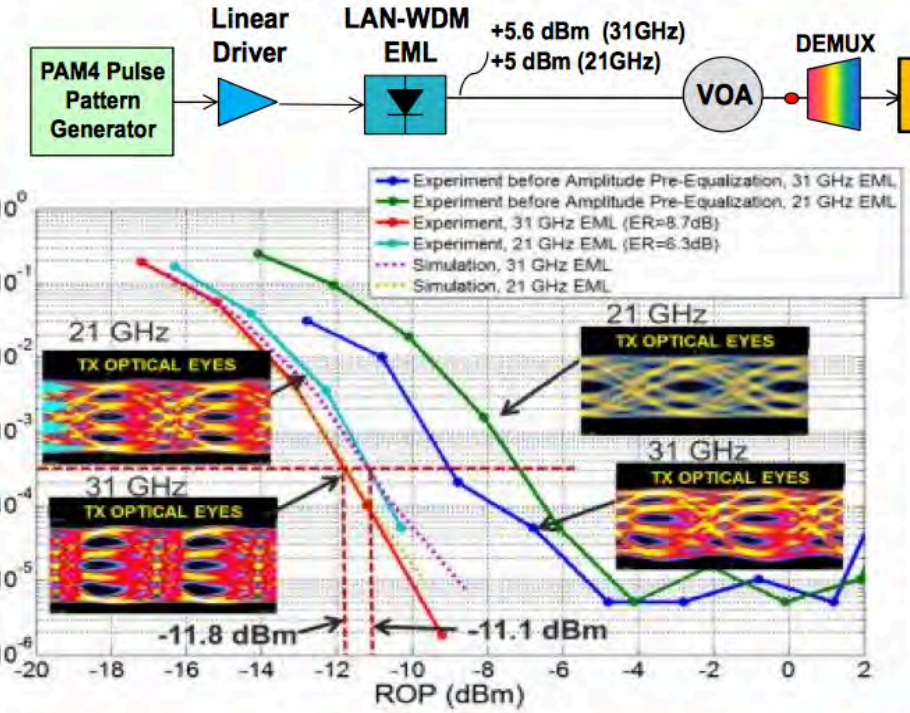




* Invited Paper: A. Ghiasi, Is There a Need for on-Chip Photonic Integration for Large Data Warehouse Switches, IEEE Photonics Group IV, 2012.

# Feasibility of 50G PAM4 Based on 21 GHz EML



## 56Gb/s PAM-4: Use Pulse Pattern Generator with adjustable voltages

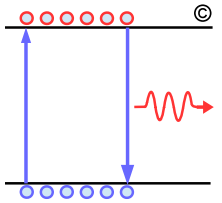


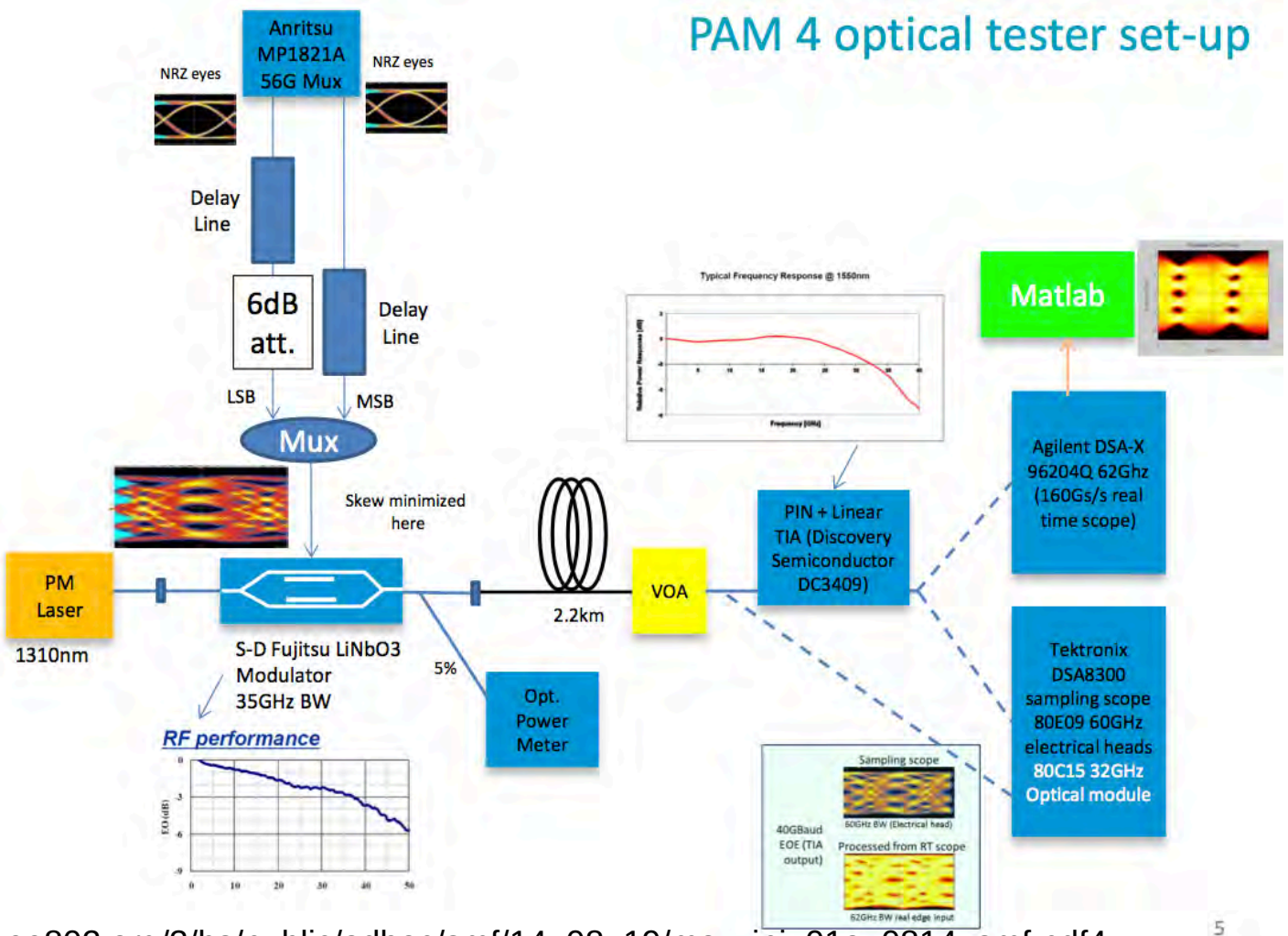

| 56Gb/s PAM-4 Simulation Parameters | | |
|---|---|---|
| Parameter | Value | Unit |
| Bit rate | 56 | Gb/s |
| SNR before EML | 21 | dB |
| EML BW (1st-order Bessel) | 21 or 31 | GHz |
| Linear driver amp BW (1st-order Bessel) | 32 | GHz |
| ER | 6.3 or 8.7 | dB |
| Wavelength | 1310 | nm |
| RIN | -145 | dB/Hz |
| Receiver input spectral noise density | 25 | pA/√Hz |
| PD + TIA BW (1st-order Bessel) | 22 | GHz |
| Number of FFE taps | 19 | |
| ADC bandwidth (5th-order Bessel) | 25 | GHz |

- **Pre-equalize three eye amplitudes can improve BER significantly**
- **31GHz vs 21GHz EML: Receiver sensitivity improvement ~ 0.7 dB, mainly due to ER difference**
- **Simulation and experimental results match well**

http://www.ieee802.org/3/bs/public/14_05/way_3bs_01a_0514.pdf

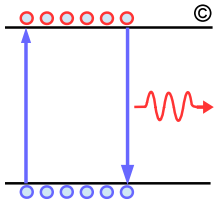
# Feasibility of 100G PAM4 Based on 35 GHz LiNbO3

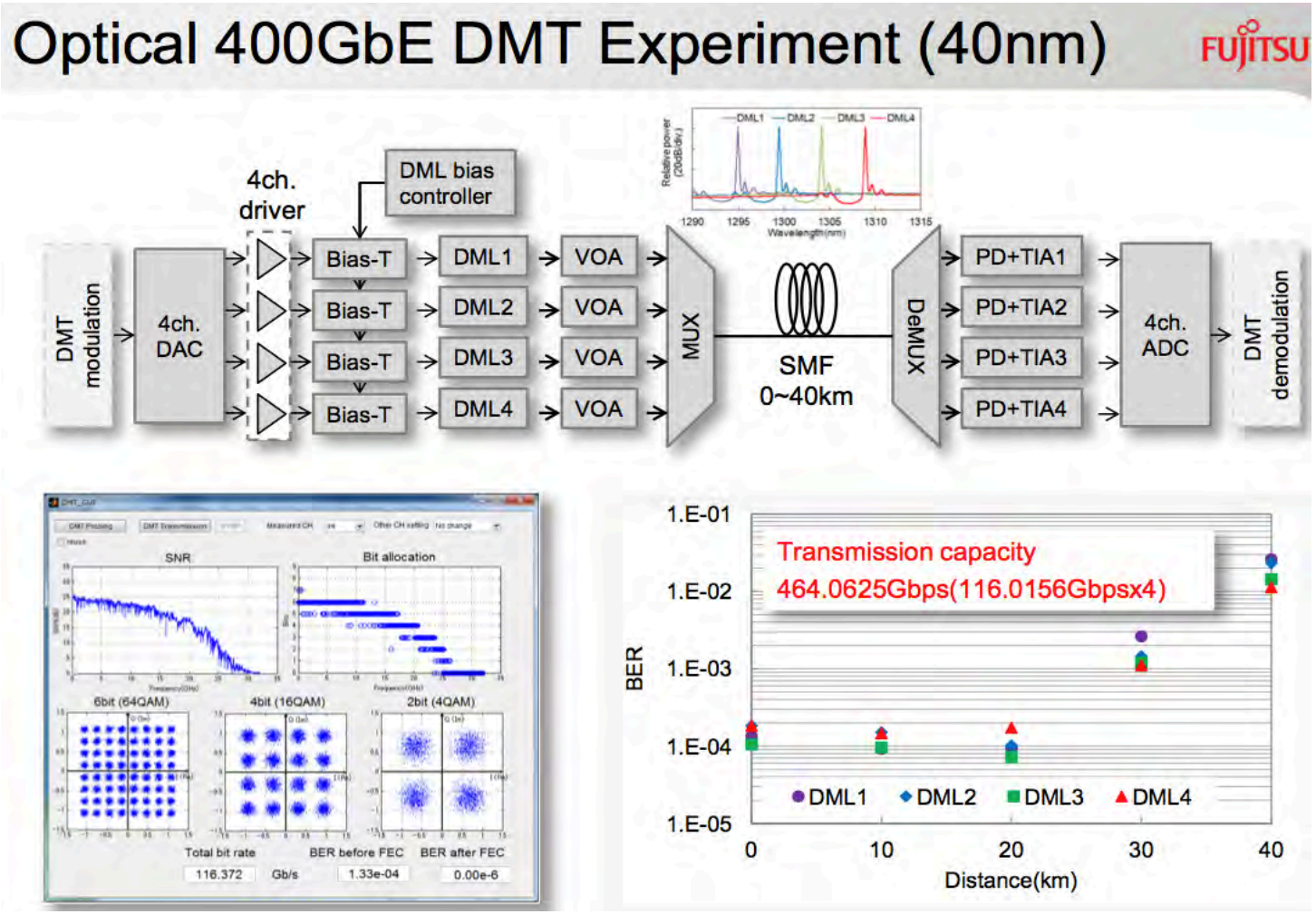





Refer: http://www.ieee802.org/3/bs/public/adhoc/smf/14_08_19/mazzini_01a_0814_smf.pdf4

# Feasibility of 100G PAM4 Based on 25G DML

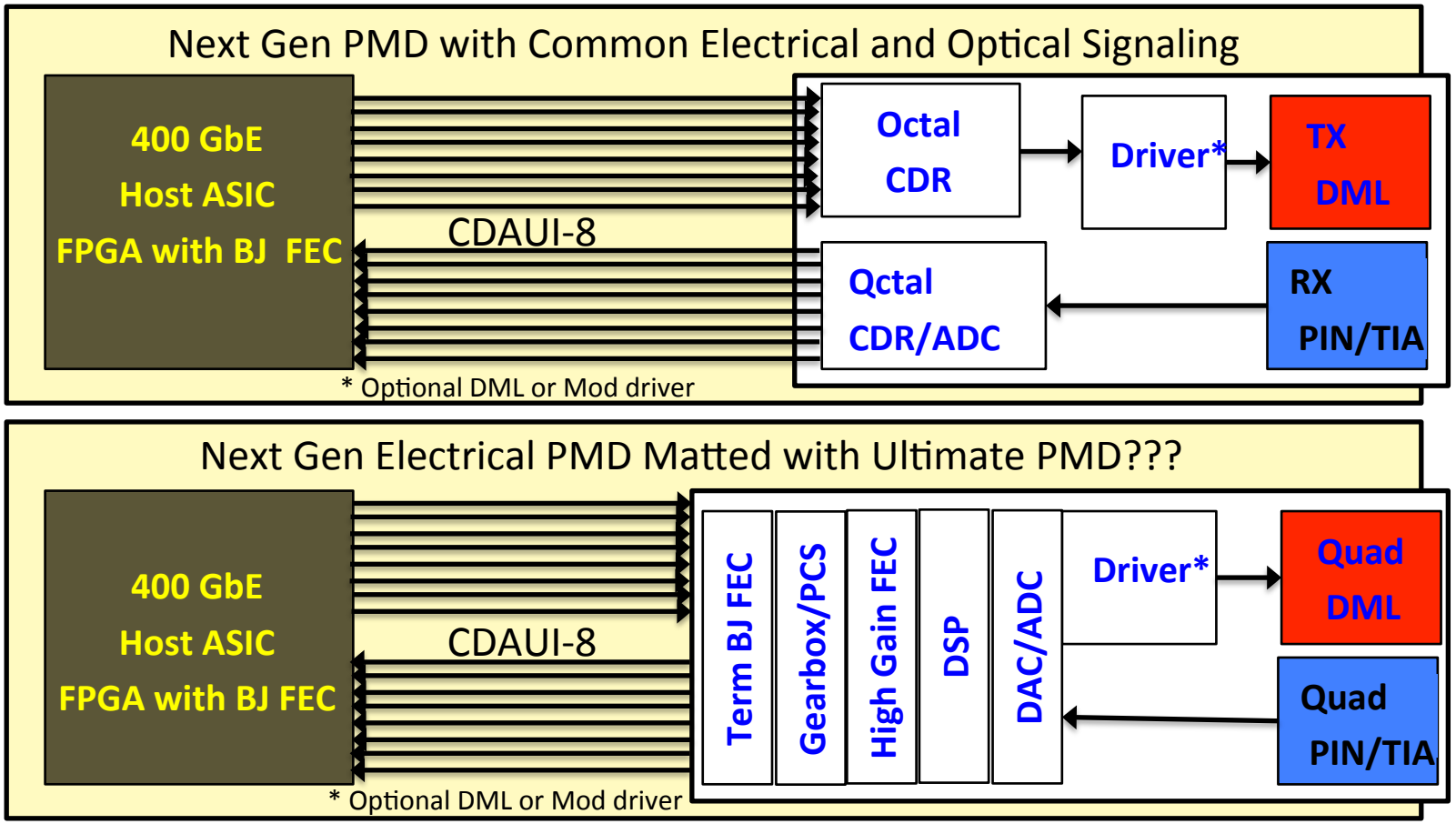





Refer: http://www.ieee802.org/3/bs/public/14_07/dedic_3bs_01a_0714.pdf

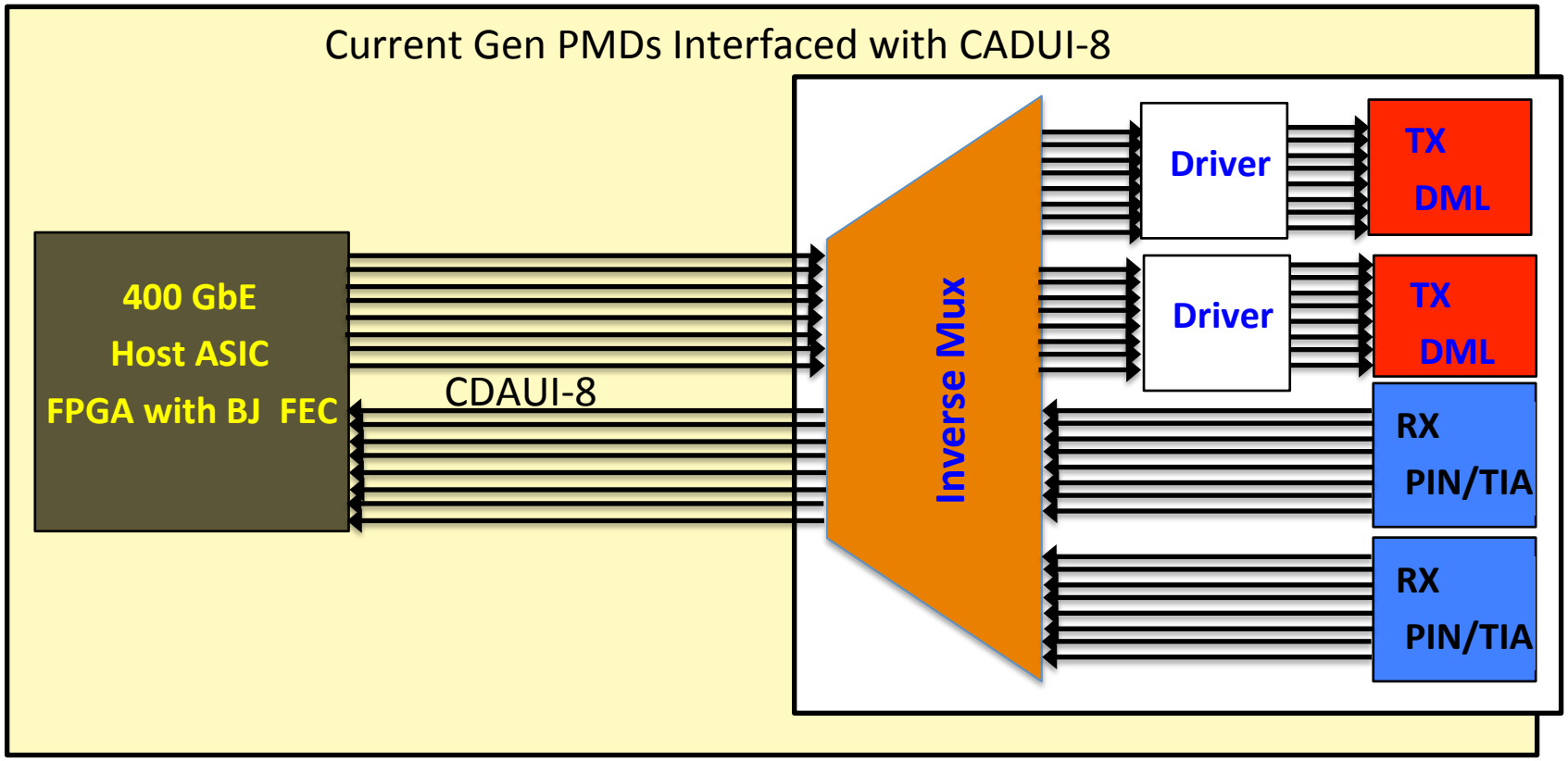
# 400 GbE PMD Architecture

- **8x50G could create ubiquitous interface similar to todays' 100Gbase-SR4/LR4**
  - Developing 2nd Gen PMD now require more complex DSP, higher gain FEC, high cost, and the solution likely will be sub-optimum than waiting ~ 3 years to develop 100 Gb/s/lane in the next project based on additional research!

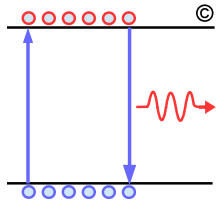


# 400 GbE PMD Architecture

- **By 2016 50 Gb/s/lane IO is needed for ASICs and C2M to address system BW**
  - In 802.3ae we also defined 16 lanes electrical XSBI but was short lived
  - CADUI-16 could also be short lived with introduction of CADUI-8
  - PSM-16 and SR-16 with in 2 years may require costly Inverse Mux in the module with migration to CADUI-8.



# Natural Evolution of 400 GbE PMDs

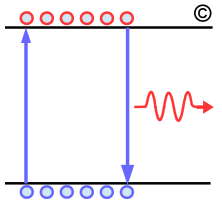


- **50 Gb/s PAM-4 is the only viable common signaling**

| PMD | Remark | 25G NRZ | 50G NRZ | 50G PAM4 | 100G PAM4 | 100G DMT |
|---|---|---|---|---|---|---|
| CADUI-16 | Needed for ASIC Currently in Design | ✔ | | | | |
| 400G-SR16 | Address Interim Need, 100G Breakout | ✔ | | | | |
| CADUI-8 C2M | Linecard I/O BW in 2016 | | No | ✔ | | |
| CADUI-8 C2C | ASIC I/O BW in 2016 | | No | ✔ | | |
| 400G-SR8 | Needed to Match ASIC I/O To Maintain 100 m reach | | ? | ✔ | | |
| 400G-LR8 | Addressing 10 km Routers Needed now | | ✔ | ✔ | | |
| 400G-FR8 | Addressing 2 km Datacenters Needed in 2018 | | ✔ | ✔ | | |
| 400G-FR4 | Addressing 2 km Datacenters Needed in 2018 | | | | ✔ | ✔ |

Area of Dispute

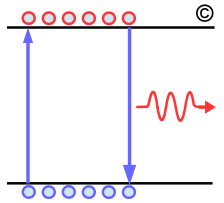
# PAM4 vs DMT



- **PAM4 advantage is the ability to cost and power optimize the SerDes for each applications and be backward compatible with 25G NRZ**
  - C2M: TX FFE + RX CTLE (Lowest Power)
  - C2C: TX FFE (optional 1+D) + RX CTLE and 1 Tap DFE (Mid Power)
  - KR/CR: TX FFE (optional 1+D) + RX CTLE and DSP (Highest Power)
  - SRx/LRx SerDes could be based on C2C
- **PAM4 disadvantage is that the equalization could be more complex**
- **DMT greatest advantage is ability to operate over channel with strong interference and suck out which is not applicable to optical channels**
  - It was shown that "DMT offer no theoretical spectral efficiently advantage over PAM-DFE receiver over reasonable channels"

    http://www.ieee802.org/3/bs/public/14_07/bliss_3bs_01_0714.pdf
- **DMT disadvantage is lack of flexibility not offering low power analog implementation similar to PAM4**
  - All DMT implementation require complex high power DSP with DAC +ADC.

# Summary



- **Should 802.3bs even define 16x25G PMDs with emergence of 50G SerDes**
  - CADUI-16 needs be defined to support current 400G ASIC in the development
  - SR-16 could serve as short term need and backfill 100 GbE breakout, but by 2016/2017 with emergence of 50G I/O it will be obsolete
- **100Gb/s/lane PAM4 or DMT still are in research phase and expect to see great technical contributions in upcoming ECOC and OFC**
  - 100 Gb/s is viewed as ultimate solution but defining a PMD based on a set of hero's experiment could become our ultimate nightmare
- **To support linecard BW ASIC I/O and module require 50 Gb/s I/O in 2016**
  - It is given that the industry is converging toward 50 Gb/s PAM4 SerDes for C2M and C2C applications
  - The 50 Gb/s SerDes will be available on the linecard and all other signaling will require a convertor IC
- **Initial 400 GbE applications will be routers and OTN**
  - The high volume data center applications when high density 32 ports of 400 GbE are available sometimes in 2018
- **PAM4 50 Gb/s is the only viable common signaling which can address both C2M/C2C, MMF, and SMF PMDs**
  - IEEE 802.3 is not a research organization
  - Need to focus on defining PMDs based on solid engineering instead of shooting for ultimate PMD with significant margin of error!