Error Floor Investigation for both 56 and 112Gb/s PAM4 Signals

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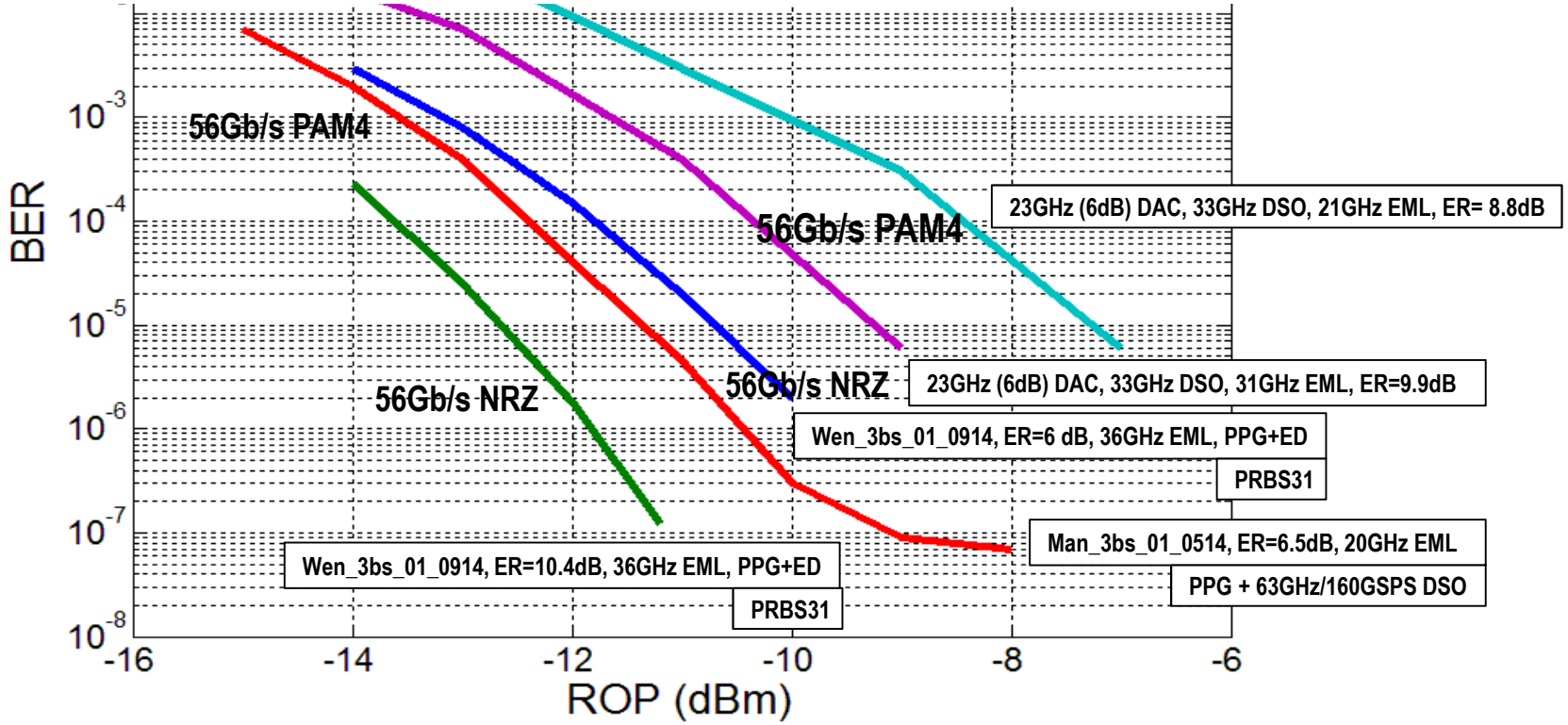
Motivation

- To investigate the main root causes of bit-error floor in 56Gb/s and 112Gb/s PAM4 links by using existing optical transmitters, receivers, and driver amplifiers.

56Gb/s PAM4

Comparing 56Gb/s PAM4 vs NRZ

1. 56Gb/s PAM4 can out perform NRZ if DAC and ADC bandwidth & ENOB limitations are essentially removed, and can use 20GHz EML as opposed to NRZ's 36GHz EML .
2. Even with limited DAC and ADC bandwidth & ENOBs, error floor can be avoided up to BER~ 1e-6
3. Sufficient link margin can be provided by 56Gb/s PAM4 over 10km SMF.



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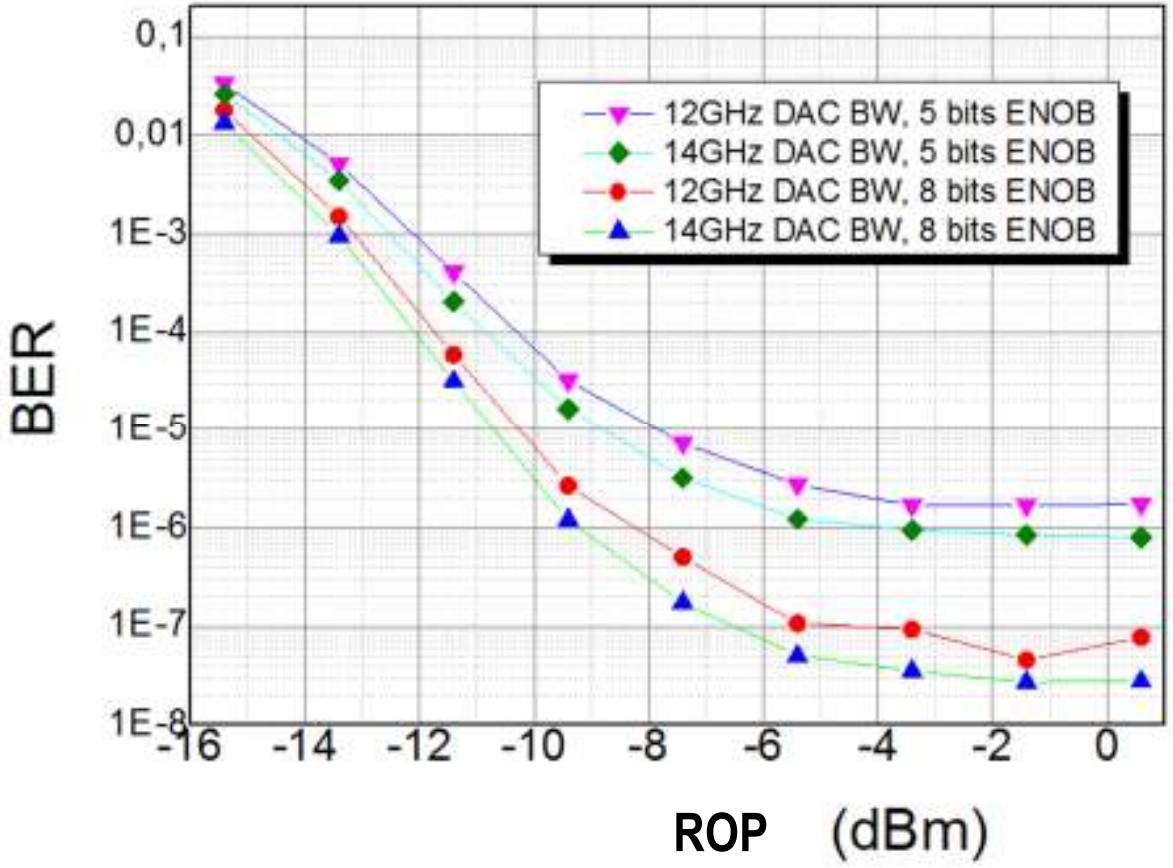
Error Floor cause 1 (albeit at low BER): DAC analog BW limitation and ENOB



(ADC bandwidth= 25GHz, ENOB= 5)

Baudrate=28Gbaud

Driver amp BW=31GHz

SNR directly before E/O (after amp)=21dB

ER~9dB (31GHz EML)

WL=1310nm

RIN=-145dB/Hz

10km SSMF

ICR input noise density=17pa/Hz^(1/2)

PD+TIA BW=22GHz

0.5A/W responsivity

25GHz A/D, A/D ENOB=5, 8bits

21-taps FFE

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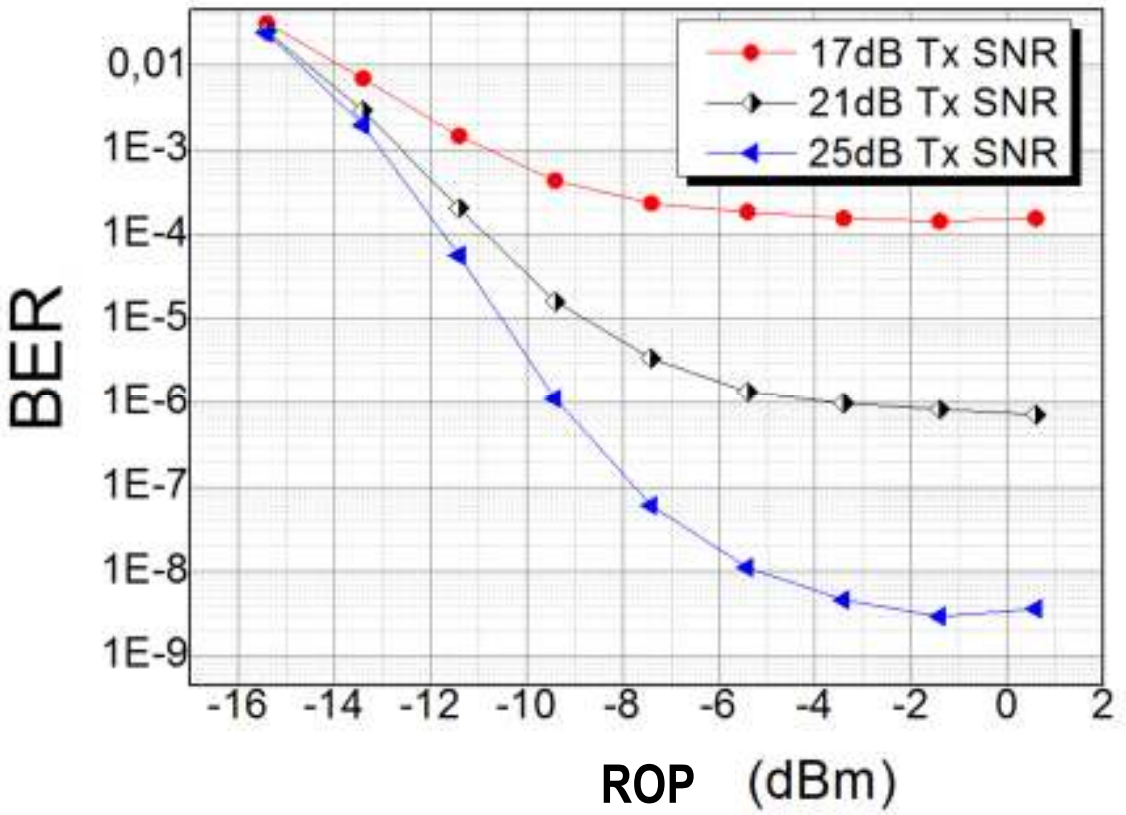
Error Floor cause 2: Electrical SNR before E/O (DAC ENOB & driver related)



(DAC bandwidth= 14GHz, ENOB=8)
(ADC bandwidth= 25GHz, ENOB= 5)

Baudrate=28Gbaud

DAC BW=14GHz

Driver amp BW=31GHz

SNR is estimated directly before the EML

ER=9dB (31 GHz EML)

WL=1310nm

RIN=-145dB/Hz

10km SSMF

ICR input noise density=17pa/Hz^(1/2)

PD+TIA BW=22GHz

0.5A/W responsivity

25GHz A/D, A/D ENOB=5

21-taps FFE

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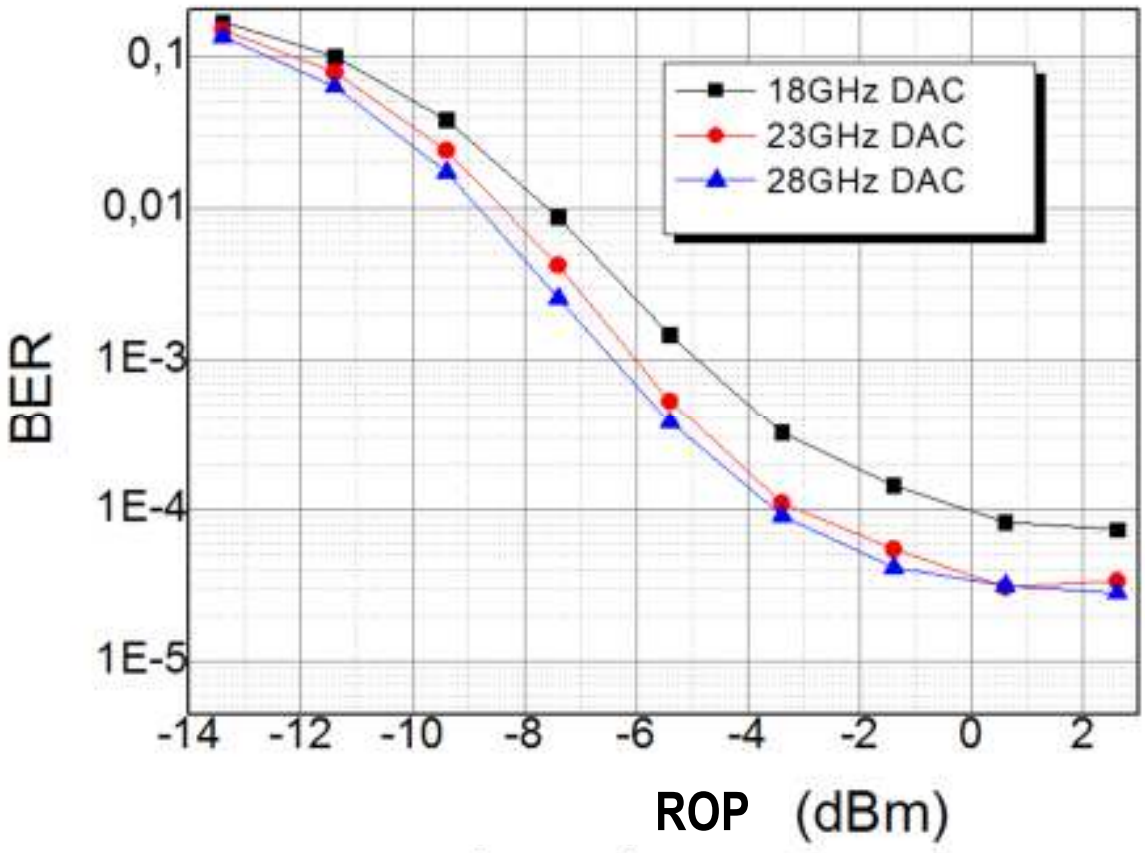
56Gbaud PAM4

112Gb/s PAM4 DAC BW Effects



(ADC bandwidth= 63GHz, ENOB= 5)

Baudrate=56Gbaud

TX linear AMP BW=31GHz

SNR before E/O (after amp)=21dB

EML BW=32GHz

Optimized modulation index

WL=1310nm

RIN=-145dB/Hz

10km SSMF

ICR input noise density=40 pa/Hz^(1/2)

PD+TIA BW=40GHz

21-taps FFE

1st-order Bessel approximation of E/O and PD+TIA

5th-order Bessel approximation for A/D (63 GHz)

5 bits A/D ENOB

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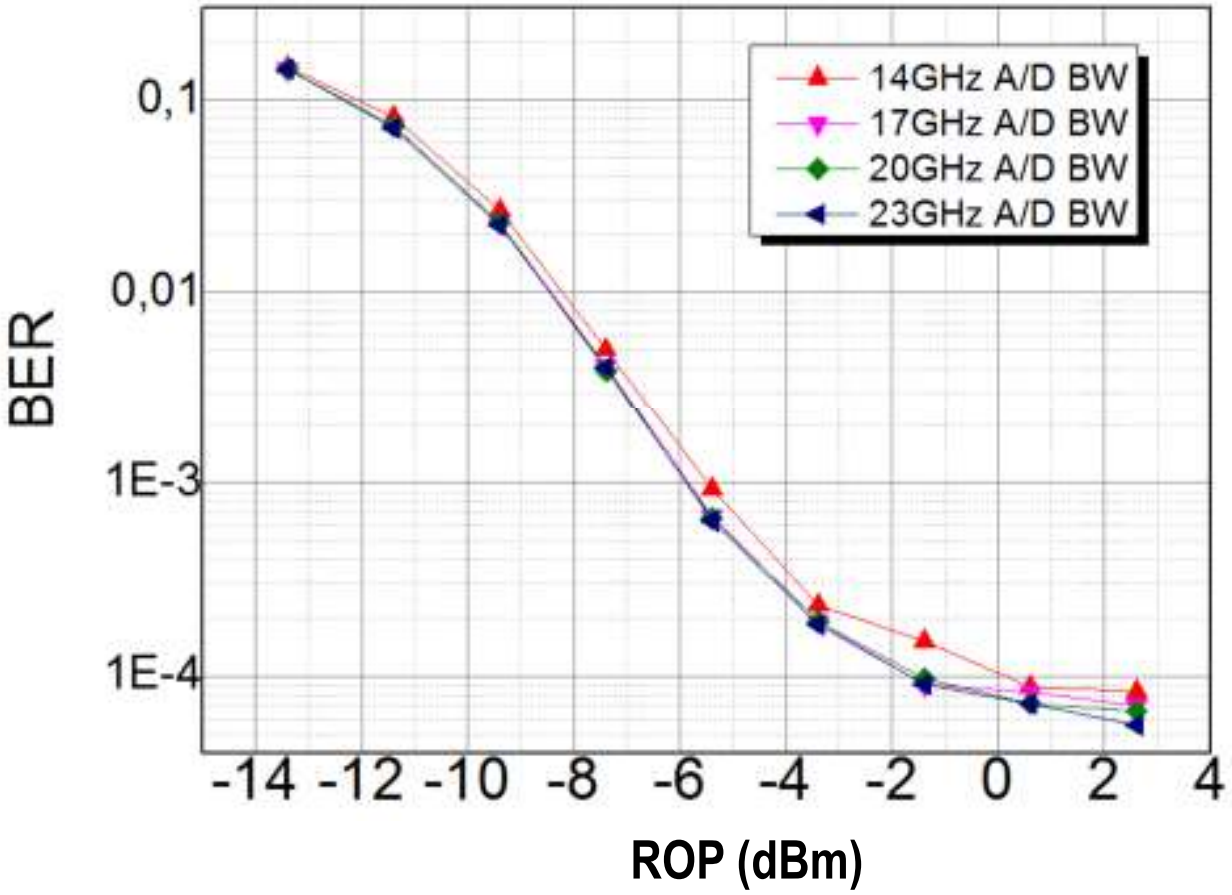
112Gb/s PAM4 ADC BW Effects



(DAC bandwidth= 23GHz, ENOB=8)

Baudrate=56Gbaud

DAC 3dB BW=23GHz

TX linear AMP BW=31GHz

SNR before E/O (after amp)=21dB

EML BW=32GHz

Optimized modulation index

WL=1310nm

RIN=-145dB/Hz

10km SSMF

ICR input noise density=40 pa/Hz^(1/2)

PD+TIA BW=40GHz

1st-order Bessel approximation of E/O , DAC and PD+TIA

5th-order Bessel approximation for A/D, 5 bits A/D ENOB

21-taps FFE

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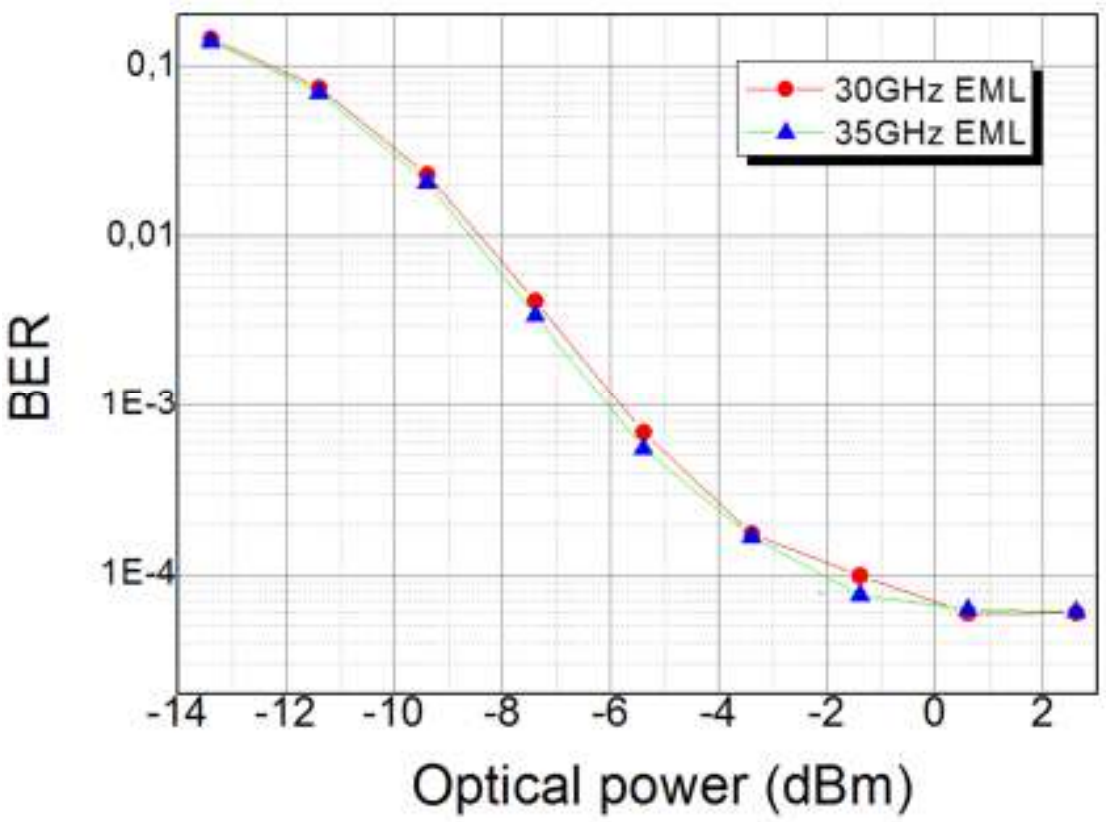
E/O BW limitation influence



(DAC bandwidth= 23GHz, ENOB=8)
(ADC bandwidth= 23GHz, ENOB= 5)

Baudrate=56Gbaud

DAC 3dB BW=23GHz

TX linear AMP BW=31GHz

SNR before E/O (after amp)=21dB

EML BW=30GHz, 35GHz

WL=1310nm

RIN=-145dB/Hz

10km SSMF

ICR input noise density=40 pa/Hz^(1/2)

PD+TIA BW=40GHz

21-taps FFE

1st-order Bessel approximation of E/O , PD+TIA and DAC

5th-order Bessel approximation for A/D (23 GHz), 5 bits ADC ENOB

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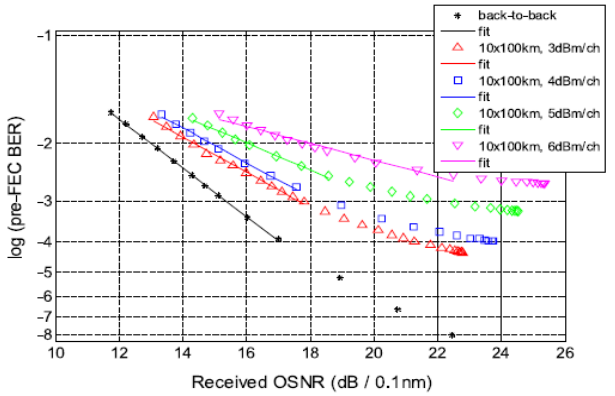
Summary

- **56Gb/s PAM4**
  - -- ADC ENOB and electrical SNR before EML impact error floor
    → With DAC BW≥14GHz, electrical SNR before EML≥21dB, and ADC BW=25GHz, the error floor occurs at ~1e-6
  - – Error floor can be avoided by using DAC and ADC with reasonable bandwidths and ENOBs -- experimental data illustrated
- **112Gb/s PAM4**
  - – For DAC BW=23GHz, ADC BW=23GHz, ENOB=5, electrical SNR before EML ≥21dB, EML BW≥ 30GHz, the error floor occurs at < 1e-4
  - – A pre-FEC threshold of ≥ 1e-3 would be preferred to close the link budget
- **Error floor is common in today's coherent systems**



(ATT, J. Opt. Commun. Netw, Vo.4, Nov 2012)

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