50G PAM4 SERDES PERFORMANCE ON A MEDIUM REACH CHIP-TO-CHIP CHANNEL

Lynn Zheng, Vivek Venkatraman, Magesh Valliappan
IEEE 802.3bs 400Gb/s Task Force
IEEE 802 November 2014 Plenary
San Antonio, TX

CONTRIBUTORS & SUPPORTERS

CONTRIBUTORS

- Anthony Brewster, Yuval Domb, Vivek Telang

SUPPORTERS

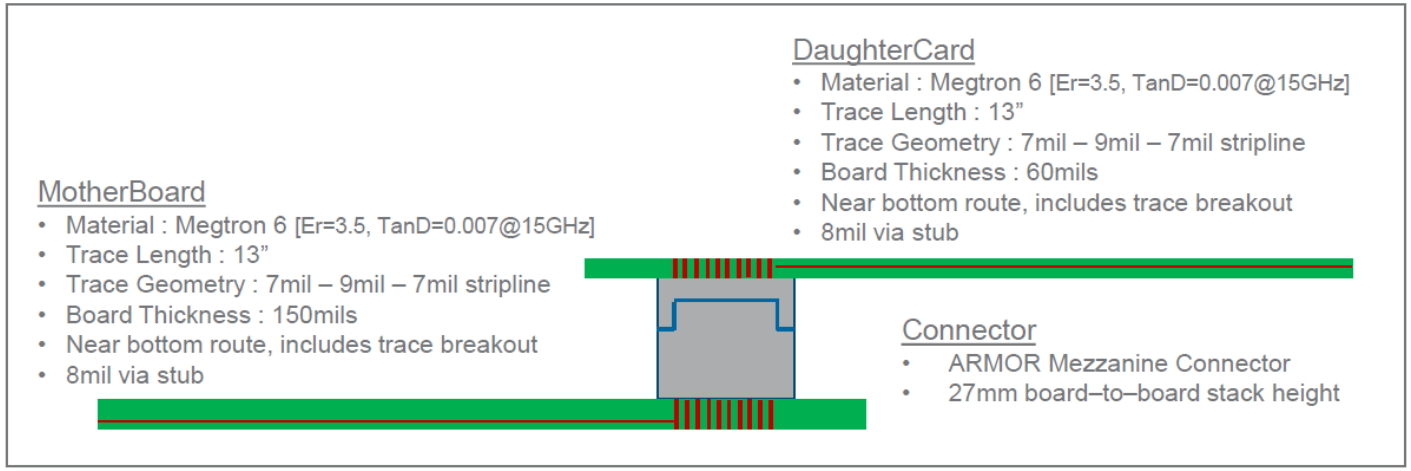
- Vasu Parthasarathy, Broadcom
- Beck Mason, JDSU
- Sudeep Bhoja, Inphi
- Scott Powell, Clariphy
- Mike Furlong, Clariphy
- Nathan Tracy, TE
- Megha Shanbhag, TE

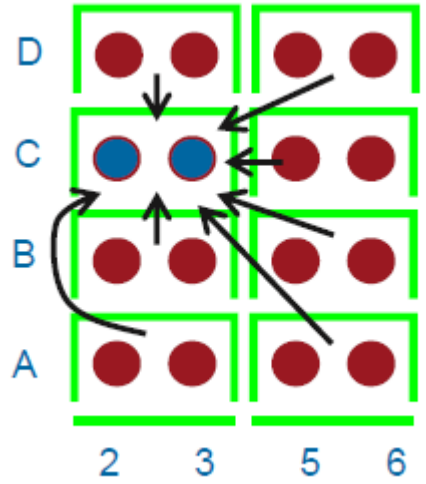
OVERVIEW

- **Channel**
  - Medium Reach, Chip to Chip channel
- **Simulation setup**
  - Data rate: 50Gbps
  - Signaling: PAM4
  - Signaling rate: 25.78125GBd
  - BER calculated from statistical analysis
- **Architecture**
  - Low power scheme
  - Extendable to higher loss channels

CHANNEL

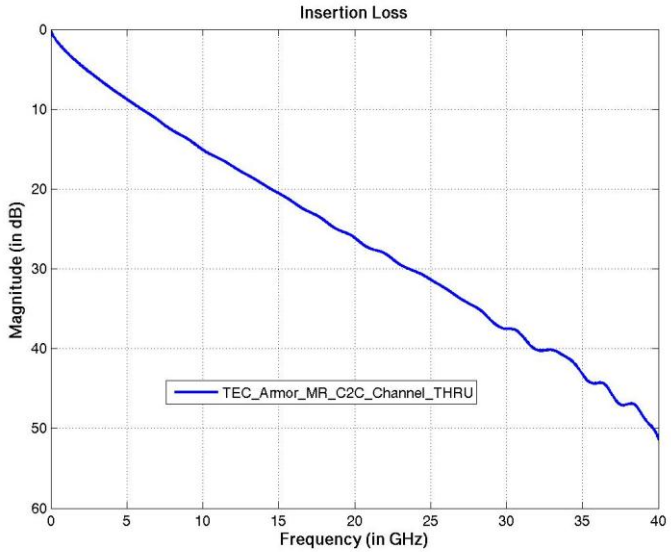
- **Source**
  - http://ieee802.org/3/bs/public/channel/TEC/shanbhag_02_0914.pdf (30-Sep-14)
  - Megha Shanbhag, Nathan Tracy, TE Connectivity
- **Channel**
  - Medium Reach/ Chip to Chip channel using a single connector (Armor)
  - Data based on simulations
  - IL: 18.2dB @12.9GHz
  - XT: 7 FEXT, 0 NEXT



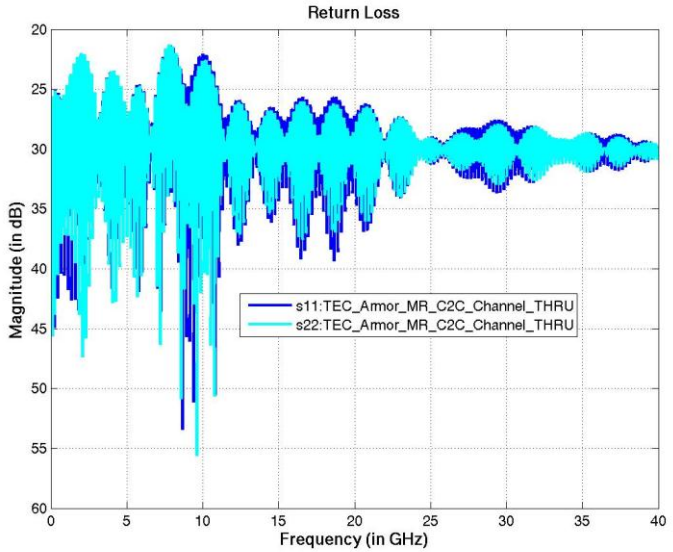


CHANNEL PARAMETERS

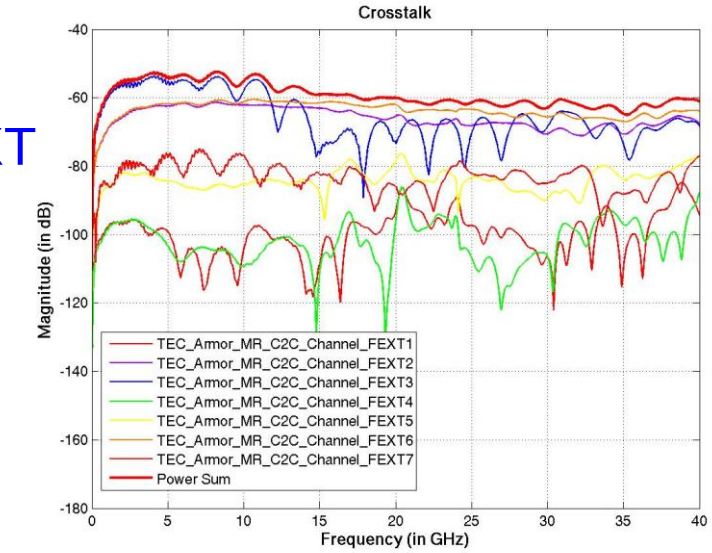
Channel IL



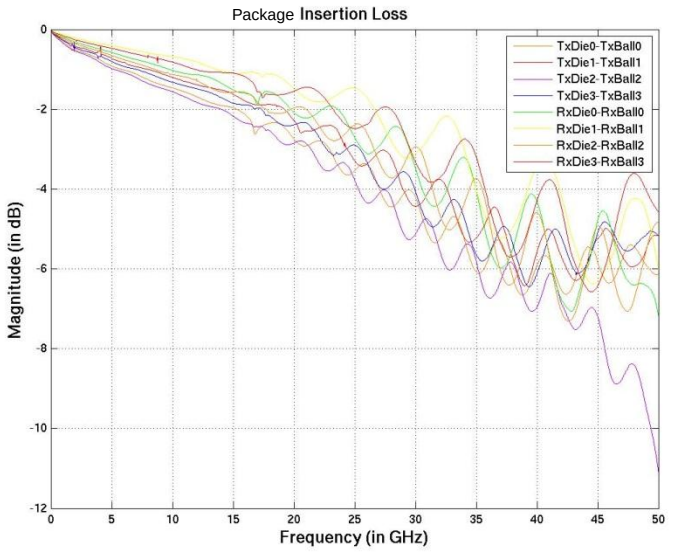
Channel RL



Channel XT

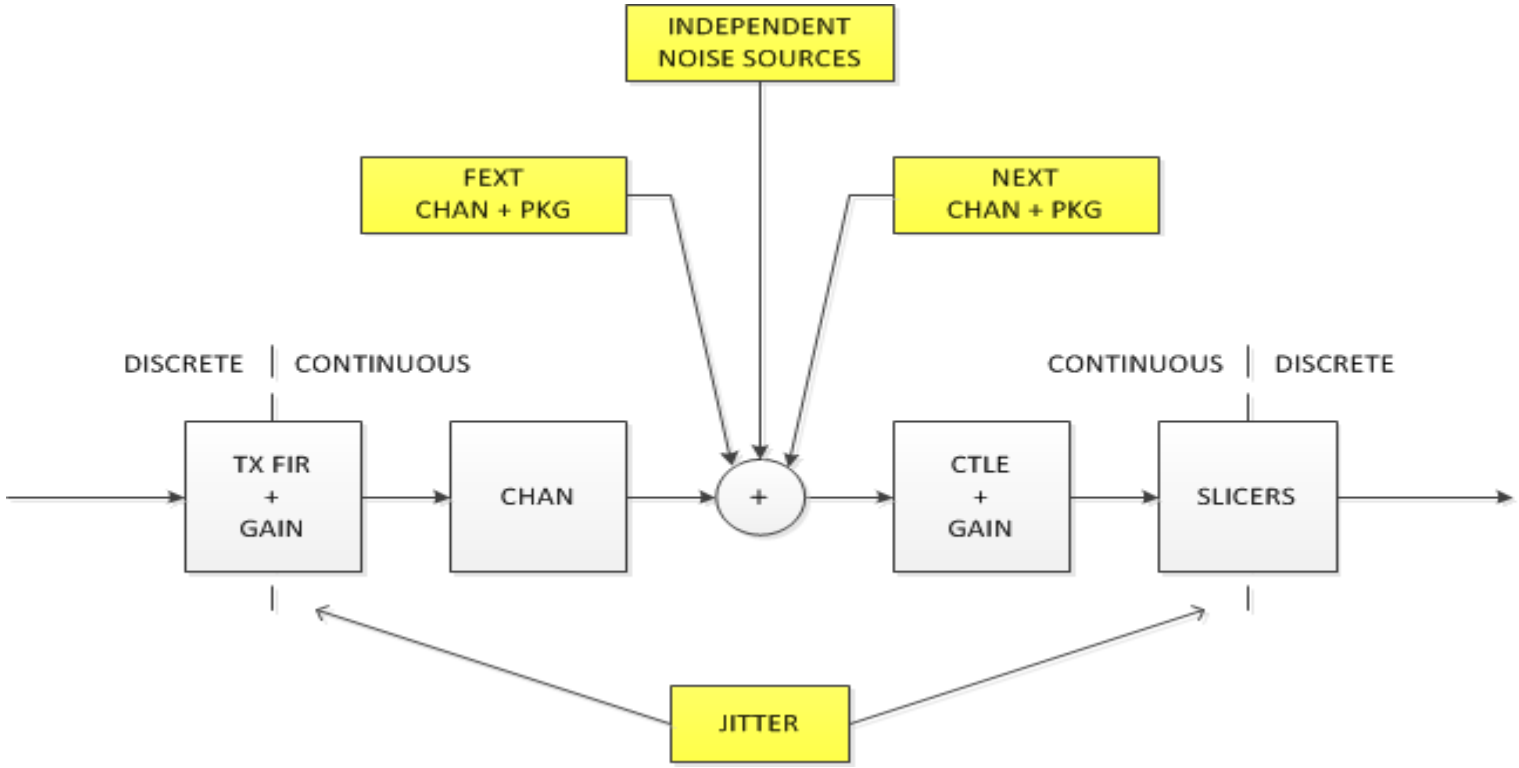


Package IL



TRANSCEIVER STRUCTURE

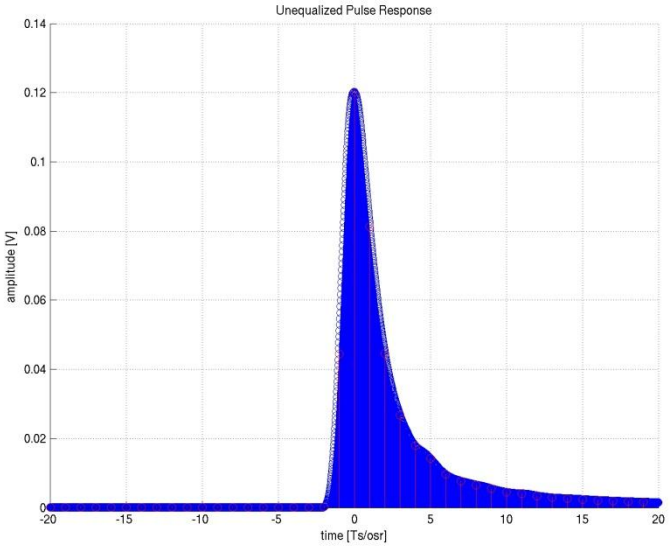
- **Signaling: PAM4**
- **Signaling rate: 25.78125 GBd**
- **CTLE**
  - **2 real zeros**
  - **2 real poles**
- **TXFIR**
  - **4 taps with 1 pre, 2 post**

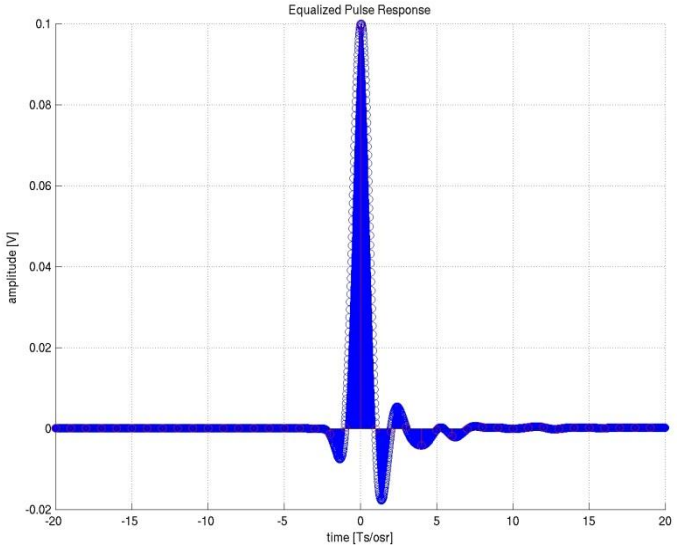


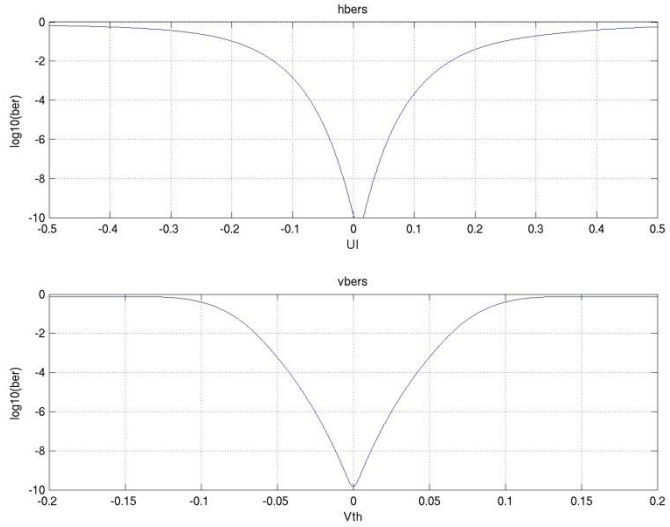
SIMULATED IMPAIRMENTS

- **Analog models based on existing 28nm, 25G NRZ Serdes IP**
- **ISI and Channel crosstalk driven by statistical worst-case sequences**
- **Package models based on large ASIC (60mmx60mm)**
  - Insertion loss of ~1.6dB on each side of the link
  - 4 NEXTs, 3 FEXTs
- **End-to-end insertion loss: 21.4dB (pkg+channel+pkg)**
- **Rx input referred AWGN: 1.6mV rms (-155dBm/Hz)**
- **Jitter: ~0.24UI pp (20mUI Tx DCD, 13mUI Tx PJ, 0.1UI Tx RJ, 0.1UI Rx RJ, 70mUI Rx DJ)**
- **Slicer offsets: ±2%**

EQUALIZATION PERFORMANCE







Normalized to an ideal eye opening of [-0.1,0.1])

RESULTS SUMMARY

Metric	Value
BER (pre-FEC)	**$1.4x10^{-10}$**
Vertical EO @ 1e-6	**50mVpp**
Horizontal EO @ 1e-6	**95mUIpp**

- **Sufficient BER to reach error free performance after simple FEC**
- **IEEE 802.3bj 100GBASE-KR4 FEC has no overhead and 4.9dB coding gain**
- **With 4.9dB of coding gain, BER < 1e-27**

CONCLUSIONS

- **Simple scheme, allows low-power implementation**
- **No DFE ➔ No error propagation issues**
- **Can easily meets BER requirement of 10^{-18} with simple FEC**
- **Extendable to LR channels**
  - May need additional mechanisms (coding, precoding, etc.)