Relative FEC Area Comparison

IEEE P802.3bs 400 Gb/s Ethernet Task Force

January 2015 Atlanta

Ian Dedic - Fujitsu
Mark Gustlin – Xilinx
Martin Langhammer - Altera
Jeff Slavick – Avago
Xinyuan Wang - Huawei
Zhongfeng Wang - Broadcom

Introduction

- This short presentation compares FEC sizing between several FECs that have been discussed in the task force
- The comparison is made at 100G, not 400G
- Also important is the power of the FECs, this is not covered in this presentation, but can be looked at in future work

100G FEC Comparison

- This is a comparison of FEC Decoder Area (ASIC gates or Luts)
  - Area A: Martin Langhammer - Altera
  - Area B: Zhongfeng Wang - Broadcom
  - Area C: Ian Dedic - Fujitsu
  - Area D: Jeff Slavic - Avago
  - Area E: Xinyuan Wang - Huawei
- The comparisons are not perfect, there are frequency variations, achievable latency variations etc. But they give a flavor of the comparable complexity of these FEC options

Type	Code word	Area A (luts)	Area B (gates)	Area C (gates)	Area D (gates)	Area E (gates)
RS KR4	(528,514,7)	10.6k	140k		250k	103k
RS KP4	(544,514,15)	26.5k			665k	228k
RS KR/P4					915k	
BCH1	(2858,2570,24)	106.8k	1.2M			
BCH1a	(2288,2048,20)		980k	750k		
BCH2	(9193,8192,71)	425k	4M			

100G FEC Comparison

- This is a comparison of **relative** FEC Decoder Area (Gates or Luts)
  - Area A: Martin Langhammer - Altera
  - Area B: Zhongfeng Wang - Broadcom
  - Area C: Ian Dedic - Fujitsu
  - Area D: Jeff Slavic - Avago
  - Area E: Xinyuan Wang - Huawei

Type	Code word	Area A	Area B	Area D	Area E
RS KR4	(528,514,7)	1	1	1	1
RS KP4	(544,514,15)	2.5		2.7	2.2
RS KR/P4				3.7	
BCH1	(2858,2570,24)	10	8.6		
BCH1a	(2288,2048,20)		7		
BCH2	(9193,8192,71)	40	28.6		

Thanks!