SEMTECH

100Gb/s/Lambda 2km PAM4 Big Ticket Items

(Addressing Page 21 of big_ticket_items_3bs_01_0115)

Alan Tipper

Supporters & Contributors

- Contributors
  - Chris Fludger, Cisco
- Supporters
  - Vipul Bhatt, Inphi
  - William Bliss, Broadcom
  - Dave Brown, Semtech
  - Keith Conroy, Multiphy
  - Dave Lewis, JDSU
  - Jeff Maki, Juniper
  - Gary Nicholl, Cisco
  - Mark Nowell, Cisco
  - Bharat Tailor, Semtech

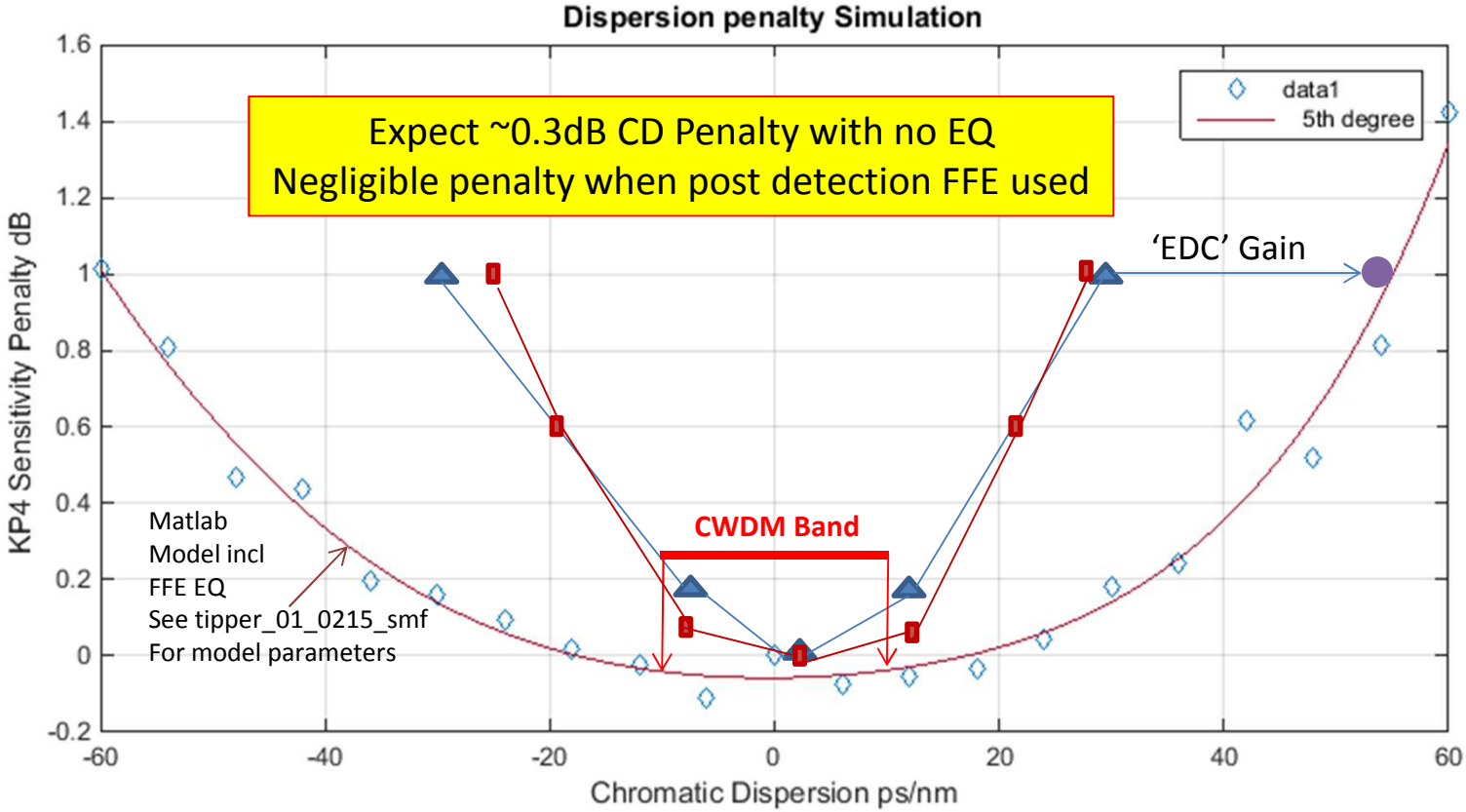
Big Ticket Items

- Lewis_3bs_01_0315 (4 x 100G PAM4 Proposal)
  - Allocation for MPI penalty 1.0 dB
  - TDP 1.5dB
- Minutes_draft_2-Feb-2015_smf.

  BTIs common to all proposals:
  - **Dispersion penalty worst case**, TDP
  - **RX sensitivity / technical feasibility**
  - **MPI**
  - More test results
  - Evaluate Coupling between electrical and optical interfaces
- Follow 802.3ba 100G BASE-LR4 Methodology
  - Generate Baseline Proposal by modeling Chromatic dispersion with realistic Chirp effects
    - Traverso_01_0907 (Model Sims) -> COLE_01_0308 ->COLE_01_0508 (Baseline)
  - Seek to refine the baseline with measurement data during detailed spec discussions
    - Isono_01_0708

CD Simulations: 53Gbaud PAM4 with KP4 FEC

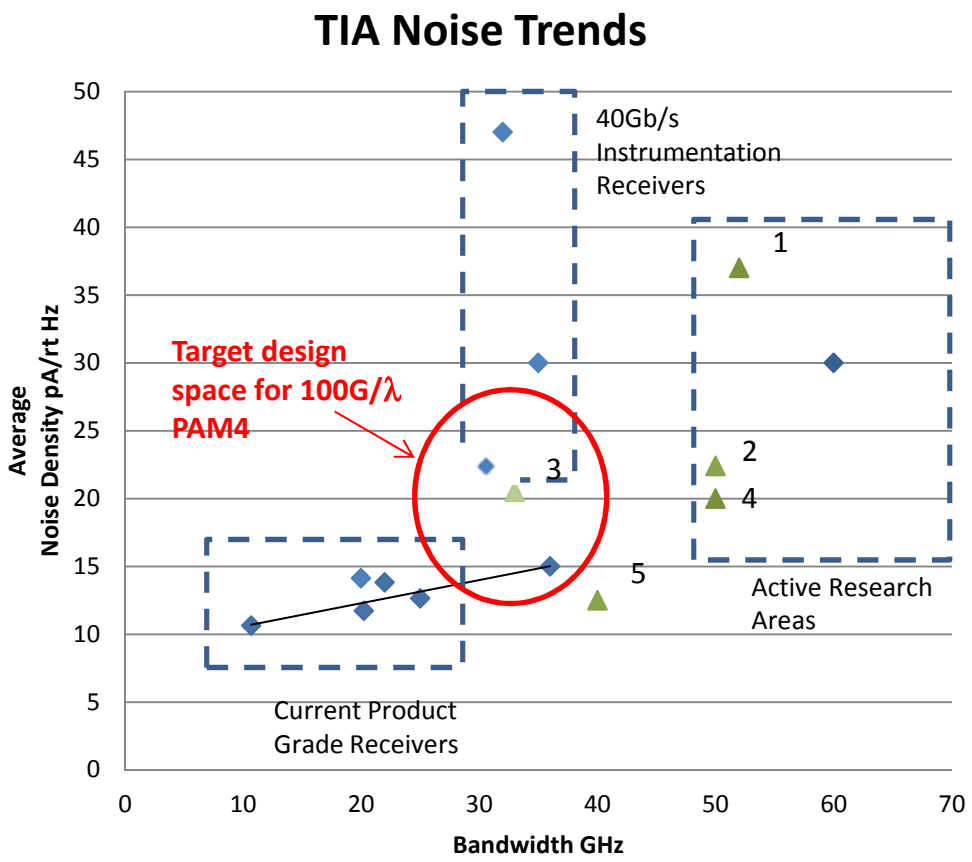
Update to Tipper_01_0215_smf



- Chris Fludger, Cisco: 51.6Gbd PAM4 VPI Simulations (High ER, unchirped Modulator, no EQ) rescaled from http://www.ieee802.org/3/100GNGOPTX/public/mar12/plenary/nicholl_01b_0312_NG100GOPTX.pdf
- No EQ Simulations, ideal High BW Tx & Rx zero chirp MZI
- Based on NRZ SMF-EDC Experiments at 10Gb/s ref: S. L. Woodward et al, Demonstration of an Electronic Dispersion Compensator in a 100-km 10-Gb/s Ring Network. IEEE PHOTONICS TECHNOLOGY LETTERS, VOL. 15, NO. 6, JUNE 2003 (shows doubling of SMF-CD limit with EAM Tx using FFE)

RX Sensitivity / Technical Feasibility

Update to Tipper_01_3bs_0914



1. Monolithic Photorecievers for 60 Gbits/s and Beyond
H.-G. Bach
OFC 2003 ThZ1

2. A 50-Gb/s Differential Transimpedance Amplifier in 65nm CMOS Technology
Sang Gyun Kim, Seung Hwan Jung, Yun Seong
Taiwan Asian Solid-State Circuits Conference
IEEE November 10 - 12, 2014/Kaohsiung,

3. A 40-Gb/s Optical Transceiver Front-End in 45 nm SOI CMOS
Joohwa Kim, and James F. Buckwalter
IEEE JOURNAL OF SOLID-STATE CIRCUITS,
VOL. 47, NO. 3, MARCH 2012

4. SiGe Differential Transimpedance Amplifier With 50-GHz Bandwidth Joseph S. Weiner, Andreas Leven, Vincent Houtsma, Yves Baeyens, Young-Kai Chen, Peter Paschke, Yang Yang, John Frackoviak, Wei-Jer Sung, Alaric Tate, Roberto Reyes, Rose F. Kopf, and Nils G. Weimann
IEEE JOURNAL OF SOLID-STATE CIRCUITS,
VOL. 38, NO. 9, SEPTEMBER 2003

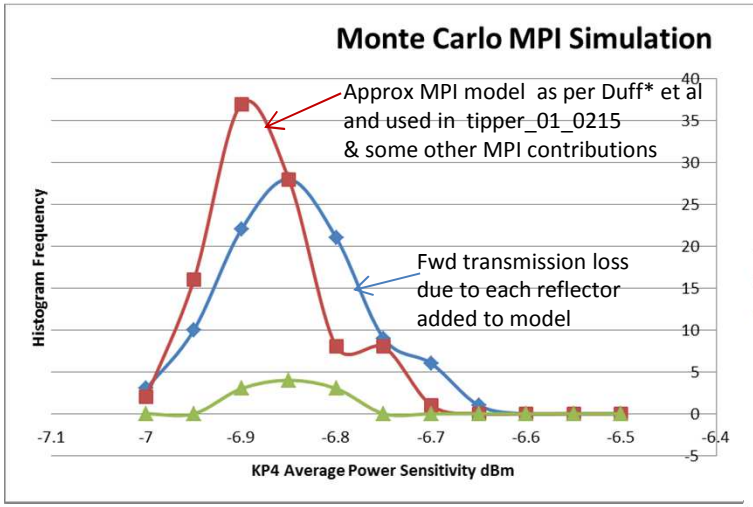
5. A 40-GHz Bandwidth Transimpedance Amplifier with Adjustable Gain-Peaking in 65-nm CMOS
Ran Ding,y Zhe Xuan, Tom Baehr-Jones, Michael Hochberg
2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS),

- Commercial deployments
- Research Publications

The TIA design space for 100Gb/s/λ PAM4
Is an extension of existing 25Gb/s & 40Gb/s product technology and not dependant upon 'Futuristic Technology Research'

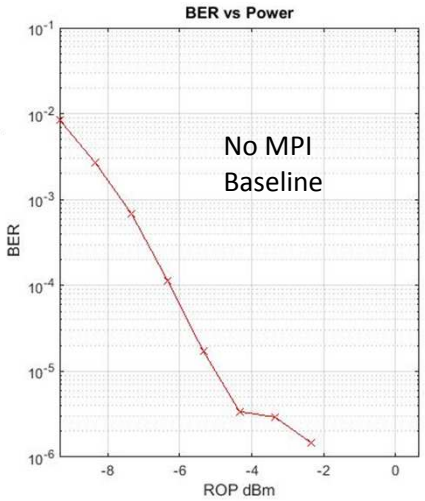
MPI: Monte Carlo Simulation

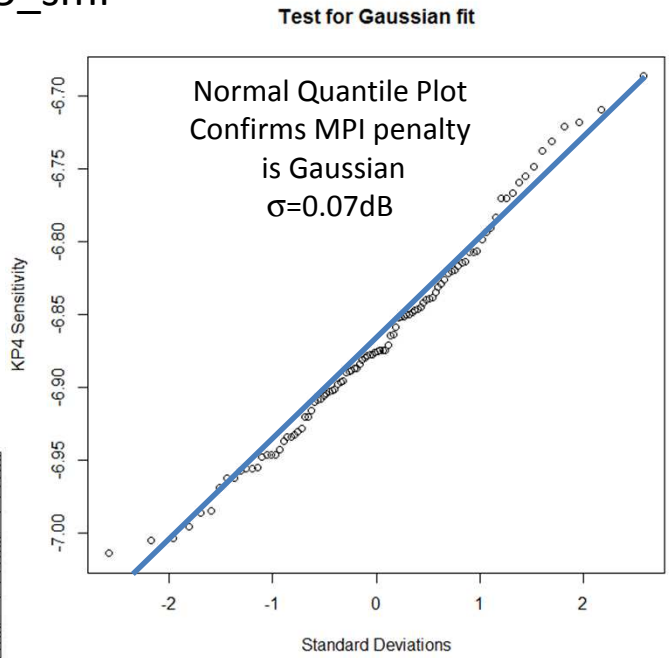
4 x 26dB connectors + Tx & Rx Reflectance with Randomized reflection phase & delay
Update to Tipper_01_0215_smf



Model uses variable seed random number generators so some inherent variability In error counts

Exact Scattering Model N=100
Approx scattering Model N=100
Repeatability with no MPI N=10



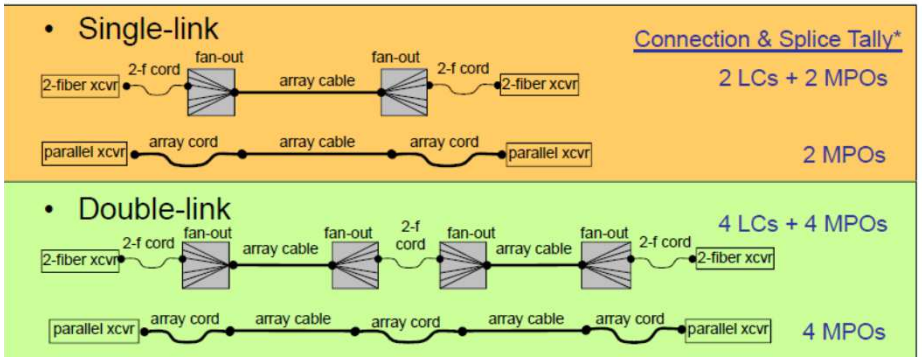


Methodology: Time Domain simulation with cascaded random scattering matrices in The SMF path. Chirp & Chromatic Dispersion Effects included. Scattering loss included.

* DANIEL A. FISHMAN, DONALD G. DUFF,JONATHAN A. NAGEL
Measurements and Simulation of Multipath Interference tor 1.7-Gb/s Lightwave Transmission Systems Using Single and Multifrequency Lasers
JOURNAL OF LIGHTWAVE TECHNOLOGY. VOL. 8. NO. 6, JUNE 1990

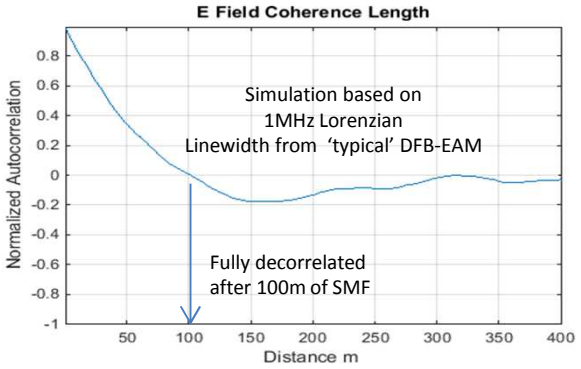
Numerical trials with randomized reflection phases & path delays suggest 0.5dB is adequate for MPI penalty with 26dB connectors.

Upper Bound MPI requires that all reflected signals remain coherent over multiple reflection paths



Decorrelated
After 48m* Array Cable
3dB unused margin
From lack of connector
& short link plant loss

Decorrelated
After 23.5m* Array Cables
1.3dB unused margin
From lack of connector
& short link plant loss



Source: kolesar_3bs_01_0514

* Assumes 2m patch cords, 1MHz linewidth Source 26dB connector reflectivity, connector losses as per Kolesar_3bs_01_0514

Note that due to return path reflection the separation between connectors is 0.5x the above distance

More work needed at detailed spec stage
To determine if linewidth contraints are needed
(& verification of 56Gbaud Tx line widths)

Most likely coherent MPI scenario is very short
Single-Link where there is 3dB loss margin
+ 1dB MPI margin available which is adequate

Summary

- CD Penalties for Equalized 2km 4 x 100G CWDM PAM4 should be negligible. Unequalized schemes should show < 0.3dB
  - Penalties should be even smaller for 500m PSM4 links
- Rx Technology is an extension of existing designs at 25Gb/s and 40Gb/s and is not dependant upon fundamental research work. Current research frontier is low noise 50GHz+ bandwidths which is well beyond what we need for 100Gb/s/λ PAM4 (~30GHz).
- End to End Monte-Carlo Simulations of 100Gb/s PAM4 assuming KP4 FEC indicates 0.5dB MPI link budget penalty is sufficient with 99.98% confidence for 6 reflections with 26dB back reflection and low loss
  - This will be significantly reduced by realistic connector return losses >>26dB
- Upper Bound MPI restricted to very short links where link margin is available
  - More work needed to determine likely Tx linewidth range
- 1dB Path penalty for MPI and 1.5dB for TDP is sufficient.