Proposed Changes for PCS Lane Forming

IEEE P802.3bs 400 Gb/s Ethernet Task Force

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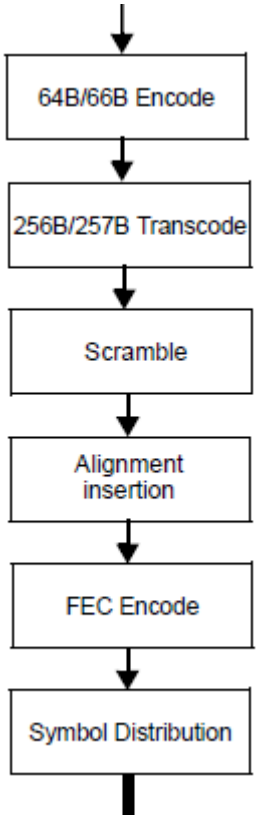
Introduction

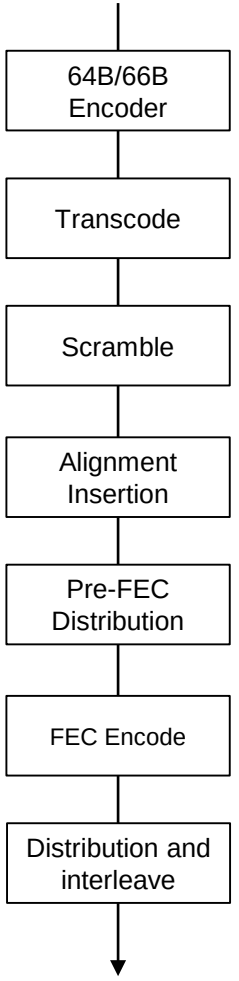
- This slide deck looks at how to form the FEC codewords and play that data out
  - Looking at how data is played into the two FEC codewords
  - Looking at how data is played out of the two FEC codewords into PCS lanes
- Also to be presented is a marked up draft of Clause 119
- In the September meeting, we adopted the interleaving of two FEC codewords:
  - Motion #4: Move to adopt symbol interleaving from two FEC codewords as the basis for forming the 16 PCS lanes
    - Y: 70 N: 0 A: 14

Modified TX Block Diagram

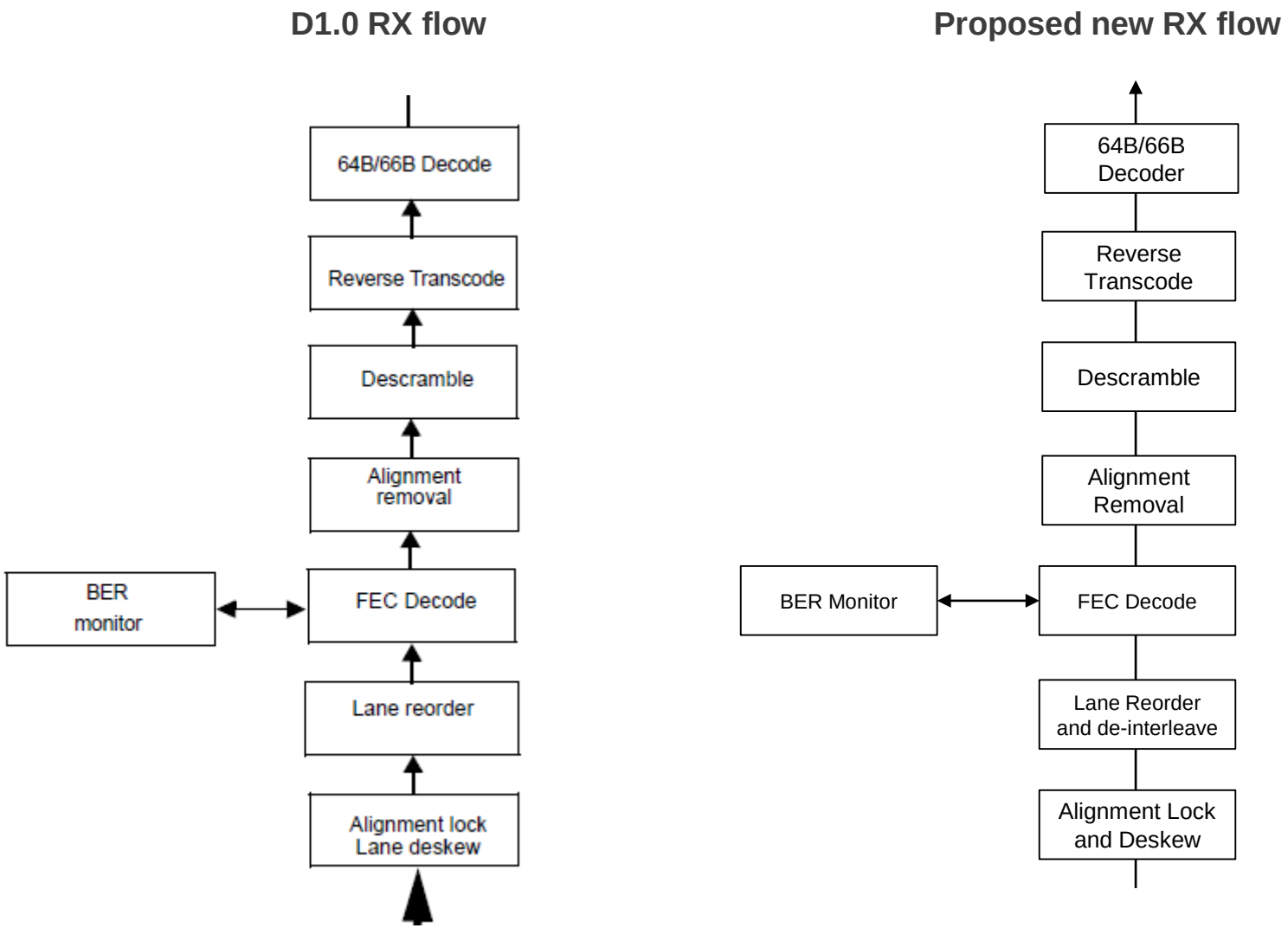
D1.0 TX flow



Proposed new TX flow



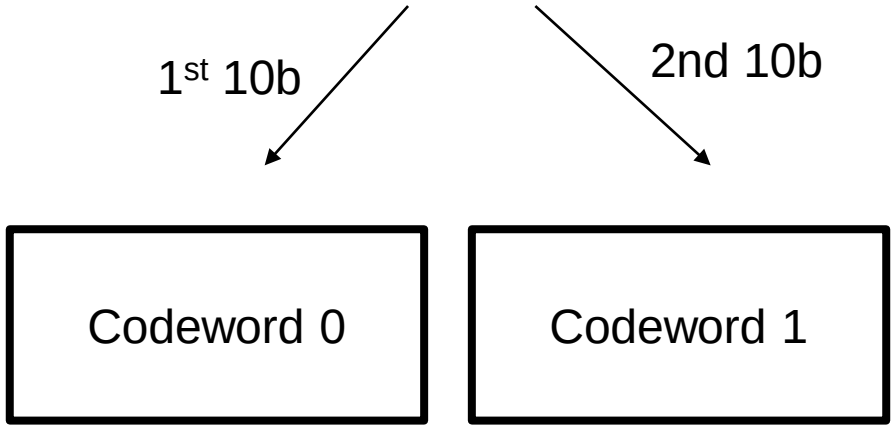
Modified RX Block Diagram



Data Into the two Codewords

- We looked at parallel and serial filling of the two FEC codewords
- Parallel filling has a small latency advantage, but a small gain disadvantage
- Serial filling is the reverse
- The performance delta was shown in anslow_01_1015_logic.pdf
- The latency delta is ~12.5ns

- The consensus of the discussions is to do a parallel fill on a 10b striping basis



Data Out of the two Codewords

- Two methods were looked at, playing 160b out of the codewords at a time in a round robin fashion, or 10b at a time
  - Option A and B from bliss_3bs_01_0915.pdf
- Option B is the consensus choice
  - Can be some gain in performance for a design that is end to end 8 lanes with no skew within a group of two PCS lanes

Conclusion

- The proposal is to implement the changes as shown in gustlin_3bs_02_1115, which is a marked up version of draft 1.0 clause 119

Thanks!