TX DIFFERENTIAL PRECODER SIMULATION RESULTS & PROPOSAL FOR CDAUI-8 C2C

Raj Hegde & Magesh Valliappan
IEEE 802.3 400Gb/s Task Force
IEEE 802.3 Plenary Session, Nov. 2015, Dallas, TX

SUPPORTERS

- Upen Reddy Kareti, Cisco

- Marco Mazzini, Cisco

- Adee Ran, Intel

- Geoff Zhang, Xilinx

- Vipul Bhatt, Inphi

- Arash Farhood, Inphi

- Venu Balasubramonian, Marvell

- Yasuo Hidaka, Fujitsu Labs of America

- Arai Tomoyuki, Socionext

- Vasu Parthasarathy, Broadcom

- Will Bliss, Broadcom

- Pirooz Tooyserkani, Cisco

- Ali Ghiazi, Ghiazi Quantum

OUTLINE

- **Introduction**

- **Precoder performance in CDAUI-8**

- **Implementation complexity**

- **Proposal**

- **Summary**
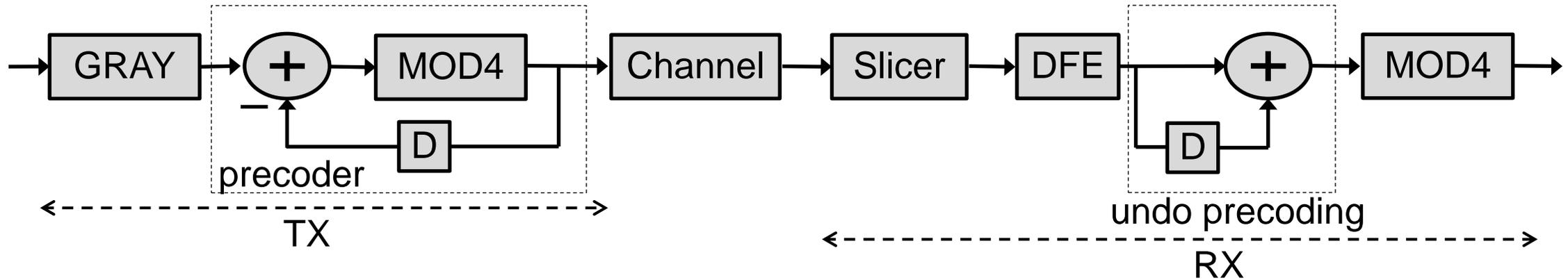
- **Burst Error in the DFE:**
  - Probability of k consecutive errors is a function of the first tap value:
    - Tap value of 1: 0.75^k, Tap value of 0.7: 0.72^k, Tap value of 0.6: 0.62^k

- **Differential Precoder reduces 1-tap DFE burst error runs into 2 errors per event**
 - Allows DFE taps not to be restricted while mitigating error-propagation risk.
    - RX implementations can take advantage of this feature
    - Tap restrictions for RX compliance (COM) can still remain
  - One error at the entry and one error at the exit
  - Useful in breaking up long bursts spanning multiple FEC symbols.

Option 8 from anslow_3bs_03_0915: Symbol interleave from 2 FEC code words and bit-muxing in the PMA

- Precoder allows **2x** relaxation in DER0 at FLR = 6.2e-11

- Precoder allows **4x** relaxation in DER0 at FLR = 6.2e-16

- Breaks up long error bursts and has steeper curve similar to a = 0.5

Case	DER0	BER	DER0	BER
FLR	6.2e-11		6.2e-16	
Random	6.4e-4	3.2e-4	3.0e-4	1.5e-4
a=0.5	2.0e-4	2.0e-4	5.3e-5	5.3e-5
a=0.5 + pre-coder	1.6e-4	1.6e-4	4.0e-5	4.0e-5
a=0.75	8.4e-5	1.7e-4	1.1e-5	2.1e-5
a = 0.75 + pre-coder	1.7e-4	1.7e-4	4.6e-5	4.6e-5
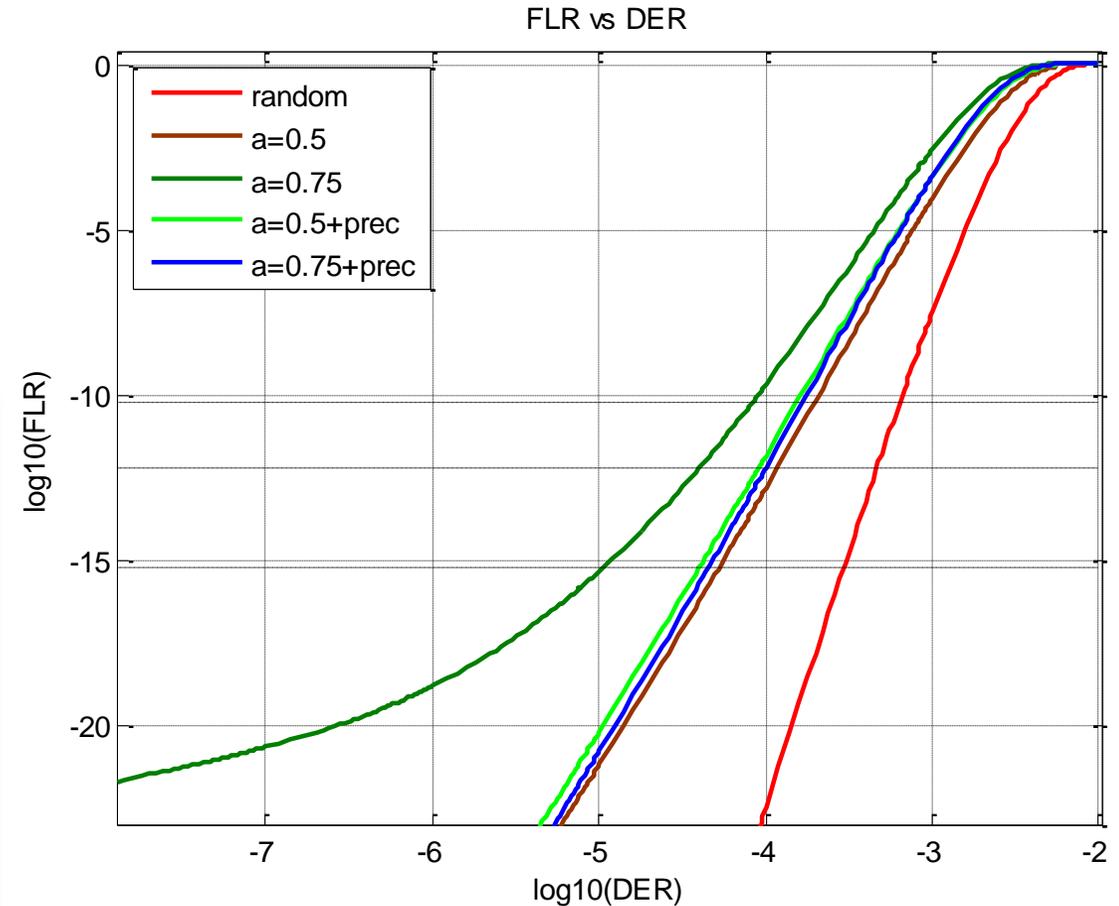
FLR vs DER

Legend:
- random
- a=0.5
- a=0.75
- a=0.5+prec
- a=0.75+prec

Option 8 from anslow_3bs_03_0915: Symbol interleave from 2 FEC code words and bit-muxing in the PMA

- Precoder allows **2.4x** relaxation in Electrical DER0 at FLR = 6.2e-11 with multi-part link with 0.1dB optical penalty (precoding on electrical links only)

Case	DER0	BER
Random	1.6e-4	8.0e-5
a=0.5	4.5e-5	4.5e-5
a=0.5 + pre-coder	3.5e-5	3.5e-5
a=0.75	1.6e-5	3.2e-5
a = 0.75 + pre-coder	3.8e-5	3.8e-5
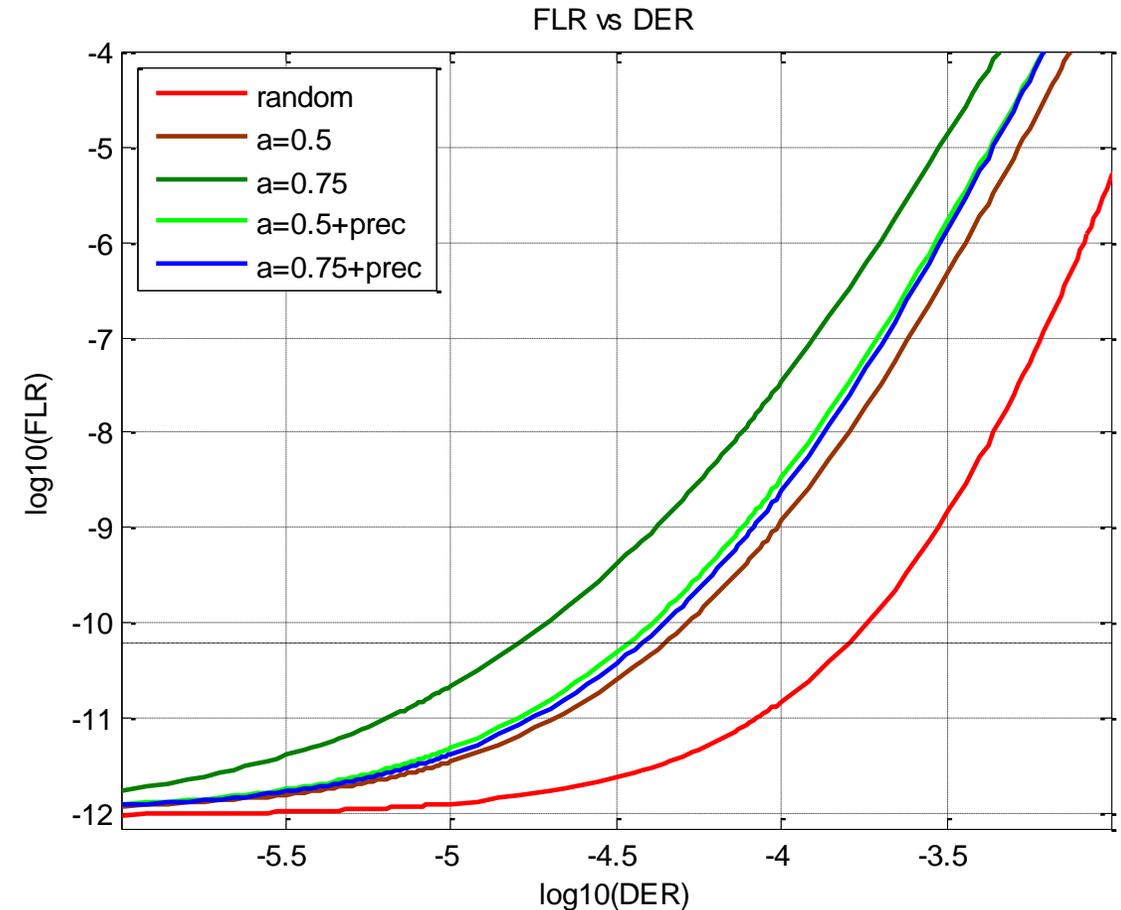
FLR vs DER

Option 8 from anslow_3bs_03_0915: Symbol interleave from 2 FEC code words and bit-muxing in the PMA

- Precoder allows **7.6x** relaxation in Electrical DER0 at FLR = 6.2e-16 with multi-part link with Optical BER = 1.1e-4 (precoding on electrical links only)

- When optical link has less margin, precoder helps electrical segments with a=0.75 more

Case	DER0	BER
Random	7.3e-5	3.7e-5
a=0.5	1.1e-5	1.1e-5
a=0.5 + pre-coder	8.6e-6	8.6e-6
a=0.75	1.3e-6	2.7e-6
a = 0.75 + pre-coder	9.9e-6	9.9e-6

FLR vs DER
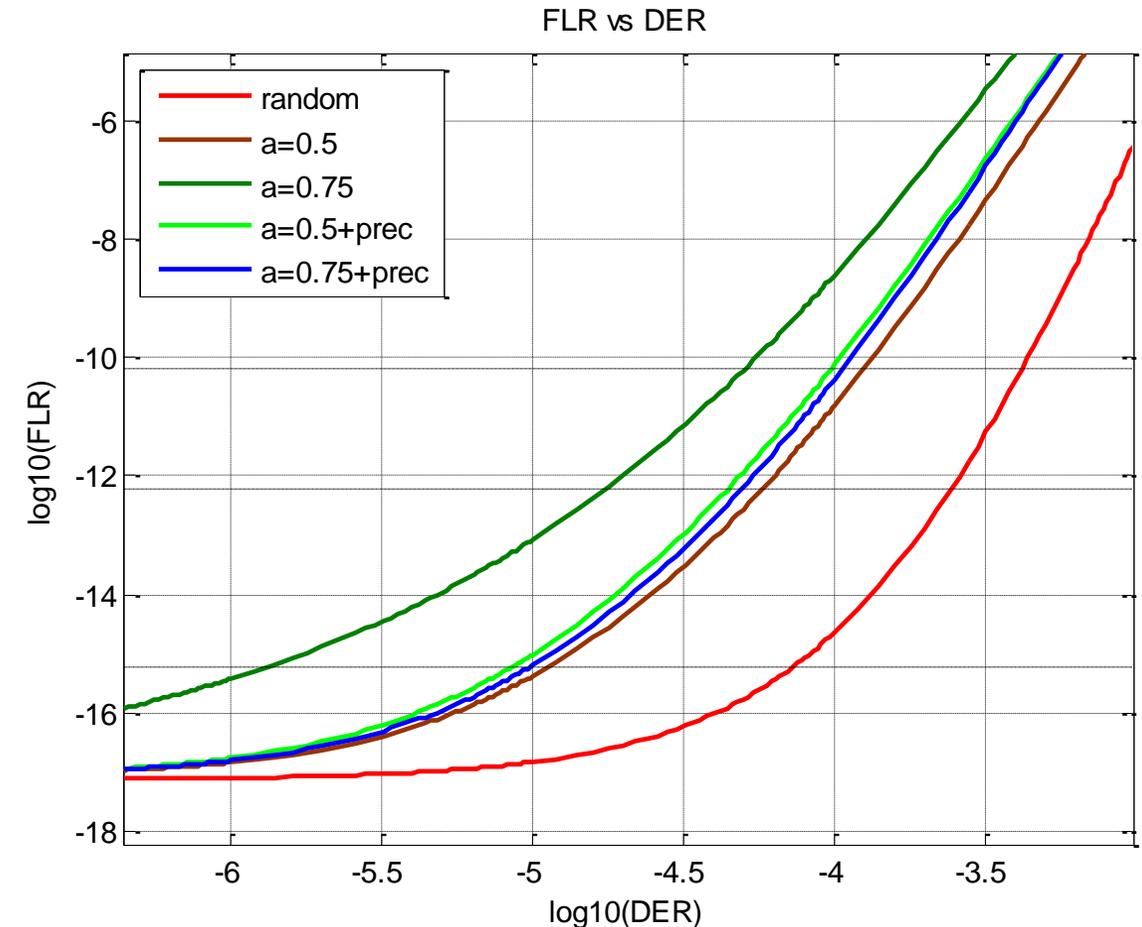
When a dominant 1st DFE tap is combined with smaller later taps, there is a small chance of a subsequent error burst to get triggered as the tail of the previous burst propagates through the DFE's pipeline. This reduces FEC performance, however precoder can still alleviate the impact, converting each to a start & stop error event.

- The later DFE taps determine the probability of a subsequent burst. For this calculation, a 2.5% probability was assumed. This is derived from what is needed to make a link with DFE tap1=0.5 behave like a=0.5 @ FLR = 6.2e-13.

- A pessimistic approximation was made that the subsequent bursts always cross over to a new RS symbol

- Precoder allows **2x** relaxation of DER0 at FLR = 6.2e-11
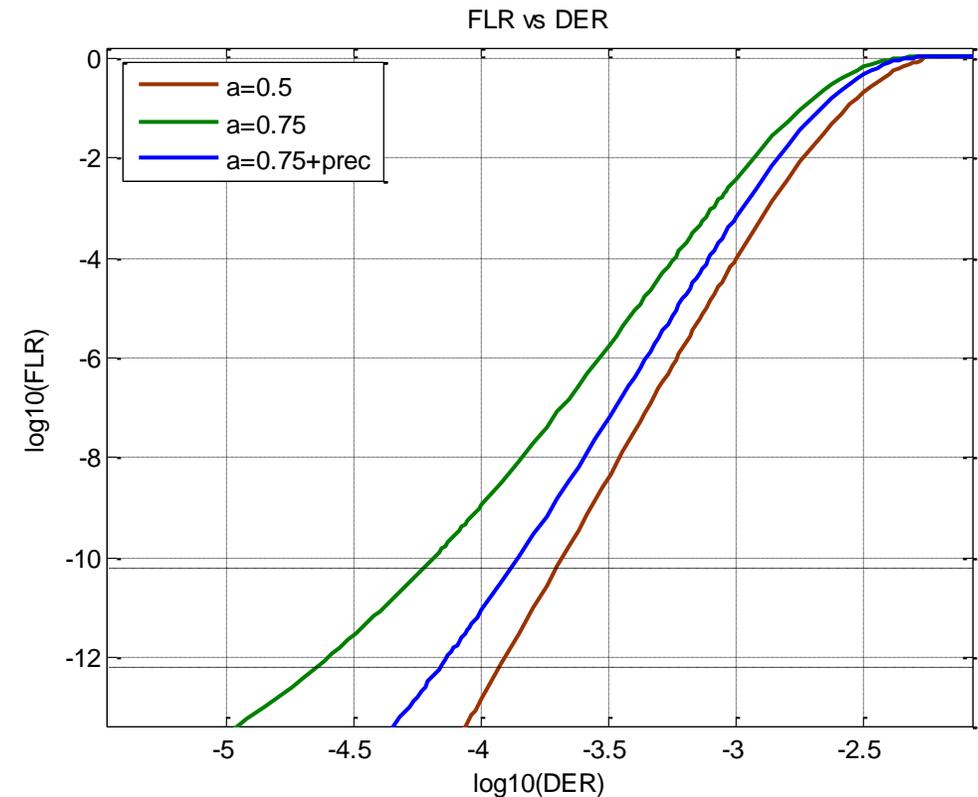
Case	DER0	BER
a=0.5 (single tap DFE)	2.0e-4	2.0e-4
a=0.75 + later DFE tap	6.0e-5	1.2e-4
a = 0.75 + pre-coder	1.3e-4	1.3e-4

FLR vs DER

PRECODER IMPLEMENTATION

- **Purely digital implementation**

- **Area estimate and gate-count for different levels of parallelization**

	10T (10 symbols/10T cycle)	16T	20T	32T
design area (um^2)	45	51	60	75
Gate count (NAND2X1 equivalent)	248	281	330	413

- **Timing closure wasn't an issue as well on a commercially available advanced CMOS process node.**

- **Requesting the optional-use precoder only for the CDAUI8 chip-to-chip TX PMA**

  - NOT for chip-to-module

  - NOT for the optical portion of the link

- **Re-use the language in 100G-BaseKP4 (94.2.2.6)**

- **Additional variables:**

  - A *binary variable* in the RX side that advertises its capability to decode precoded data and a *binary variable* to turn this decoder ON to be set by the station manager. These variables apply to all lanes

  - A *binary variable* in the TX that can turn on the precoder (to be set by the station manager)

  - Normative requirement that the TX variable shall match the RX variable

  - If MDIO is supported, the above variables shall be mapped to bits in MDIO space

CONCLUSIONS

- **Effective mechanism for burst error protection due to dominant 1st tap in the DFE**

  - Expands receiver design space.

- **Bypass-able option with minimal overhead**

- **Significant improvement in performance (pre-interleaved case) with inexpensive implementation**

- **Allows FEC code word interleaving to handle other sources of correlated errors**

- **Provides lane-level mitigation against lane-level DFE generated burst errors**

  - Lane-level protection allows extension to other PAM4 AUI configurations where interleaving multiple FEC code words may not be feasible

- **No impact to an RX that doesn't need it**

For electrical sub-links in Multi-Part links with a penalty of ~0.1dB in the optical sub-link

	FLR = 6.2e-11	
	DER0	BER
Random (No DFE)	1.60E-04	8.02E-05
a=0.5	5.19E-05	5.19E-05
a=0.75	3.67E-07	7.34E-07
a=0.75 precoded	2.66E-05	2.66E-05

DER0 is the Detector Error Ratio as defined in COM

- Almost 2 orders of magnitude improvement in DER0/BER for DFE tap value ~ 0.7 to 1.0