Per-Lane CTLE

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CFP4 Form Factor

	CFP4 Bottom
1	3.3V_GND
2	3.3V_GND
3	3.3V
4	3.3V
5	3.3V
6	3.3V
7	3.3V_GND
8	3.3V_GND
9	VND_IO_A
10	VND_IO_B
11	TX_DIS *(PRG_CNTL 1)*
12	RX_LOS *(PRG_ALRM 1)*
13	GLB_ALRMn
14	MOD_LOPWR
15	MOD_ABS
16	MOD_RSTn
17	MDC
18	MDIO
19	PRTADR0
20	PRTADR1
21	PRTADR2
22	VND_IO_C
23	VND_IO_D
24	VND_IO_E
25	GND
26	*(MCLKn)*
27	*(MCLKp)*
28	GND

	CFP4 Top
56	GND
55	TX3n
54	TX3p
53	GND
52	TX2n
51	TX2p
50	GND
49	TX1n
48	TX1p
47	GND
46	TX0n
45	TX0p
44	GND
43	*(REFCLKn)*
42	*(REFCLKp)*
41	GND
40	RX3n
39	RX3p
38	GND
37	RX2n
36	RX2p
35	GND
34	RX1n
33	RX1p
32	GND
31	RX0n
30	RX0p
29	GND

Toward Host

(pin views from top)

REFCLK
(Optional)

MCLK = TX_MCLK + RX_MCLK
(Optional)

TX_DIS *(PRG_CNTL 1)*
(Optionally configurable as Progammable Control after Reset)

RX_LOS *(PRG_ALRM 1)*
(Optionally configurable as Progammable Alarm after Reset)

Connector contacts for 4 TX and 4 RX differential pairs

TX contacts and RX contacts are both on the top row of connector

PCB routing often can be made such that a per-module CTLE value is sufficient for CAUI-4

(Note that the CFP MSA does define per-lane CTLE management although the 802.3 defines only per-module)

CFP8 Form Factor

	CFP8 Bottom			CFP8 Top		Toward Host
1	GND		124	GND		
2	TX15n		123	TX14n		
3	TX15p		122	TX14p		(pin views from top)
4	GND		121	GND		
5	TX13n		120	TX12n		
6	TX13p		119	TX12p		
7	GND		118	GND		
8	TX11n		117	TX10n		
9	TX11p		116	TX10p		
10	GND		115	GND		
11	TX9n		114	TX8n		
12	TX9p		113	TX8p		
13	GND		112	GND		
14	TX7n		111	TX6n		
15	TX7p		110	TX6p		
16	GND		109	GND		
17	TX5n		108	TX4n		
18	TX5p		107	TX4p		
19	GND		106	GND		
20	TX3n		105	TX2n		
21	TX3p		104	TX2p		
22	GND		103	GND		
23	TX1n		102	TX0n		
24	TX1p		101	TX0p		
25	GND		100	GND		
26	GND *(VND_IO_A)*		99	*REFCLKn (VND_IO_E)*		*REFCLK (optional)*
27	3.3V		98	*REFCLKp (VND_IO_D)*		
28	3.3V		97	GND		
29	3.3V		96	TX_DIS *(PRG_CNTL1)*		GND *(tied to host GND)*
30	3.3V		95	RX_LOS *(PRG_ALRM1)*		
31	3.3V		94	MOD_LOPWR		
32	3.3V		93	MOD_ABS		MOD_ABS *(tied to module GND)*
33	3.3V		92	MDC		
34	3.3V		91	MDIO		
35	GND		90	MOD_SELn		
36	*MCLKn (VND_IO_B)*		89	GLB_ALRMn		*MCLK (optional) = TX_MCLK + RX_MCLK*
37	*MCLKp (VND_IO_C)*		88	MOD_RSTn		
38	GND		87	GND		
39	RX15n		86	RX14n		
40	RX15p		85	RX14p		
41	GND		84	GND		
42	RX13n		83	RX12n		
43	RX13p		82	RX12p		
44	GND		81	GND		
45	RX11n		80	RX10n		
46	RX11p		79	RX10p		
47	GND		78	GND		
48	RX9n		77	RX8n		
49	RX9p		76	RX8p		
50	GND		75	GND		
51	RX7n		74	RX6n		
52	RX7p		73	RX6p		
53	GND		72	GND		
54	RX5n		71	RX4n		
55	RX5p		70	RX4p		
56	GND		69	GND		
57	RX3n		68	RX2n		
58	RX3p		67	RX2p		
59	GND		66	GND		
60	RX1n		65	RX0n		
61	RX1p		64	RX0p		
62	GND		63	GND		

Connector contacts for 16 TX and 16 RX differential pairs

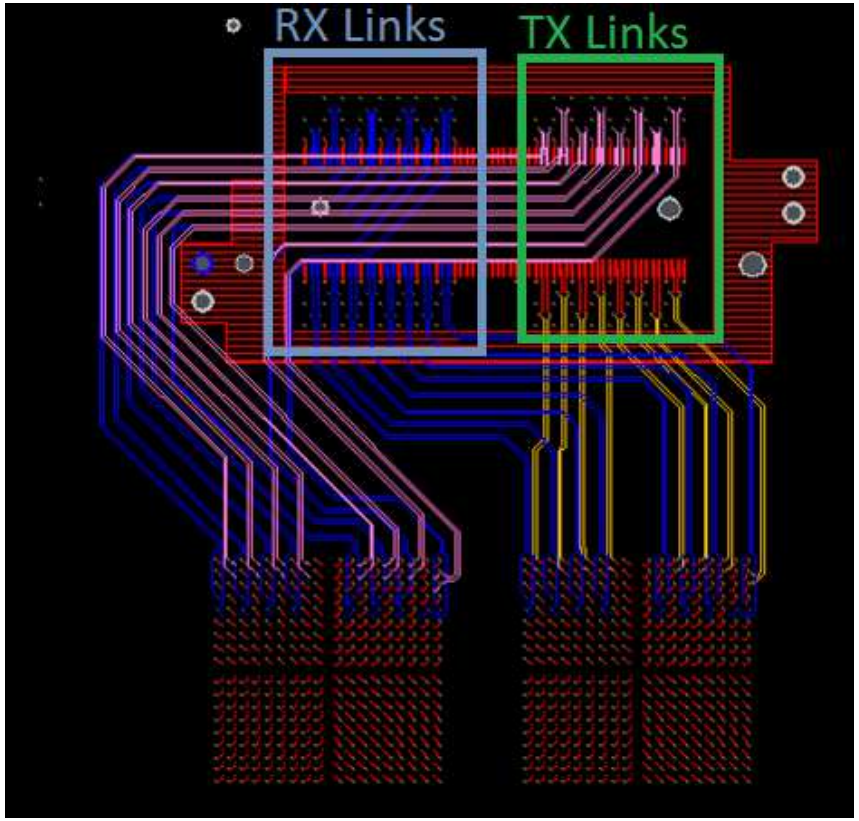
TX contacts on top and bottom row of connector

RX contacts on top and bottom row of connector

PCB routing cannot easily be made such that a per-module CTLE value is sufficient for CDAUI-16

- Paths would become excessively serpentine to match path lengths, which takes up board space and increases path lengths

CFP8 PCB Routing Study



Yellow differential-pair traces are for the top row TX

Magenta (pink) differential-pair traces are for the bottom row TX

Length variation between the top and bottom row TX lanes is more than 2 inches

Recommended CTLE setting cannot be the same for all lanes

Comment #39 – Juniper

Cl **45** *SC* **45.2.1.116a** *P* **44** *L* **8**

Maki, Jeffery Juniper Networks

Comment Type **TR**

Table 45–90a. CDAUI-16 chip-to-module recommended CTLE register bit definitions need to be per lane and not per module. PCB routing studies for CFP8 connectors show it to be problematic to match the length of all chip-to-module traces sufficiently for the TX links. The length variation between the bottom row TX lanes and top row TX lanes is more than 2 inches. (See the pink and yellow traces in the drawing with filename "CFP8 PCB Routing Example.png")

Suggested Remedy

Define Register 1.499 to be per-lane for setting of the CTLE recommended value for this 16 lane interface.

Comment #136 – Cisco

Cl **45** *SC* **45.2.1.116a** *P* **44** *L* **2**

Nicholl, Gary Cisco Systems

Comment Type **TR**

The current text only specifies a single recommended CTLE setting register for all 16 lanes of a CDAUI-16 chip-to module interface. In keeping with all CAUI-4 module implementations there should be a separate recommended CTLE register for each individual CDAUI-16 lane. A single register (and CTLE setting) for all 16 lanes is too restrictive. The whole point of the MLD protocol was to allow board designers flexibility in routing of the individual lanes of a CAUI-4 or CDAUI-16 interface.

Suggested Remedy

Please add a 'recommended CTLE setting' register for each individual lane of the CDAUI-16 chip-to-module interface.

Conclusions

Per-module CTLE setting is not sufficient for CDAUI-16 C2M

Need to provision for per-lane CTLE settings so that implementations route the required 16-lane wide connector (whatever it is) without unnecessary lane-length matching

Note towards CDAUI-8 C2M

- Autonomous self-adaption of CTLE should not presume each of the 8 lanes will require the same value