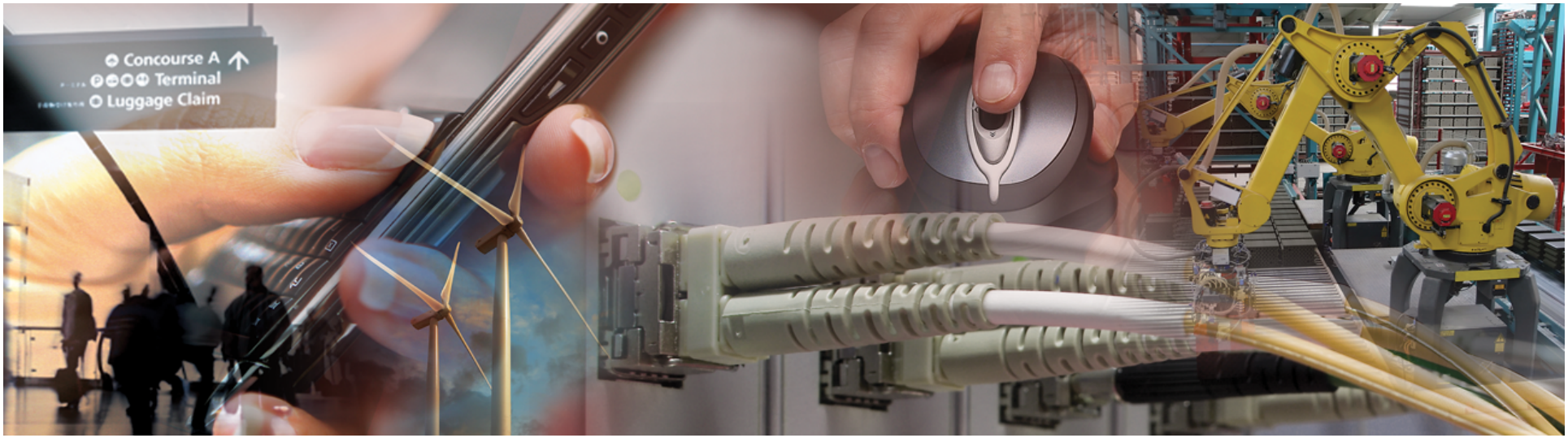
# Supporting material for comment #46




Jeff Slavick

*Cl* **119** *SC* **119.2.5.8** *P* **106** *L* **5** # 46

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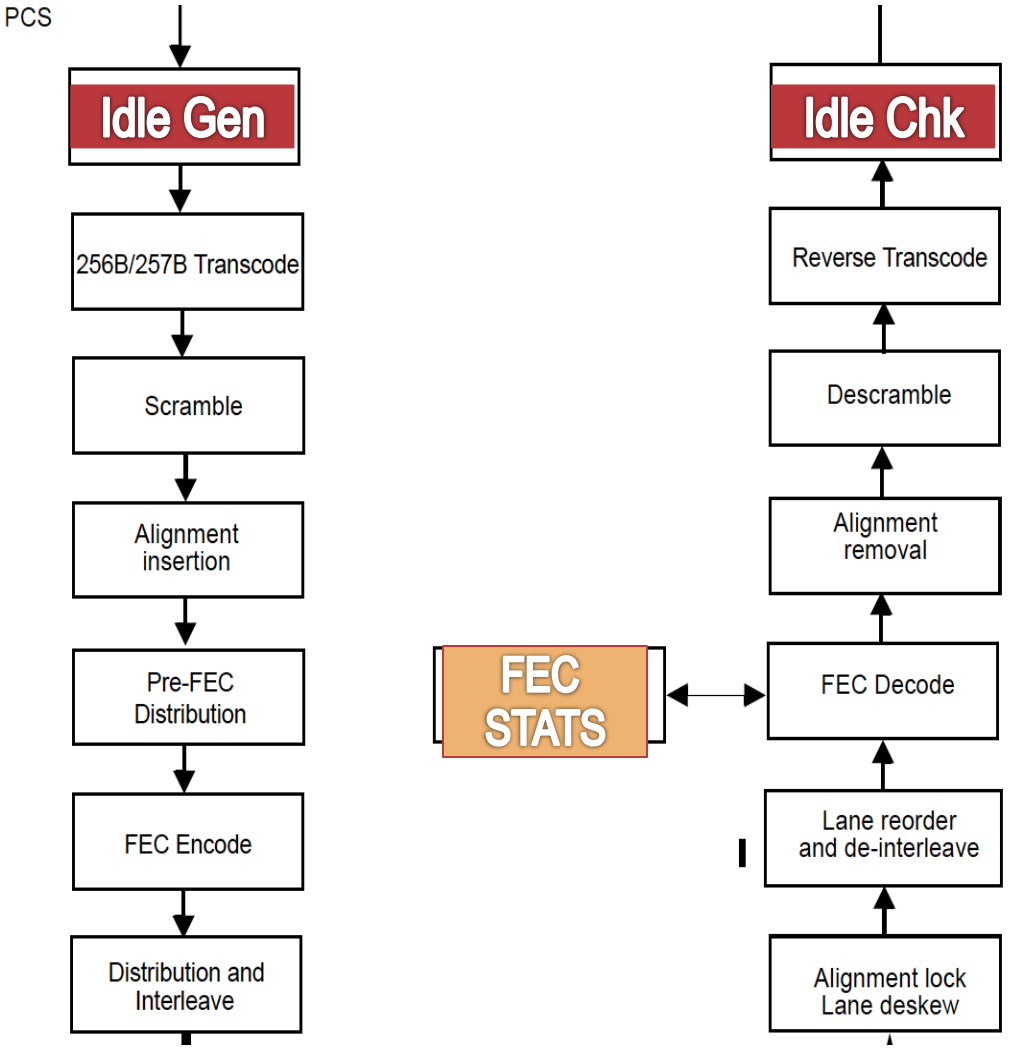
*Comment Type* **T** *Comment Status* **X**

What is the point of the scrambled idle checker? FEC statistics provide superior granularity of error rate (10b checking instead of 66b) and you need the FEC engine to be running to provide valid data to the output of the descrambler. If you can't link up a full 400G PHY, then use a PMA test pattern. (Scrambled Idle Generation is needed to enable PCS to generate valid FEC data streams)

*SuggestedRemedy*

Remove the scramble idle checker from clause 119.

# Test Mode Datapath



# Idle Checker

- **Counts the number of times a 66b block doesn't match IDLE block**

- **Idle Checker is after FEC engine**
  - So only time an invalid IDLE block would be seen is when an uncorrectable codeword is received.

# FEC STATS

- **Per Lane RS-symbol checkers**
  - Each PCS lane provides error count checked on a 10b granularity
- **Corrected codewords**
  - Count of number of corrected codewords, occurrences when 1-15 RS-symbols were detected having errors
- **Uncorrected codewords**
  - Count of number of uncorrected codewords, occurrences when >=16 RS-symbols were detected having errors

# RS-FEC Operating modes for IDLE checking

- **All On –**
  - Every uncorrected codeword would induce 72[1] or 80 IDLE check violations since all sync headers are corrupted by error indication
- **Bypass Indication[2] –**
  - Uncorrectable error blocks will randomize the amount the errors in the data stream, so the number of IDLE check violations will not indicate an accurate representation of the errors received.
- **Detect Only[3] –**
  - Mandated that indication is active, so any error on the link will cause 72 or 80 IDLE check violations to occur.

1. 72 occurs when AM block is present in the codeword
2. Mode availability depends on comment #47 resolution
3. Mode availability depends on comment #129 resolution

# Conclusion

- **Remove the idle checker since it's count isn't representative of the errors coming in on the received PCS lanes**
  - Gain no information on correctable codewords
  - Uncorrectable codewords cause large count increase such that idle check counter would likely be roughly 80x the uncorrectable codeword count
- **Rely on the FEC stats when testing with FEC input data**
  - per PCS lane error count with finer granularity (10b v 66b)
  - count of when >= 16 errors occurrences happened (when the idle checked would count errors)
- **Leave the Idle Gen in place to provide a defined method to generate a valid FEC data stream from the PCS**